J.B. INSTITUTE OF ENGINEERING AND TECHNOLOGY

(UGC AUTONOMOUS)

Bhaskar Nagar, Yenkapally Village, Moinabad Mandal, R.R. District, Hyderabad - 500075

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

3-Day VLSI Training Session on Cadence Software for IC Design

2nd, 3rd, and 4th

September 2025

Coordinator **HOD-ECE**

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Report
On
"3-Day VLSI training session on Cadence Software for IC Design"

Vision of Institute:

To be a centre of excellence in Engineering education, research and application of knowledge to benefit society with ethical values.

Mission of Institute:

1. To provide world class engineering education, encourage research and Development.
2. To evolve innovative applications of technology and develop entrepreneurship.
3. To mould the students into socially responsible and capable leaders.

Vision of ECE Department:

To be a guiding force enabling multifarious applications in Electronics and Communications Engineering, promote innovative research in the latest technologies to meet societal needs

Mission of ECE Department:

1. To provide and strengthen core competencies among the students through expert training and industry interaction.
2. To promote advanced designing and modelling skills to sustain technical development and lifelong learning in ECE.
3. To promote social responsibility and ethical values, within and outside the department.

About the Department:

The Department of ECE is best known for its talented and dedicated professionals renowned for their excellence in various specializations in the field of Electronics & Communication Engineering. For the last ten years, the students of ECE, who walked out of the portals of the institute successfully, holding their degrees, were immediately inducted into the MNCs of high reputation in India & abroad. The intake of B. Tech Program is 120 and of MTech program in VLSI System Design is 18. Department of ECE is having professional societies like IEEE, Department clubs etc.

Report:

This report outlines the key activities and learnings from an intensive three-day Cadence Virtuoso IC Design training held from September 2nd to September 4th, 2025. Day one focused on the complete full-custom design flow using 180nm technology, including the practical design of a CMOS inverter and a NAND gate. Day two transitioned to the semi-custom RTL-to-GDSII flow with 90nm technology, using a 4-bit binary counter as a case study. The third day was dedicated to a hands-on session, allowing for the practical application of the IC design concepts learned. The training provided a strong, hands-on foundation in VLSI design methodologies and comprehensive exposure to industry-standard Cadence tools, leaving participants well-prepared for a career in the field.

About the Event:

The training was an intensive, three-day deep dive into the world of IC design, covering the complete end-to-end process for both full-custom and semi-custom methodologies. Day 1 focused on the fundamentals of full-custom design using 180nm technology, while Day 2 explored the more complex RTL-to-GDSII semi-custom flow using a 90nm technology node. The sessions combined theoretical instruction with practical, hands-on examples to solidify understanding.

Objective:

The primary objective of this three-day training program was to gain a comprehensive, hands-on understanding of both full-custom and semi-custom Integrated Circuit (IC) design flows using the Cadence tool suite. The key goals were:

- To build a strong foundational and practical knowledge base in Very Large-Scale Integration (VLSI) design.
- To understand the complete end-to-end design process, from initial schematic entry and RTL coding to the final GDSII file generation ready for fabrication.
- To gain practical experience with industry-standard tools for simulation, layout, physical verification, and synthesis.
- To apply theoretical concepts to real-world design examples, such as a CMOS inverter and a 4-bit counter, to solidify understanding and build practical skills.

Engagement and Activities

The training was highly interactive, with a strong emphasis on applying theoretical concepts to practical design challenges. Key hands-on activities included:

- **Full-Custom Design:**
  - Designed a CMOS inverter from scratch.
  - Designed a NAND gate using PMOS and NMOS transistors.
  - These designs were taken through the entire flow from schematic to layout and verification.
- **Semi-Custom Design:**

- Worked through the complete RTL-to-GDSII flow using a 4-bit binary up-down counter as a practical case study.
- Engaged in a floorplanning session, learning the strategy behind using different metal layers for horizontal and vertical routing.

Software and tools mentioned

The training provided an overview and practical exposure to a wide range of industry-standard Cadence tools:

- **Virtuoso Schematic Editor:** For schematic entry.
- **Spectre:** For circuit simulation.
- **Virtuoso Layout Suite:** For creating physical layouts.
- **Assura:** For physical verification (DRC & LVS).
- **Quantus:** For RC Extraction.
- **Simvision:** For analyzing simulation waveforms.
- **Genus:** For synthesis.
- **Conformal LEC:** For logical equivalence checking and verification.

Topics and Processes covered

The curriculum was comprehensive and covered the critical stages of modern IC design:

Day 1: Full-Custom IC Design Flow

- Schematic Entry
- Simulation and Analysis
- Layout Creation
- Design Rule Check (DRC) & Layout vs. Schematic (LVS)
- Parasitic RC Extraction
- GDSII File Generation

Day 2: Semi-Custom IC Design Flow (RTL-to-GDSII)

- Specification & RTL Coding
- Functional Simulation
- Synthesis
- Timing Simulation
- Floorplanning and Power Planning
- Placement
- Clock Tree Synthesis (CTS)
- Routing
- Final GDSII Generation

Outcomes and Impact

The training provided a robust foundational knowledge base in VLSI design. The hands-on experience of taking circuits from concept to a fabrication-ready file was invaluable. This practical understanding of the complete design flow is crucial for a career in VLSI, providing the skills and confidence to tackle real-world IC design challenges. The session also provided valuable career guidance, including a list of key VLSI companies and resources for continued learning.

Feedback and Suggestions

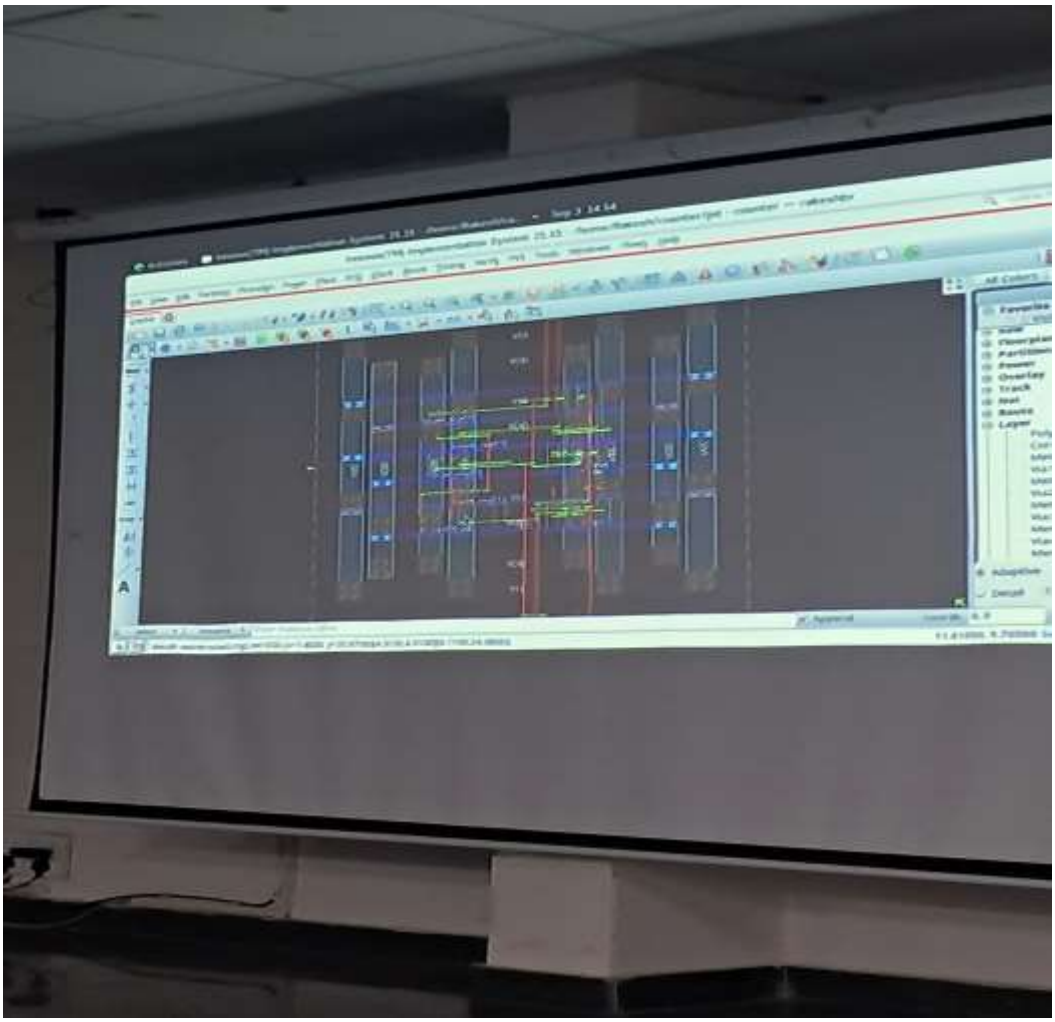
The feedback for the session was overwhelmingly positive. The instructor, Rakesh B R, was highly praised for his expert guidance, clear instruction, and ability to effectively walk participants through complex design flows for both the CMOS inverter, NAND gate, and the 4-bit counter.

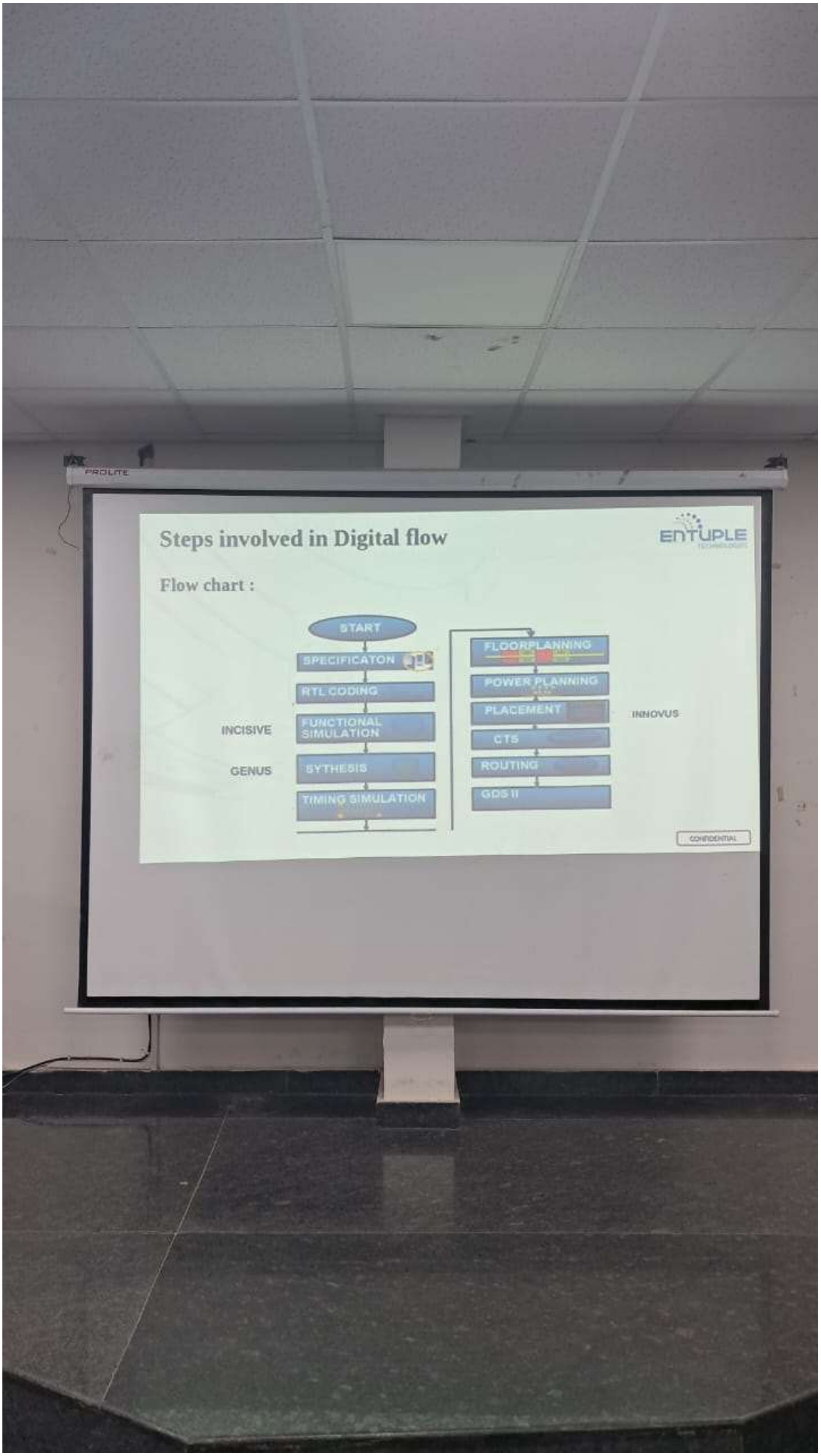
Conclusion

The three-day Cadence Virtuoso training was a fantastic and highly effective program. It successfully bridged the gap between theoretical knowledge and practical application. The first two days provided a solid understanding of the entire IC design lifecycle, and on the third day, all students applied this knowledge by designing ICs. The skills acquired are directly applicable to the VLSI industry and have significantly increased my excitement and preparedness for a career in this field. I look forward to applying this knowledge in future projects.

PHOTOGRAPHS:


EDTUPLE
TECHNOLOGIES
CIC Design flow
using
Cadence EDA Design Tools
Rakesh B R
Field Application Engineer
2nd September 2025
cadence




Steps involved in Digital flow
ENTUPLE
Flow chart :
START
SPECIFICATON
RTL CODING
FUNCTIONAL SIMULATION
SYTHESIS
TIMING SIMULATION
INCISIVE
GENUS
FLOORPLANNING
POWER PLANNING
PLACEMENT
CTS
ROUTING
GDS II
INNOVUS
CONFIDENTIAL


ENTUPLE
TECHNOLOGIES
CIC Design flow
using
Cadence EDA Design Tools
GPS Map Camera
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