IC APPLICATIONS LAB MANUAL

II BTECH, ECE

2nd SEMESTER

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

J B Institute of Engineering and Technology
(UGC AUTONOMOUS)
Accredited by NAAC & NBA, Approved by AICTE,
Permanently Affiliated to JNTUH
Bhaskar Nagar, Yenkapally (V), Moinabad (M),
Hyderabad-500075, Telangana, India

INSTITUTE VISION

To be a centre of excellence in engineering and management education, research and application of knowledge to benefit society with blend of ethical values and global perception.

INSTITUTE MISSION

1. To provide world class engineering education, encourage research and development.
2. To evolve innovative applications of technology and develop entrepreneurship.
3. To mould the students into socially responsible and capable leaders.

DEPARTMENT VISION

To be a guiding force enabling multifarious applications in Electronics and Communications Engineering, promote innovative research in the latest technologies to meet societal needs.

DEPARTMENT MISSION

M1: To **provide** and strengthen core competencies among the students through expert training and industry interaction.

M2: To **promote** advanced designing and modeling skills to sustain technical development and lifelong learning in ECE.

M3: To **promote** social responsibility and ethical values, within and outside the department

PEO'S, PO'S & PSOS

Program Educational Objectives (PEOs):	
PEO 1	Practice Technical skills widely in industrial, societal and real time applications.
PEO 2	Engage in the pursuit of higher education, delve into extensive research and development endeavours, and explore creative and innovative ventures in the domains of science, engineering, technology.
PEO 3	Exhibit professional ethics and moral values and capability of working with professional skills to contribute towards the need of industry and society.

Program Outcomes (POs)	
PO1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7	**Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	**Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs):	
PSO 1	Carry out the Analysis and Design different Analog & Digital circuits with given specifications.
PSO 2	Construct and test different communication systems for various applications.

CODE OF CONDUCT FOR THE LABORATORIES

➢ All students must observe the Dress Code while in the laboratory.

➢ Sandals or open-toed shoes are NOT allowed.

➢ Foods, drinks and smoking are NOT allowed.

➢ All bags must be left at the indicated place.

➢ The lab timetable must be strictly followed.

➢ Be PUNCTUAL for your laboratory session.

➢ Program must be executed within the given time.

➢ Noise must be kept to a minimum.

➢ Workspace must be kept clean and tidy at all time.

➢ Handle the systems and interfacing kits with care.

➢ All students are liable for any damage to the accessories due to their own negligence.

➢ All interfacing kits connecting cables must be RETURNED if you take from the lab supervisor.

➢ Students are strictly PROHIBITED from taking out any items from the laboratory.

➢ Students are NOT allowed to work alone in the laboratory without the Lab Supervisor ➢ USB Ports have been disabled if you want to use USB drive consult lab supervisor.

➢ Report immediately to the Lab Supervisor if any malfunction of the accessories, is there. Before leaving the lab • Place the chairs properly. • Turn off the system properly • Turn off the monitor. • Please check the laboratory notice board regularly for updates

IC APPLICATIONS SYLLABUS

Minimum Twelve Experiments to be conducted: (Six from each part A & B)

(IC APPLICATIONS LAB):

Experiment-1:Adder,Subtractor,usingIC741Op-Amp.
Experiment-2:InvertingandNonInvertingComparatorusingIC741Op-Amp.
Experiment-3:IntegratorandDifferentiatorusingIC741Op-Amp.
Experiment-4:Active Low Pass &High Pass Butterworth(second Order).
Experiment-5:Sample and Hold circuit using Op-Amp.
Experiment-6:RCPhaseShiftandWienBridgeOscillatorsusingIC741Op-Amp.
Experiment-7:WaveformgeneratorsusingIC741.
Experiment-8:IC555timerinMonostableandAstableoperation.
Experiment-9:SchmitttriggercircuitsusingIC741&IC555.
Experiment-10:IC565–PLL.
Experiment-11:VoltageregulatorIC723,threeterminalvoltageregulators-7805,7809,7912.
Experiment-12:A/D and D/A converters.

INTEGRATED CIRCUITS AND APPLICATIONS LAB

INDEX

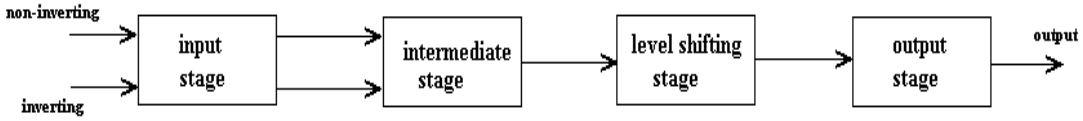
STUDY OF OP AMPS - IC 741, IC 555-FUNCTIONING, PARAMETERS AND SPECIFICATIONS

IC 741

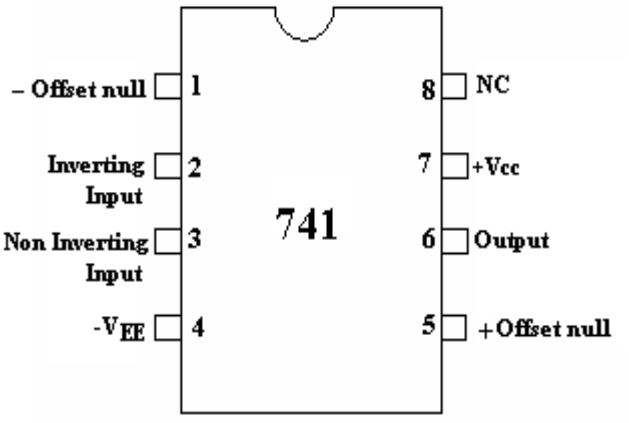
General Description:

The IC 741 is a high performance monolithic operational amplifier constructed using the planer epitaxial process. High common mode voltage range and absence of latch-up tendencies make the IC 741 ideal for use as voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier and general feedback applications.

Block Diagram of Op-Amp:



Pin Configuration:



Features:

1. No frequent compensation required.
2. Short circuit protection
3. Offset voltage null capability.
4. Large common mode and differential voltage ranges
5. Low power consumption
6. No latch-up

Specifications:

1. Voltage gain A = α typically 2,00,000
2. I/P resistance R_L = α Ω, practically 2MΩ
3. O/P resistance R =0, practically 75Ω
4. Bandwidth = α Hz. It can be operated at any frequency.
5. Common mode rejection ratio = α (Ability of op amp to reject noise voltage)
6. Slew rate + α V/μsec
   (Rate of change of O/P voltage)
7. When $V_1 = V_2$, V_D=0
8. Input offset voltage (Rs ≤ 10KΩ) max 6 mv.
9. Input offset current = max 200nA
10. Input bias current: 500nA
11. Input capacitance: typical value 1.4pF
12. Offset voltage adjustment range: ± 15mV.
13. Input voltage range: ± 13V
14. Supply voltage rejection ratio: 150 μV/V
15. Output voltage swing: + 13V and – 13V for R_L > 2KΩ
16. Output short-circuits current: 25mA.
17. supply current: 28mA.
18. Power consumption: 85mW
19. Transient response: rise time= 0.3 us Overshoot= 5%

Applications:

1. AC and DC amplifiers
2. Active filters
3. Oscillators
4. Comparators
5. Regulators

IC 555:

Description:

The operation of SE/NE 555 timer directly depends on its internal function. The three equal resistors R_1, R_2, R_3 serve as internal voltage divider for the source voltage. Thus one-third of the source voltage V_{CC} appears across each resistor.

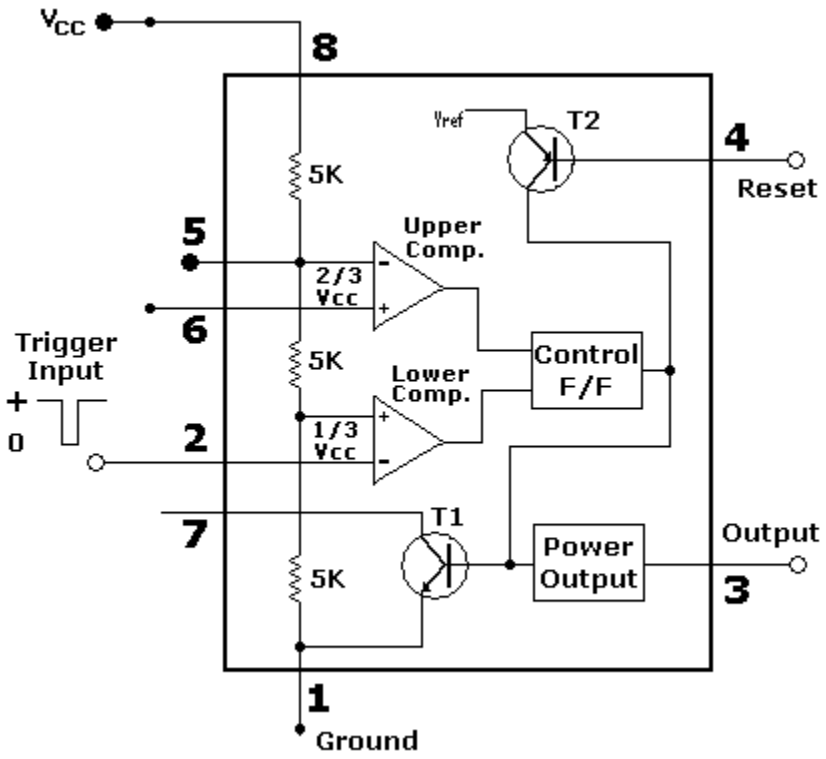
Comparator is basically an Op amp which changes state when one of its inputs exceeds the reference voltage. The reference voltage for the lower comparator is +1/3 V_{CC}. If a trigger pulse applied at the negative input of this comparator drops below +1/3 V_{CC}, it causes a change in state. The upper comparator is referenced at voltage +2/3 V_{CC}. The output of each comparator is fed to the input terminals of a flip flop.

The flip-flop used in the SE/NE 555 timer IC is a bistable multivibrator. This flip flop changes states according to the voltage value of its input. Thus, if the voltage at the threshold terminal rises above +2/3 V_{CC}, it causes upper comparator to cause flip-flop to change its states. On the other hand, if the trigger voltage falls below +1/3 V_{CC}, it causes lower comparator to change its states. Thus, the output of the flip flop is controlled by the voltages of the two comparators. A change in state occurs when the threshold voltage rises above +2/3 V_{CC} or when the trigger voltage drops below +1/3 V_{cc}.

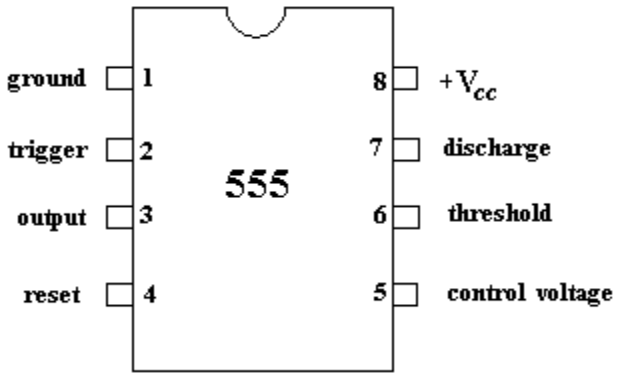
The output of the flip-flop is used to drive the discharge transistor and the output stage. A high or positive flip-flop output turns on both the discharge transistor and the output stage. The discharge transistor becomes conductive and behaves as a low resistance short circuit to ground. The output stage behaves similarly. When the flip-flop output assumes the low or zero states reverse

action takes place i.e., the discharge transistor behaves as an open circuit or positive V_{CC} state. Thus, the operational state of the discharge transistor and the output stage depends on the voltage applied to the threshold and the trigger input terminals.

Block Diagram of IC 555:



Pin Configuration:



Function of Various Pins of 555 IC:

Pin (1) of 555 is the ground terminal; all the voltages are measured with respect to this pin.

Pin (2) of 555 is the trigger terminal, If the voltage at this terminal is held greater than one-third of V_{CC}, the output remains low. A negative going pulse from V_{cc} to less than $V_{ec}/3$ triggers the output to go High. The amplitude of the pulse should be able to make the comparator (inside the IC) change its state. However the width of the negative going pulse must not be greater than the width of the expected output pulse.

Pin (3) is the output terminal of IC 555. There are 2 possible output states. In the low output state, the output resistance appearing at pin (3) is very low (approximately 10 Ω). As a result the output current will goes to zero , if the load is connected from Pin (3) to ground , sink a current I_{Sink} (depending upon load) if the load is connected from Pin (3) to ground, and sinks zero current if the load is connected between $+V_{CC}$ and Pin (3).

Pin (4) is the Reset terminal. When unused it is connected to $+V_{cc}$. Whenever the potential of Pin (4) is drives below 0.4V, the output is immediately forced to low state. The reset terminal enables the timer over-ride command signals at Pin (2) of the IC.

Pin (5) is the Control Voltage terminal. This can be used to alter the reference levels at which the time comparators change state. A resistor connected from Pin (5) to ground can do the job. Normally a 0.01μF capacitor is connected from Pin (5) to ground. This capacitor bypasses supply noise and does not allow it to affect the threshold voltages.

Pin (6) is the threshold terminal. In both astable as well as monostable modes, a capacitor is connected from Pin (6) to ground. Pin (6) monitors the voltage across the capacitor when it charges from the supply and forces the already high O/p to Low when the capacitor reaches $+2/3\ V_{CC}$.

Pin (7) is the discharge terminal. It presents an almost open circuit when the output is high and allows the capacitor charge from the supply through an external resistor and presents an almost short circuit when the output is low.

Pin (8) is the $+V_{cc}$ terminal. 555 can operate at any supply voltage from +3 to +18V.

Features of 555 IC

1. The load can be connected to o/p in two ways i.e. between pin 3 & ground 1 or between pin 3 & V_{CC} (supply)
2. 555 can be reset by applying negative pulse, otherwise reset can be connected to $+V_{cc}$ to avoid false triggering.
3. An external voltage affects threshold and trigger voltages.
4. Timing from microseconds through hours.
5. Mono astable and bi stable operation
6. Adjustable duty cycle
7. Output compatible with CMOS, DTL, TTL
8. High current output sink or source 200mA
9. High temperature stability
10. Trigger and reset inputs are logic compatible.

Specifications:

1.	Operating temperature	:	SE 555-- -55^oC to 125^oC NE 555-- 0^o to 70^oC
2.	Supply voltage	:	+5V to +18V
3.	Timing	:	µSec to Hours
4.	Sink current	:	200mA
5.	Temperature stability	:	50 PPM/^oC change in temp or 0-005% /^oC.

Applications:

1. Mono stable and A stable Multi vibrators
2. dc-ac converters
3. Digital logic probes
4. Waveform generators
5. Analog frequency meters
6. Tachometers
7. Temperature measurement and control
8. Infrared transmitters
9. Regulator & Taxi gas alarms etc.

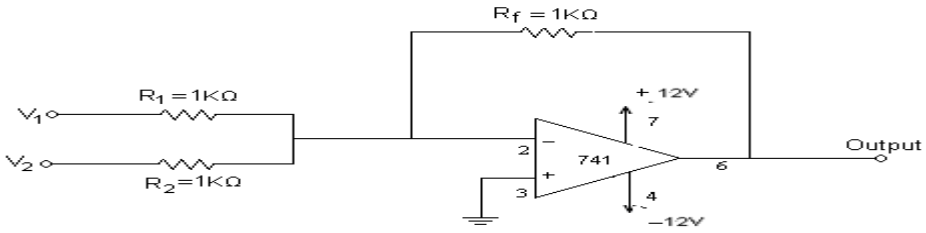
1. ADDER, SUBTRACTOR, USINGIC741OP-AMP

Aim:
To study the applications of IC 741 as adder, sub tractor, comparator.

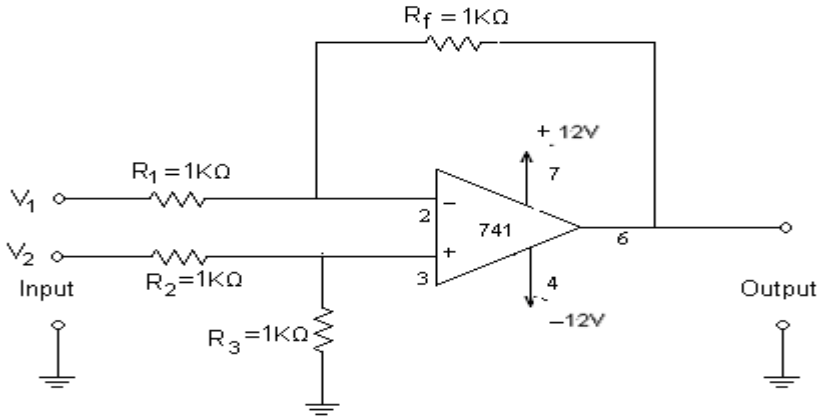
Apparatus:
1. IC 741
2. Resistors (1KΩ)—4
3. Function generator
4. Regulated power supply
5. IC bread board trainer
6. CRO
7. Patch cards and CRO probes

Circuit diagram:

Adder:



Subtractor:



Theory:

Adder:

Op-Amp may be used to design a circuit whose output is the sum of several input signals such as circuit is called a summing amplifier or summer. We can obtain either inverting or noninverting summer. The circuit diagrams show a two-input inverting summing amplifier. It has two input voltages V1and V2, two input resistors R1, R2 and a feedback resistor Rf. Assuming that op-amp is in ideal conditions and input bias current is assumed to be zero, there is no voltage drop across the resistor Rcomp and hence the non inverting input terminal is at ground potential.

By taking nodal equations.

V1/R1 +V2/R2 +V0/Rf =0

V0 = - [(Rf/R1) V1 +(Rf/R2) V2]

And here R1 = R2 = Rf = 1KΩ

V0 = -(V1 +V2)

Thus, output is inverted and sum of input.

Subtractor:

A basic differential amplifier can be used as a sub tractor. It has two input signals V1 and V2 and two input resistances R1 and R2 and a feedback resistor Rf. The input signals are scaled to the desired values by selecting appropriate values for the external resistors. From the figure, the output voltage of the differential amplifier with a gain of '1' is.

V0 = -R/Rf(V2-V1)

V0 = V1-V2.

Also, R1 =R2 = Rf =1KΩ.

Thus, the output voltage V0 is equal to the voltage V1 applied to the noninverting terminal minus voltage V2 applied to inverting terminal. Hence the circuit is a sub tractor.

Observations:

Adder:

V_1(V)	V_2(V)	V_o(V)
2.5	2.5	
3.8	4.0	

Subtractor:

V_1(V)	V_2(V)	V_o(V)
2.5	3.3	
4.1	5.7	

Procedure:

Adder:
1. connections are made as per the circuit diagram.
2. Apply input voltage 1) V1= 5v, V2=2v
2) V1= 5v, V2=5v
3) V1= 5v, V2=7v.
3. Using Millimeter measure the dc output voltage at the output terminal.
4. For different values of V1 and V2 measure the output voltage.

Subtractor:
1. Connections are made as per the circuit diagram.
2. Apply input voltage 1) V1= 5v, V2=2v
2) V1= 5v, V2=5v
3) V1= 5v, V2=7v.
3. Using multi meter to measure the dc output voltage at the output terminal.
4. For different values of V1 and V2 measure the output voltage.

Comparator:
1. Connections are made as per the circuit diagram.
2. Select the sine wave of 10V peak to peak, 1K Hz frequency.
3. Apply the reference voltage 2V and trace the input and output wave forms.
4. Superimpose input and output waveforms and measure sine wave amplitude with reference to V ref.
5. Repeat steps 3 and 4 with reference voltages as 2V, 4V, -2V, -4V and observe the waveforms.
6. Replace sine wave input with 5V dc voltage and V ref= 0V.
7. Observe dc voltage at output using CRO.
8. Slowly increase V ref voltage and observe the change in saturation voltage.

Precautions:
1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

Result:
The operation of IC 741 Op-Amp as adder, sub tractor and comparator is studied and values are noted.

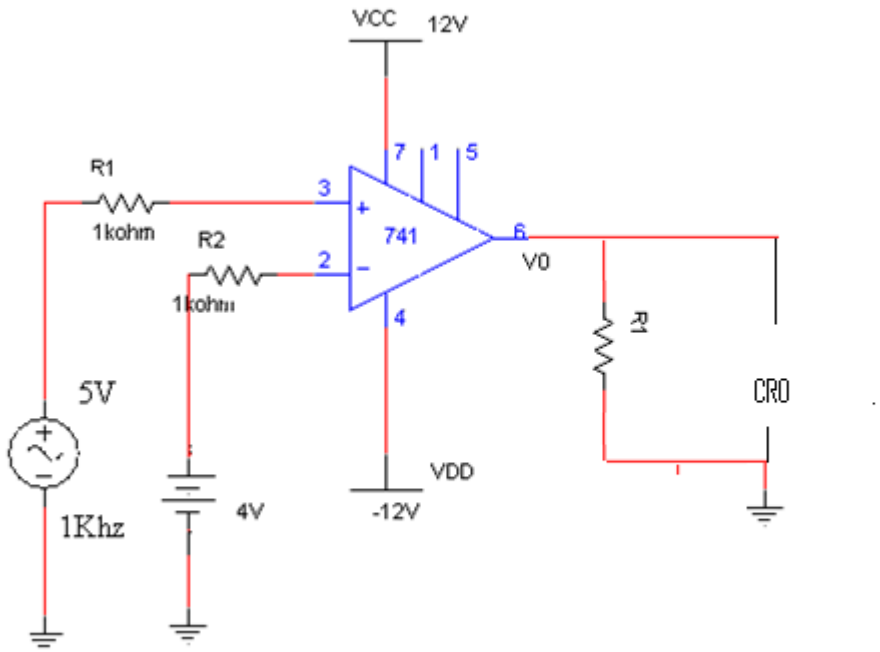
VIVA QUESTIONS:
1. What is an op-amp?
2. What are ideal characteristics of op amp?
3. What is the function of an adder?
4. What is meant by comparator?

2. INVERTING AND NON-INVERTING COMPARATOR USING IC 741 OP-AMP

Aim:
To study the applications of IC 741 as inverting and non-inverting comparator.

Apparatus:
1. IC 741
2. Resistors (1KΩ)—4
3. Function generator
4. Regulated power supply
5. IC bread board trainer
6. CRO
7. Patch cards and CRO probes

Circuit diagram:



Theory:

Comparator:

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open loop op-amp with output ±Vsat a in the ideal transfer characteristics.

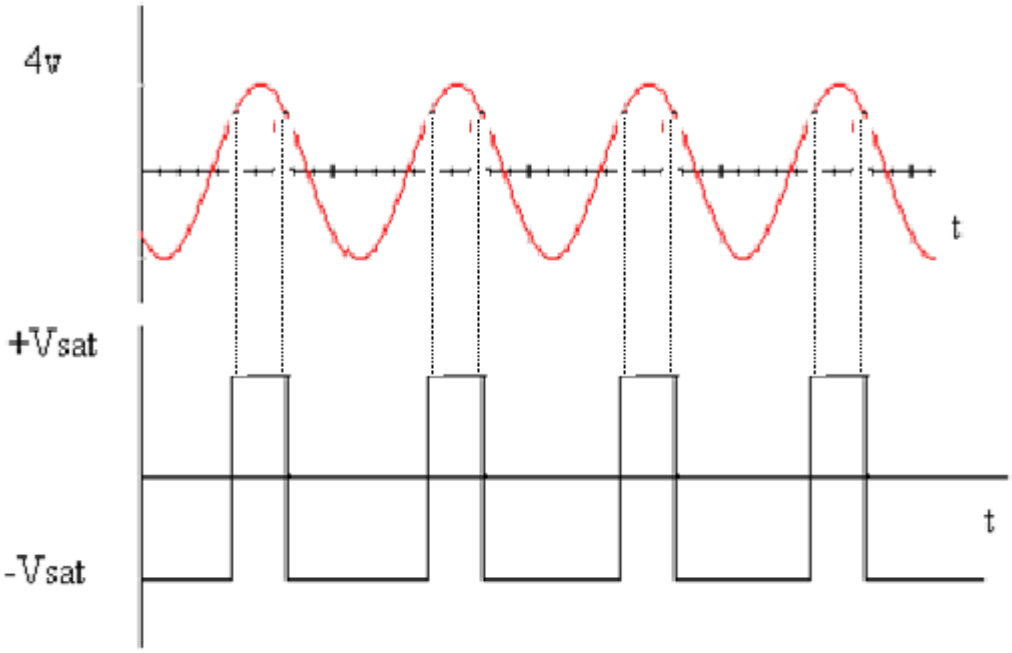
The change in the output state takes place with an increment in input Vi of only 2mv. This is the uncertainty region where output cannot be directly defined. There are basically 2 types of comparators.

1. Noninverting comparator and.
2. Inverting comparator.

The applications of comparator are zero crossing detector, window detector, time marker generator and phase meter.

OBSERVATIONS:

MODEL GRAPH:



Comparator:

1. Connections are made as per the circuit diagram.
2. Select the sine wave of 10V peak to peak, 1K Hz frequency.
3. Apply the reference voltage 2V and trace the input and output wave forms.
4. Superimpose input and output waveforms and measure sine wave amplitude with reference to Vref.
5. Repeat steps 3 and 4 with reference voltages as 2V, 4V, -2V, -4V and observe the waveforms.
6. Replace sine wave input with 5V dc voltage and Vref= 0V.
7. Observe dc voltage at output using CRO.
8. Slowly increase Vref voltage and observe the change in saturation voltage.

Precautions:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

Result:

The operation of IC 741 Op-Amp as comparator is studied and values are noted.

Viva Questions:

1. What is an op-amp?
2. What are ideal characteristics of op amp?
3. What is meant by comparator?

3. INTEGRATOR AND DIFFERENTIATOR CIRCUITS USING IC 741

Aim: To design and verify the operation of an integrator and differentiator for a given input.

Apparatus required:

S. No	Equipment/Component name
1	741 IC Trainer Kit
2	CRO
3	Function generator
4	Patch Chords

Theory:

Integrator:

In an integrator circuit, the output voltage is integral of the input signal. The output voltage of an integrator is given by $V_o = -1/R_1C_f \int_o^t Vidt$

At low frequencies the gain becomes infinite, so the capacitor is fully charged and behaves like an open circuit. The gain of an integrator at low frequency can be limited by connecting a resistor in shunt with capacitor.

Differentiator: In the differentiator circuit the output voltage is the differentiation of the input voltage. The output voltage of a differentiator is given by $V_o = -RfC_1 \frac{dV_i}{dt}$ .The input impedance of this circuit decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise. At high frequencies circuit may become unstable.

Circuit Diagrams:

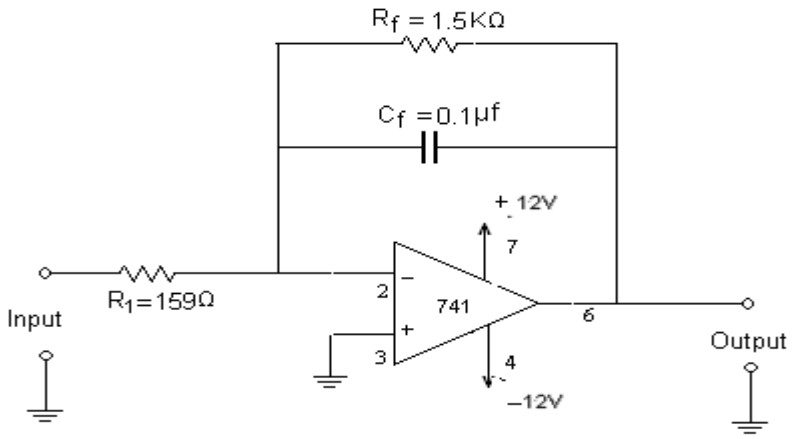


Fig 1: Integrator

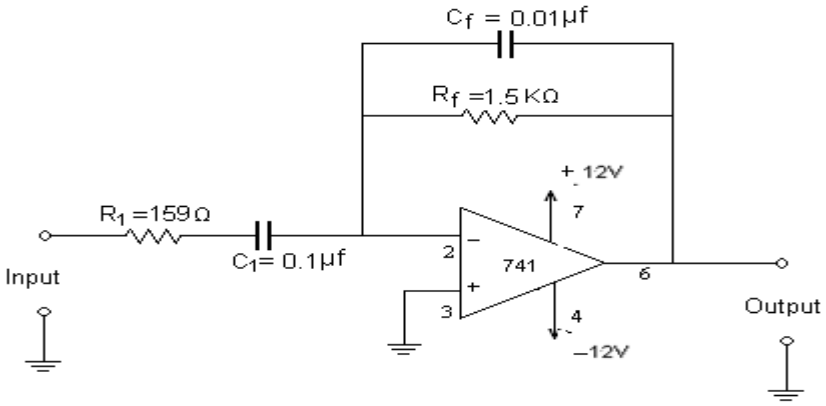


Fig 2: Differentiator

Design equations:

Integrator:

Choose $T = 2\pi R_f C_f$

Where T= Time period of the input signal

Assume C_f and find R_f

Select $R_f = 10R_1$

$$V_{o\,(p\text{-}p)} = \frac{-1}{R_1 C_f} \int_o^{T/2} V_{i(p-p)}\, dt$$

Differentiator

Select given frequency $f_a = 1/(2\pi R_f C_1)$, Assume C_1 and find R_f

Select $f_b = 10\ f_a = 1/2\pi R_1 C_1$ and find R_1

From $R_1C_1 = R_fC_f$, find Cf

Procedures:

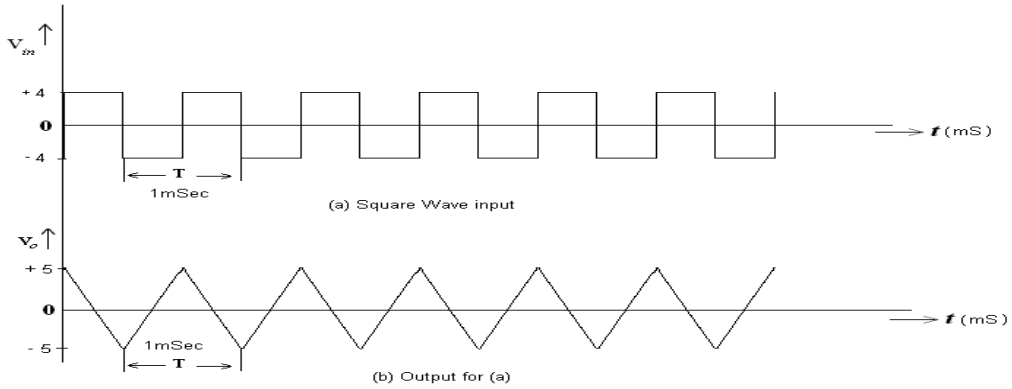
Integrator

1. Connect the circuit as per the diagram shown in Fig.
2. Apply a square wave/sine input of 4V(p-p) at 1KHz.
3. Observe the output at pin 6.
4. Draw input and output waveforms as shown in Fig.

Differentiator

1. Connect the circuit as per the diagram shown in Fig.
2. Apply a square wave/sine input of 4V(p-p) at 1KHz.
3. Observe the output at pin 6.
4. Draw the input and output waveforms as shown in Fig

Wave Forms:



Integrator

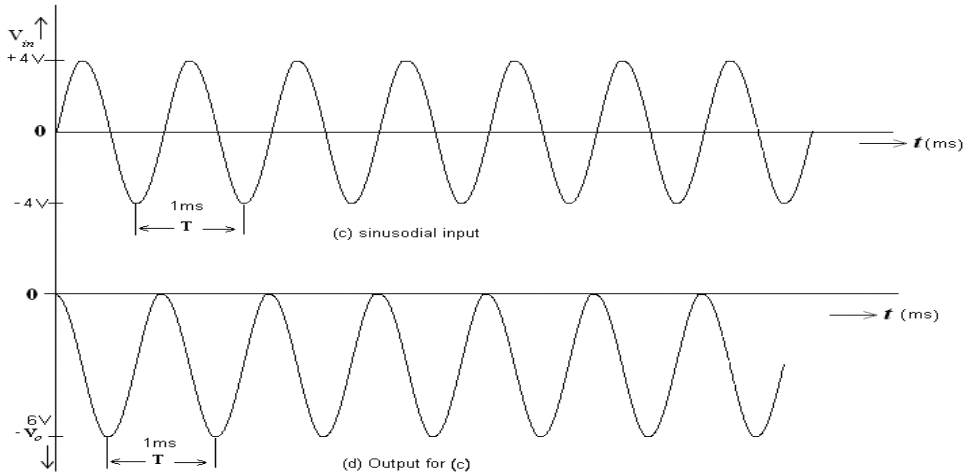
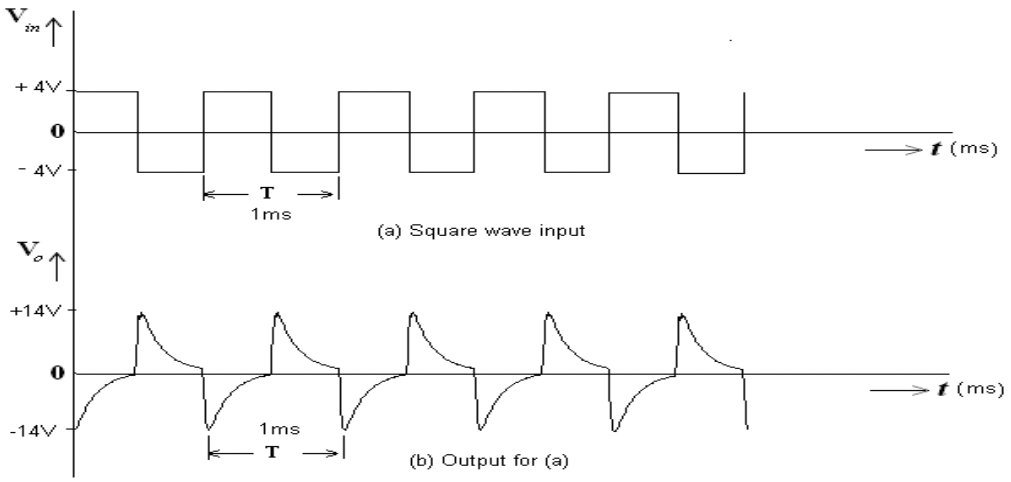


Fig 3: Input and output waves forms of integrator



Differentiator

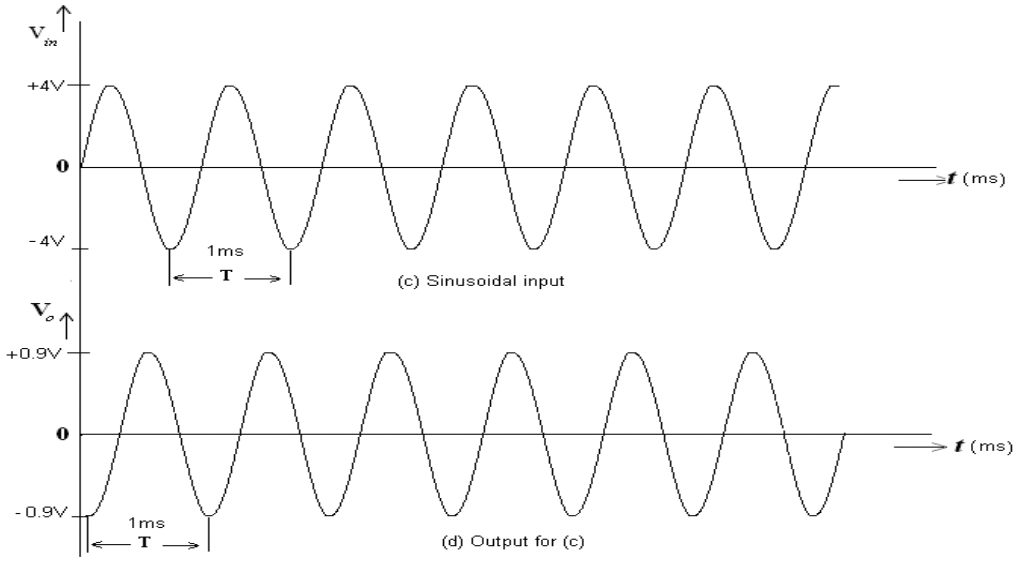


Fig 4: Input and output waveforms of Differentiator

Sample readings:

Integrator

Input –Square wave		**Output - Triangular**	
Amplitude (V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)
5	1		

Input –sine wave		**Output - cosine**	
Amplitude (V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)
5	1		

Differentiator

Input –square wave		**Output - Spikes**	
Amplitude (V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)
5	1		

Input –sine wave		**Output - cosine**	
Amplitude (V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)
5	1		

Model Calculations:

Integrator:

For T= 1 msec

$f_a = 1/T = 1$ KHz

$f_a = 1$ KHz $= 1/(2\pi R_f C_f)$

Assuming Cf= 0.1μf, R_f is found from $R_f=1/(2\pi f_a C_f)$

R_f=1.59 KΩ

$R_f = 10\ R_1$

R_1= 159Ω

Differentiator

For T = 1 msec

f= 1/T = 1 KHz

f_a = 1 KHz = $1/(2\pi R_f C_1)$

Assuming C_1= 0.1μf, R_f is found from $R_f=1/(2\pi f_a C_1)$

R_f=1.59 KΩ $f_b = 10\ f_a = 1/2\pi R_1 C_1$

for C_1= 0.1μf; R_1 =159Ω

Precautions: Check the connections before giving the power supply.

Readings should be taken carefully.

Result: For a given square wave and sine wave, output waveforms for integrator and differentiator are observed.

Inferences: Spikes and triangular waveforms can be obtained from a given square waveform by using differentiator and integrator respectively.

Questions & Answers:

1. What are the problems of ideal differentiator?

   Ans: At high frequencies the differentiator becomes unstable and breaks into oscillation. The differentiator is sensitive to high frequency noise.

2. What are the problems of ideal integrator?

   Ans: The gain of the integrator is infinite at low frequencies.

3. What are the applications of differentiator and integrator?

Ans: The differentiator used in wave shaping circuits to detect high frequency components in an input signal and also as a rate-of –change detector in FM demodulators.

The integrator is used in analog computers and analog to digital converters and signal-wave shaping circuits.

4. What is the need for R_f in the circuit of integrator?

   Ans: The gain of an integrator at low frequencies can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance $R_{f.}$

5. What is the effect of C_1 on the output of a differentiator?

   Ans: It is used to eliminate the high frequency noise problem.

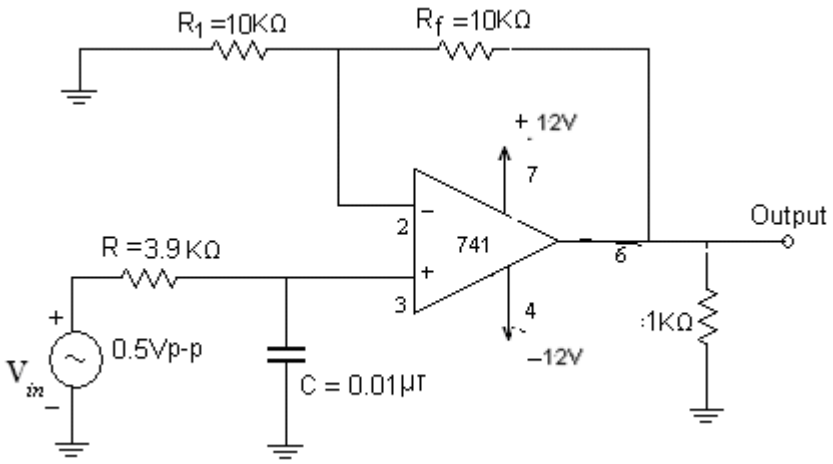
4. ACTIVE LOW PASS &HIGH PASS BUTTERWORTH (SECOND ORDER)

Aim:
To study Op-Amp as second order LPF and second order HPF and to obtain frequency response.

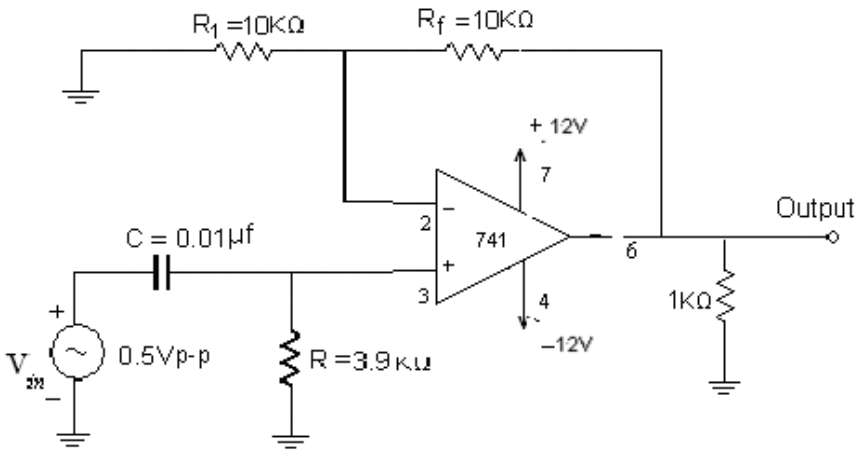
Apparatus:
1. IC 741.
2. Resistors (10KΩ--2, 560Ω, 330Ω
3. Capacitors(0.01Ω)
4. Bread board trainer
5. CRO
6. Function generator
7. connecting wires
8. Patch cards.

Circuit Diagram:

(a) LPF



(a) HPF



Theory:

Lowpass Filter:

A LPF allows frequencies from 0 to higher cut of frequency, f_H. At f_H the gain is 0.707 A_{max}, and after f_H gain decreases at a constant rate with an increase in frequency. The gain decreases 20dB each time the frequency is increased by 10. Hence the rate at which the gain rolls off after f_H is 20dB/decade or 6 dB/ octave, where octave signifies a two-fold increase in frequency. The frequency $f=f_H$ is called the cut off frequency because the gain of the filter at this frequency is down by 3 dB from 0 Hz. Other equivalent terms for cut-off frequency are -3dB frequency, break frequency, or corner frequency.

High pass filter:

The frequency at which the magnitude of the gain is 0.707 times the maximum value of gain is called low cut off frequency. Obviously, all frequencies higher than f_L are pass band frequencies with the highest frequency determined by the closed –loop band width all of the op-amp.

Design:

First Order LPF:

To design a Low Pass Filter for higher cut off frequency f_H = 4 KHz and pass band gain of 2

$f_H = 1/ (2\pi RC)$

Assuming C=0.01 µF, the value of R is found from

$R= 1/(2\pi f_H C)\ \Omega = 3.97K\Omega$

The pass band gain of LPF is given by $A_F = 1+ (R_F/R_1) = 2$

Assuming R_1=10 KΩ, the value of R_F is found from

$R_F=(AF-1)\ R_1=10K\Omega$

First Order HPF: To design a High Pass Filter for lower cut off frequency fL = 4 KHz and pass band gain of 2

$f_L = 1/ (2\pi RC)$

Assuming C=0.01 µF,the value of R is found from

$R= 1/(2\pi f_L C)\ \Omega = 3.97K\Omega$

The pass band gain of HPF is given by $A_F = 1+ (R_F/R_1)= 2$

Assuming R_1=10 KΩ, the value of R_F is found from

$R_F=(AF-1)\ R_1=10K\Omega$

Procedure:

First Order LPF

1. Connections are made as per the circuit diagram shown in Fig 1.
2. Apply sinusoidal wave of constant amplitude as the input such that op-amp does not go into saturation.
3. Vary the input frequency and note down the output amplitude at each step as shown in Table (a).
4. Plot the frequency response as shown in Fig 3.

First Order HPF

1. Connections are made as per the circuit diagrams shown in Fig 2.
2. Apply sinusoidal wave of constant amplitude as the input such that op-amp does not go into saturation.
3. Vary the input frequency and note down the output amplitude at each step as shown in Table (b).
4. Plot the frequency response as shown in Fig 4.

Observations:

Tabular Form and Sampled Values:

a) LPF

Input voltage V_{in} = 0.5V

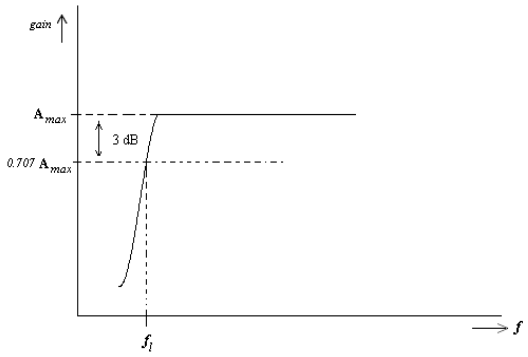
Frequency	O/P Voltage(V)	Voltage Gain Vo/Vi	Gain in dB
100Hz			
200Hz			
300Hz			
500Hz			
750Hz			
900Hz			
1KHz			
2KHz			
3KHz			
4KHz			
5KHz			
6KHz			
7KHz			
8KHz			
9KHz			
10KHz			

b) HPF

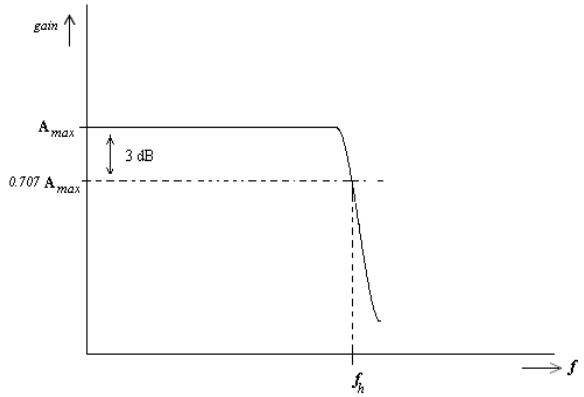
Frequency	O/P Voltage(V)	Voltage Gain Vo/Vi	Gain in dB
10KHz			
9KHz			
8KHz			
7KHz			
6KHz			
5KHz			
4KHz			
3KHz			
2KHz			
2KHz			
1KHz			
900Hz			
750Hz			

Model Graph:

High Pass Filter



Low Pass Filter



Precautions:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

Result:
The frequency response of LPF and HPF is plotted using IC741 Op-Amp.

VIVA QUESTIONS:

1. What is the function of the filter?
2. What are the different types of filters?
3. Define pass band and stop band of filters?
4. Define cut off frequency?
5. What is the difference between HPF&LPF?

5. SAMPLE AND HOLD CIRCUIT USING OPERATIONAL AMPLIFIER

Aim:

To construct and study the sample and hold circuit using operational amplifier IC 741.

Test equipment:

1. Hi-Q TEST EQUIPMENT PVT.LTD. Sample And Hold Circuit Using OP-Amp.
2. Signal Generators – 2Nos.
3. Oscilloscope.
4. Connecting Patch Cords.

Components required:

Resistors	R, R_L-10K	2No's
Pot	10K	1No
Capacitor	C- 0.1µf	1No
	470 µf /35V	2No's
	22 µf /25V	2No's
MOSFET	IRF630	1No
IC	741	1No
Diodes	IN4007	4No's
Regulators	7815,7915	1 No

Introduction:

The sample and hold circuit, as its name implies, samples an input signal and holds on to its last sampled value until the input is sampled again. Figure. 1 shows a sample and hold circuit using an op-amp with an EMOSFET. In this circuit the E-MOSFET works as a switch that is controlled

by the sample and hold control voltage Vs, and the capacitor *C* serves as a storage element. The circuit operates as follows. The analog signal Vi to be sampled is applied to the drain, and sample and hold control voltage Vs is applied to the gate of the E-MOSFET.

During the positive portion of Vs, the E-MOSFET conducts and acts as a closed switch. This allows input voltage to charge capacitor C. In other words, input voltage appears across C and in turn at the output, as shown in Figure 2. On the other hand, when Vs is zero, the E-MOSFET is *off* (nonconductive) and acts as an open switch. The only discharge path for C is, therefore, through the op-amp. However, the input resistance of the op-amp voltage follower is also very high; hence the voltage across C is retained. The time periods Ts of the sample and hold control voltage Vs during which the voltage across the capacitor is equal to the input voltage are called *sample periods.* The time periods T_H of Vs during which the voltage across the capacitor is constant are called *hold periods* [see Figure 2]. The output of the op-amp is usually processed / observed during hold periods. To obtain close approximation of the input waveform, the frequency of the sample-and-hold control voltage must be significantly higher than that of the input. In critical applications a

precision and/or high-speed op-amp is helpful. If possible, choose a lowleakage capacitor such as Teflon or polyethylene.

The sample and hold circuit is commonly used in digital interfacing and communications such as analog-to-digital and pulse modulation systems.

Procedure:

1. Connect the circuit as shown in Figure 1.

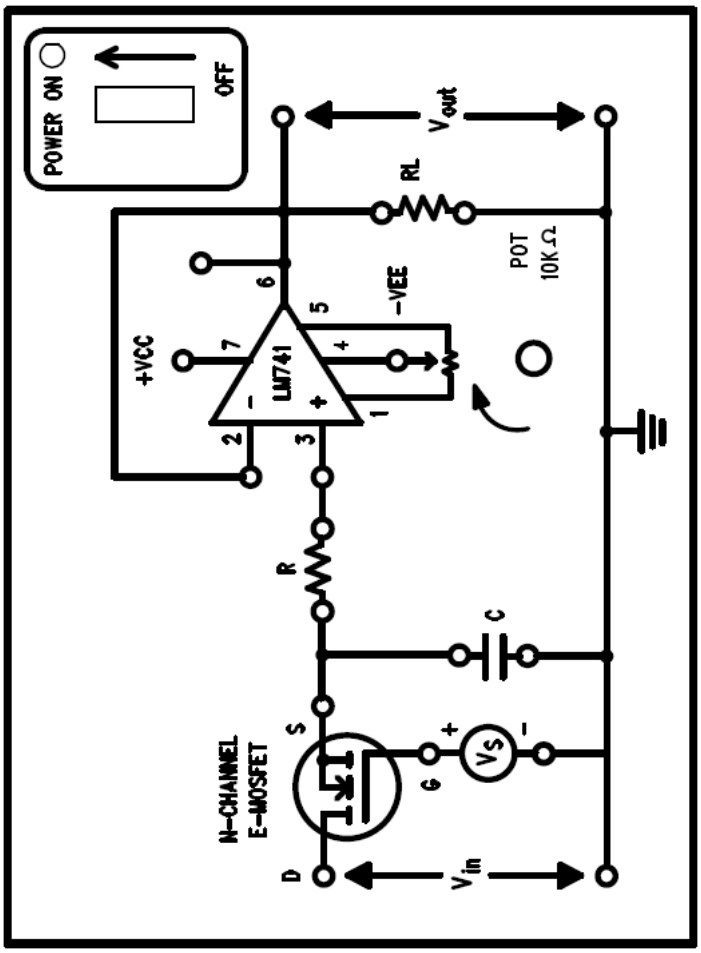
2. Switch on the trainer and observe for the power LED indication.

3. Observe the input and output waveforms on CRO.

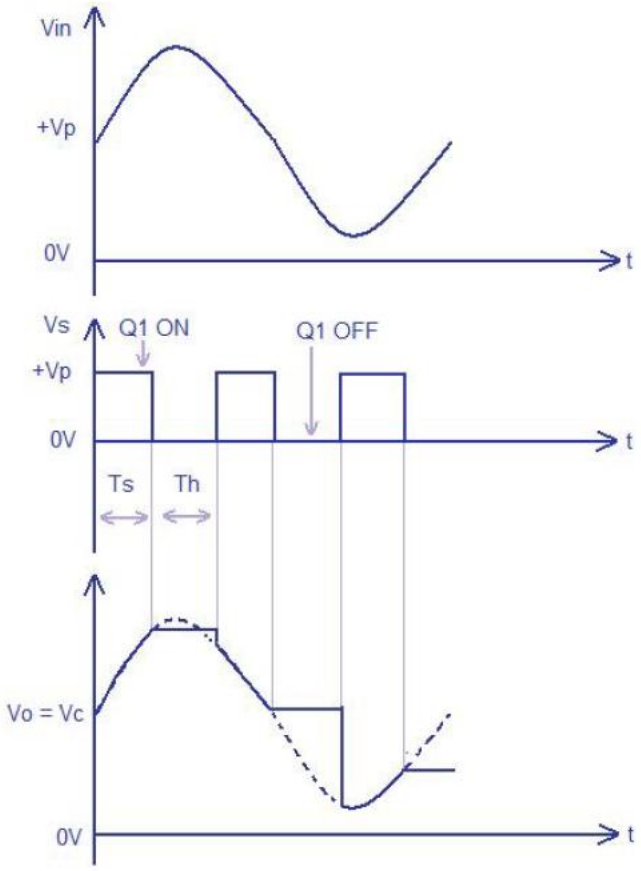
4. Now vary the input frequency and observe the sampling affect on the output waveform , comment on the result obtained.

5. Sample input and output waveforms as shown in fig. 2.

Circuit diagram:



Graph



input and output waveforms

6. RC PHASE SHIFT AND WIEN BRIDGE OSCILLATORS USINGI C741OP-AMP.

Aim: To design (i) phase shift and (ii) Wien Bridge oscillators for the given frequency of oscillation and verify it practically.

Apparatus required:

S. No	Equipment/Component name
1	IC 741 Trainer kit
2	CRO
3	Patch cards
4	CRO Cable
5	Adapter AC Voltage 0-18V

Theory:

The μA741 is a high performance monolithic operational amplifier constructed using the planar epitaxial process. High common mode voltage range and absence of latch-up tendencies make the μA741 ideal for use as voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier and general feedback applications.

In the phase shift oscillator, out of 360^o phase shift, 180^o phase shift is provided by the op-amp and another 180^o is by 3 RC networks. In the Wein bridge oscillator, the balancing condition of the bridge provides the total 360^o phase shift.

Circuit Diagrams:

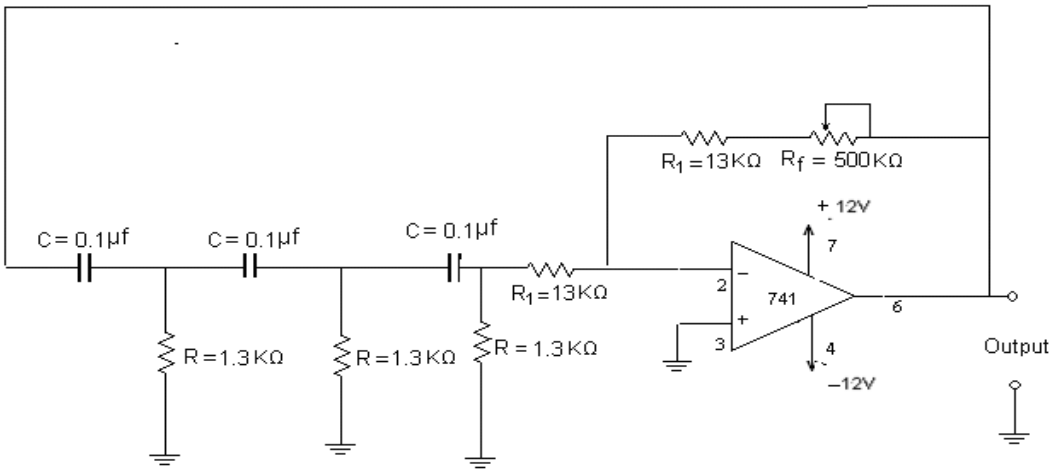


Fig 1: RC Phase shift oscillator

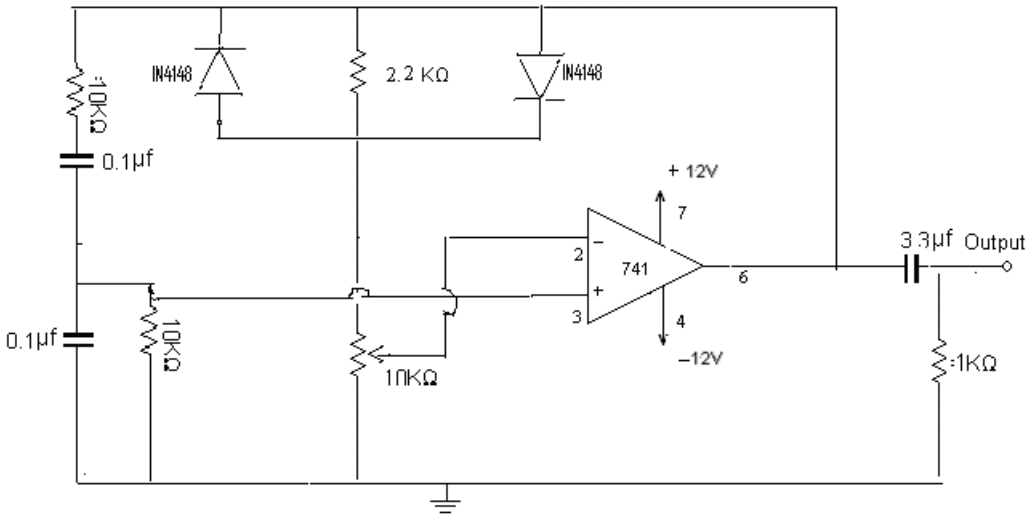


Fig 2: Wien Bridge oscillator

Design:

1. Phase shift oscillator

To design a phase shift oscillator with f_o =500 Hz

$f_o = 1/(2\pi RC\sqrt{6})$

and gain= R_F/R_1= 29

Assuming C = 0.1 µF, the value of R is found from

$R = 1/(2\pi f_o C\sqrt{6}) = 1.3$ KΩ

Take R_1 = 10R =13 KΩ

$R_F = 29R_1$ (use 500K pot)

2. Wien bridge Oscillator

To design a Wien bridge oscillator with f_o =5 KHz

$f_o = 1/2\pi RC$ and $R_F = 2R_1$

Assuming C = 0.01 µF, the value of R is found from

R= 1/2πfc= 3.18 KΩ

Take R_1 = 10 R=31.8 KΩ

$R_F = 2R_1$ (use 100K pot)

Procedure:

1. Phase shift oscillator

1. Connect the circuit as per the circuit diagram shown in Fig 1
2. Observe the output waveform on the CRO.
3. Vary the potentiometer to get the undistorted waveform as shown Fig a.
4. Measure the time period and amplitude of the output waveform.
5. Plot the waveforms on a graph sheet.

2. Wien bridgeOscillator

1. Connect the circuit as per the circuit diagram shown in Fig 2
2. Observe the output waveform on the CRO.
3. Vary the potentiometer to get the undistorted waveform as shown in Fig b
4. Measure the time period and amplitude of the output waveform.
5. Plot the waveforms on a graph sheet

Waveforms:

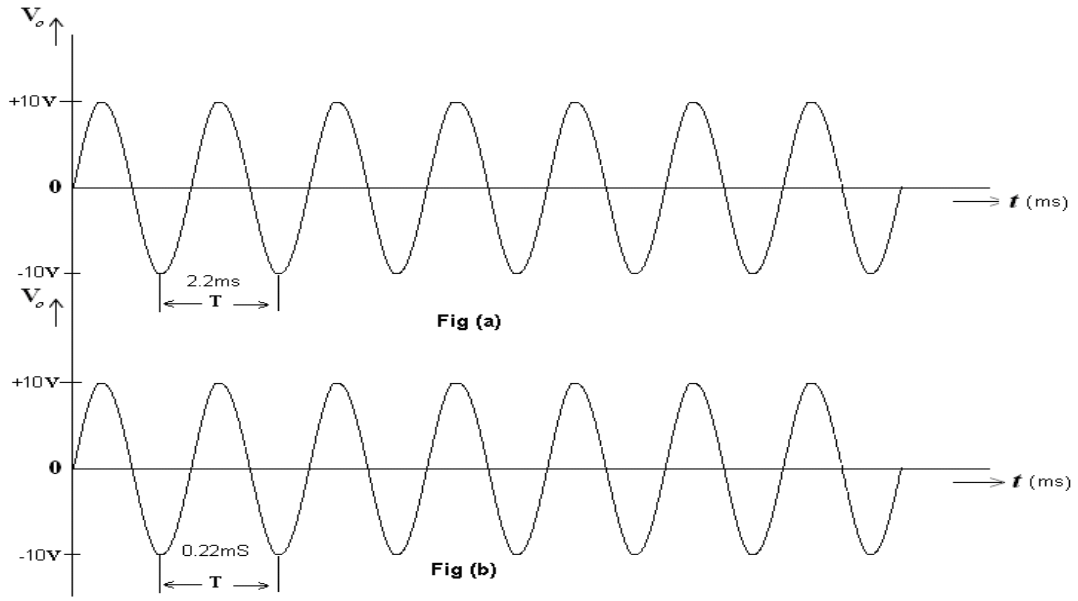


Fig (a): RC Phase Shift Oscillator, Fig (b): Wien Bridge Oscillator

Tabular Form:

1. Phase shift oscillator:

S. No	Amplitude (V_{P-P})	Time period (ms)	Practical frequency (Hz)	Theoretical frequency (Hz)
1	20V	2.2		

2. Wien bridge Oscillator:

S. No	Amplitude (V_{P-P})	Time period (ms)	Practical frequency (Hz)	Theoretical frequency (Hz)
1	20V	0.22ms		

Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Result:

RC phase shift and Wien bridge oscillators are designed, and output waveforms are observed as shown in Fig (a) and (b).

Inferences:

Sinusoidal waveforms can be designed by using RC phase shift and Wien-Bridge oscillators.

Questions & Answers:

1. How do you change the frequency of oscillation in RC phase shift and
   Ans: Wien bridge oscillators?
2. By varying either resistor R or capacitor C values
3. What are the applications of oscillators?
   Ans: Oscillators are used in radio, television, computers, and communications.
4. What is the advantage of using op amp in the oscillator circuit?
   Ans: Op amp is used to generate a variety of output wave forms.
5. How do you achieve fine variations in f_o ?
   Ans: Fine variations in fo can be achieved by changing the C value.
6. How do you achieve coarse variations in f_o ?
   Ans: Coarse variations in fo can be achieved by changing R value.

7. WAVEFORM GENERATION USING OP-AMP (SQUARE & TRIANGULAR)

Aim:
To generate square wave and Triangular wave form by using OPAMPs.

Apparatus required:
S. No Equipment/Component name Specifications/Value Quantity
1 741 IC Refer Appendix A 2
2 Capacitors 0.01µf, 0.001µf Each one
3 Resistors
4 Regulated Power supply (0 – 30V), 1A
5 Cathode Ray Oscilloscope (0 -20MHz)

Theory:

Function generator generates waveforms such as sine, triangular, square waves and so on of different frequencies and amplitudes. The circuit shown in Fig1 is a simple circuit which generates square waves and triangular waves simultaneously. Here the first section is a square wave generator and second section is an integrator. When square wave is given as input to integrator it produces triangular wave.

Circuit Diagram:

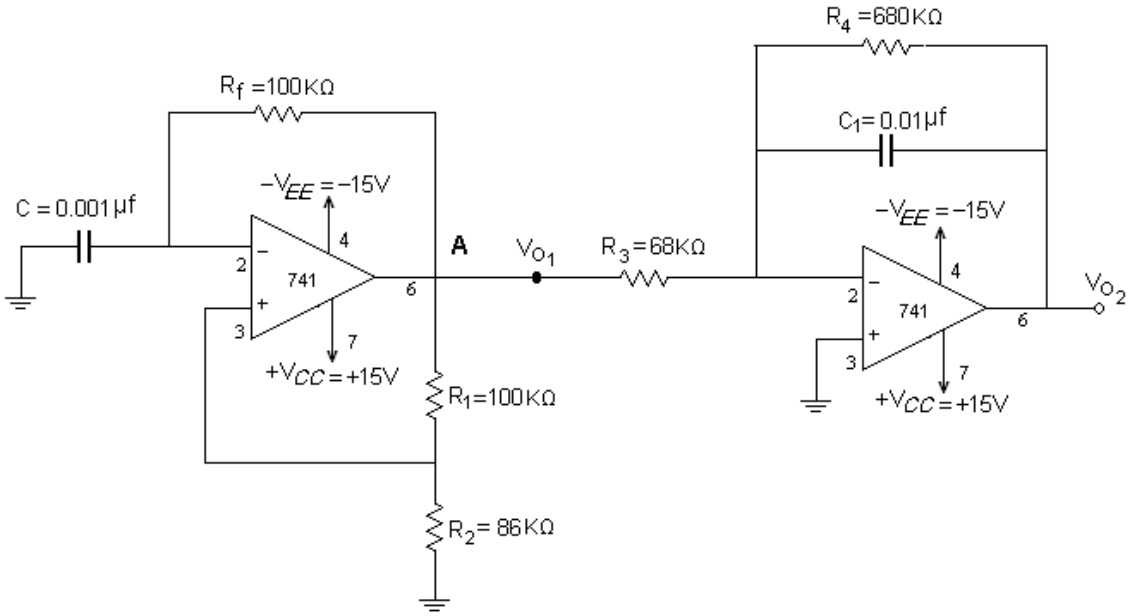


Fig1 Function Generator

Design:
Square wave Generator:

T= 2RfC ln (2R2 +R1/ R1)
Assume R1 = 1.16 R2
Then T= 2RfC

Assume C and find Rf
Assume R1 and find R2

Integrator:
Take R3 Cf >> T
R3 Cf = 10T
Assume Cf find R3
Take R3Cf = 10T
Assume Cf = 0.01μf
R3 = 10T/C
= 20K_

Procedure:
1. Connect the circuit as per the circuit diagram shown in Fig 1.
2. Obtain square wave at A and Triangular wave at Vo as shown in fig (a) and (b).
3. Draw the output waveforms as shown in fig (a) and (b).

Model Calculations:
For T= 2 m sec
T = 2 RfC
Assuming C= 0.1μf
Rf = 2.10-3/ 2.01.10-6
= 10 K_
Assuming R1 = 100 K
R2 = 86 K_

Sample readings:
Square Wave:
Vp-p = 26 V(p-p)
T = 1.8 msec
Triangular Wave:
Vp-p = 1.3 V
T= 1.8 msec

Wave Forms:

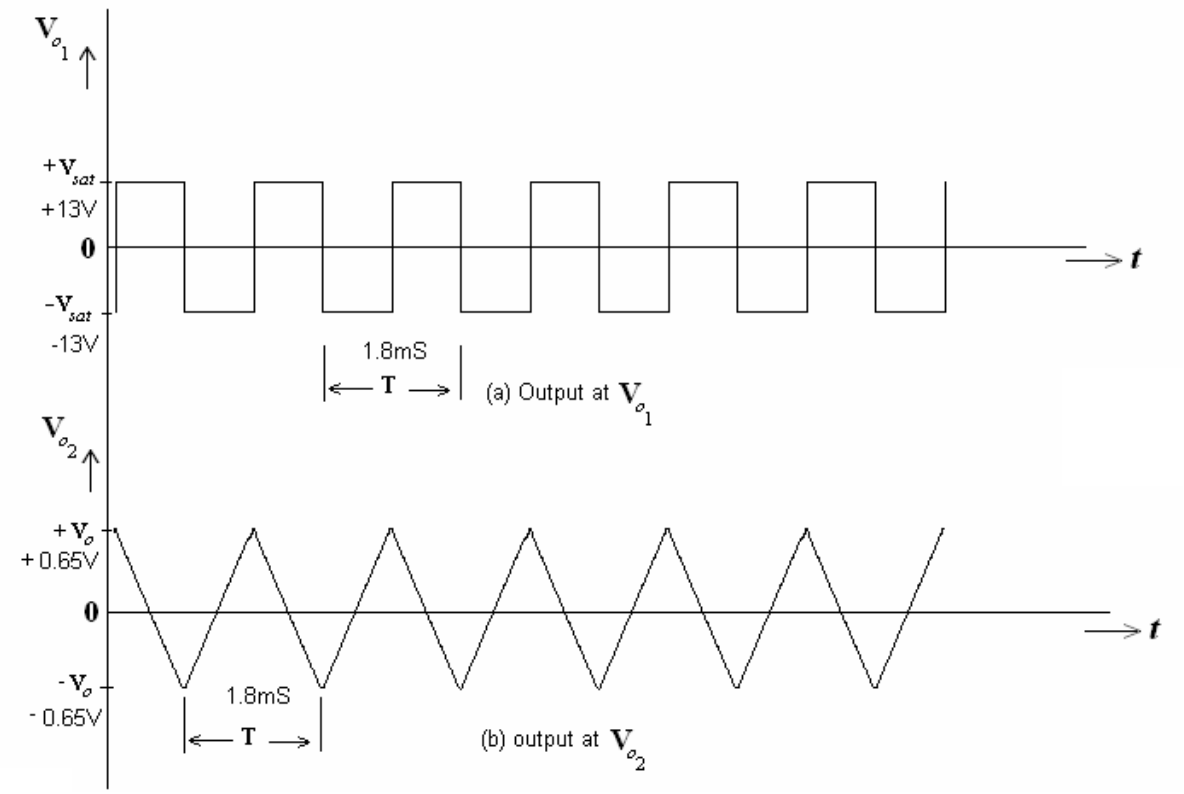


Fig (a): Output at 'A', Fig (b): Output

Precautions: Check the connections before giving the power supply.
Readings should be taken carefully.

Result: Square wave and triangular wave are generated and the output waveforms are observed.

8. IC 555 TIMER-MONOSTABLE OPERATION CIRCUIT

Aim: To generate a pulse using Monostable Multivibrator by using IC555

Apparatus required:

S. No	Equipment/Component name
1	555 IC Trainer kit
2	Function Generator
3	Cathode ray oscilloscope
4	Patch chords
5	CRO Cable

Theory:

A Monostable Multivibrator, often called a one-shot Multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or stand by mode the output of the circuit is approximately Zero or at logic-low level. When an external trigger pulse is obtained, the output is forced to go high ($\cong V_{CC}$). The time for which the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The Monostable circuit has only one stable state (output low), hence the name mono stable. Normally the output of the Monostable Multivibrator is low.

Circuit Diagram:

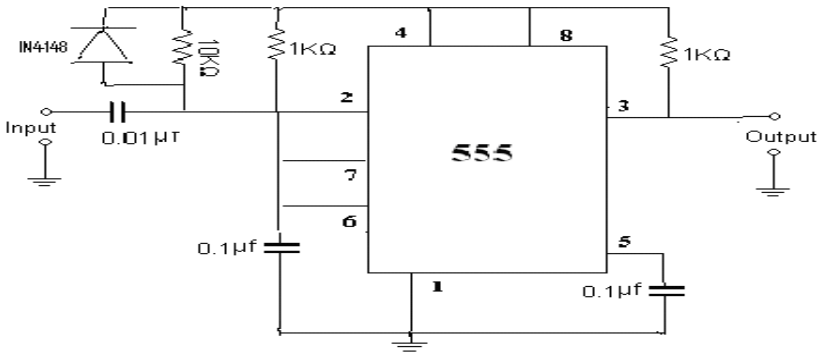


Fig1: Monostable Circuit using IC555

Design:

Consider V_{CC} = 12V, for given t_p

Output pulse width $t_p = 1.1\ R_A\ C$

Assume C in the order of microfarads & Find R_A

Typical values:

If C=0.1 µF , R_A = 10k then t_p = 1.1 mSec

Trigger Voltage =4 V

Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Apply Negative triggering pulses at pin 2 of frequency 1 KHz.
3. Observe the output waveform and measure the pulse duration.
4. Theoretically calculate the pulse duration as $T_{high}=1.1.\ R_AC$
5. Compare it with experimental values.

Waveforms:

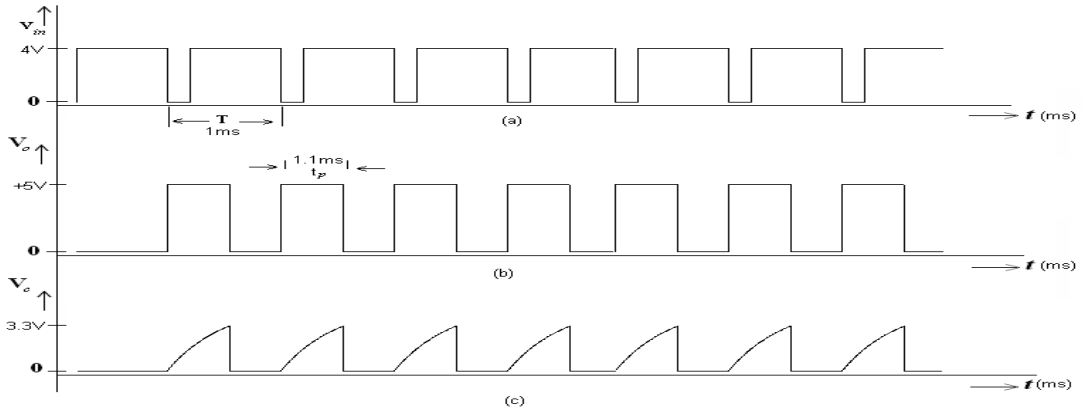


Fig 2 (a): Trigger signal, (b): Output Voltage, (c): Capacitor Voltage

Sample Readings:

Trigger	Output wave	Capacitor output
0 to 5V range 1)1V,0.09 msec	0 to 5V range 4.6V, 0.5 msec	

Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Result: The input and output waveforms of 555 timer mono stable Multi vibrator are observed as shown in Fig 2(a), (b), (c).

Inferences: Output pulse width depends only on external components R_A and C connected to IC555.

Questions & Answers:

1. Is the triggering given is edge type or level type? If it is edge type, trailing or raising edge?
   Ans: Edge type and it is trailing edge
2. What is the effect of amplitude and frequency of trigger on the output?
   Ans: Output varies proportionally.
3. How to achieve variation of output pulse width over fine and course ranges?
   Ans: One can achieve variation of output pulse width over fine and course ranges by varying capacitor and resistor values respectively.
4. What is the effect of Vcc on output?
   Ans: The amplitude of the output signal is directly proportional to Vcc
5. What is the ideal charging and discharging time constants (in terms of R and C) of capacitor voltage?
   Ans: Charging time constant T=1.1RC Sec
   Discharging time constant=0 Sec
6. What is the other name of mono stable Multi vibrator? Why?
   Ans: i) Gating circuit. It generates rectangular waveform at a definite time and thus could be used in gate parts of the system.

   ii) One shot circuit. The circuit will remain in a stable state until a trigger pulse is received. The circuit then changes states for a specified period, but then it returns to the original state.
7. What are the applications of mono stable Multi vibrator?
   Ans: Missing Pulse Detector, Frequency Divider, PWM, Linear Ramp Generator

9. SCHMITT TRIGGER CIRCUITS- USING IC 741

Aim: To design the Schmitt trigger circuit using IC 741.

Apparatus required:

S. No	Equipment/Component name
1	IC 741 Op-Amp
2	Function generator
3	Cathode Ray Oscilloscope
4	CRO Cable
5	Bread Board
6	Connecting Wires
7	R=1K(4),R=10K(1)

Theory:

The circuit shows an inverting comparator with positive feedback. This circuit converts arbitrary wave forms to a square wave or pulse. The circuit is known as the Schmitt trigger (or) squaring circuit. The input voltage V_{in} changes the state of the output V_o every time it exceeds certain voltage levels called the upper threshold voltage V_{ut} and lower threshold voltage V_{lt}.

When V_o= - V_{sat}, the voltage across R_1 is referred to as lower threshold voltage, V_{lt}. When V_o=+V_{sat}, the voltage across R_1 is referred to as upper threshold voltage V_{ut}.

The comparator with positive feed back is said to exhibit hysterisis, a dead band condition.

Circuit Diagrams:

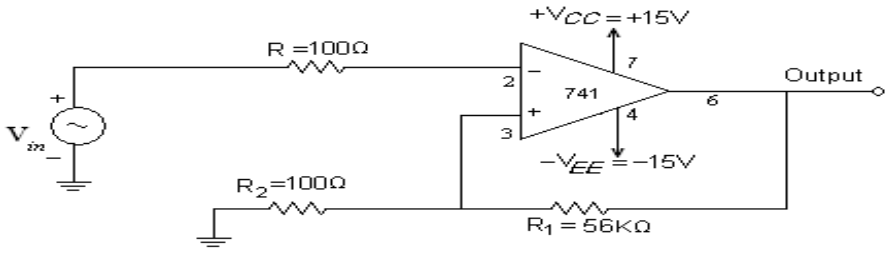


Fig 1: Schmitt trigger circuit using IC 741

Design:

$V_{utp} = [R_1/(R_1+R_2)](+V_{sat})$

$V_{ltp} = [R_1/(R_1+R_2)](-V_{sat})$

$V_{hy} = V_{utp} - V_{ltp}$

$=[R_1/(R_1+R_2)]\ [+V_{sat} - (-V_{sat})]$

Procedure:

1. Connect the circuit as shown in Fig 1 and Fig2.
2. Apply an arbitrary waveform (sine/triangular) of peak voltage greater than UTP to the input of a Schmitt trigger.
3. Observe the output at pin6 of the IC 741 Op-Amp Schmitt trigger circuit by varying the input and note down the readings as shown in Table 1 and Table 2
4. Find the upper and lower threshold voltages (V_{utp}, V_{Ltp}) from the output wave form.

Wave forms:

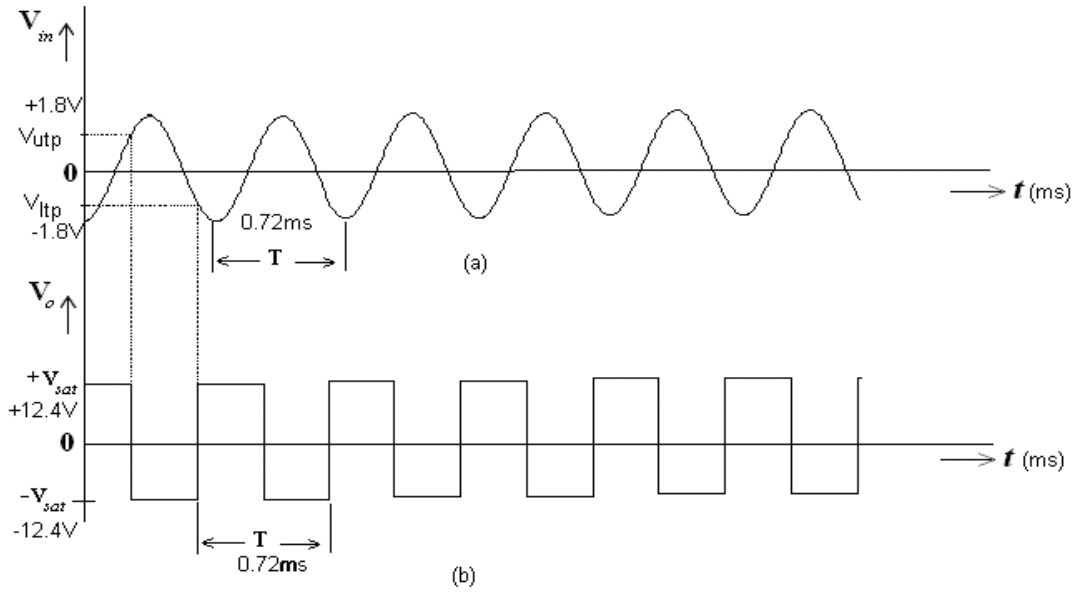


Fig 3: (a) Schmitt trigger input wave form (b) Schmitt trigger output wave form

Sample readings:

Table 1:

Parameter 741	**Input**		**Output**	
Voltage (Vp_{-p})	·			
Time period(ms)				

Table 2:

Parameter	**741**	**555**
V_{utp}		
V_{ltp}		

Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Results:

UTP and LTP of the Schmitt trigger are obtained by using IC 741 and IC 555 as shown in Table 2.

Inferences: Schmitt trigger produces square waveform from a given signal.

Questions & Answers:

1. What is the other name for Schmitt trigger circuit?
   Ans: Regenerative comparator
2. In Schmitt trigger which type of feedback is used?
   Ans: Positive feedback.
3. What is meant by hysteresis?
   Ans: The comparator with positive feedback is said to be exhibit hysteresis, a dead band condition. When the input of the comparator is exceeds V_{utp}, its output switches from + V_{sat} to - V_{sat} and reverts back to its original state,+ V_{sat} ,when the input goes below V_{ltp}
4. What are the effects of input signal amplitude and frequency on output?
   Ans: The input voltage triggers the output every time it exceeds certain voltage levels (UTP and LTP). Output signal frequency is same as input signal frequency.

10.PHASE LOCKED LOOP IC 565 APPLICATIONS

Aim: PLL as voltage-controlled oscillator.

Apparatus Required:

S.No	Equipment/Component Name
1	Bread board
2	IC565
3	PLL Trainer kit
4	CRO
5	CRO Cable
6	Function Generator
7	DC power supply
8	Patch chords

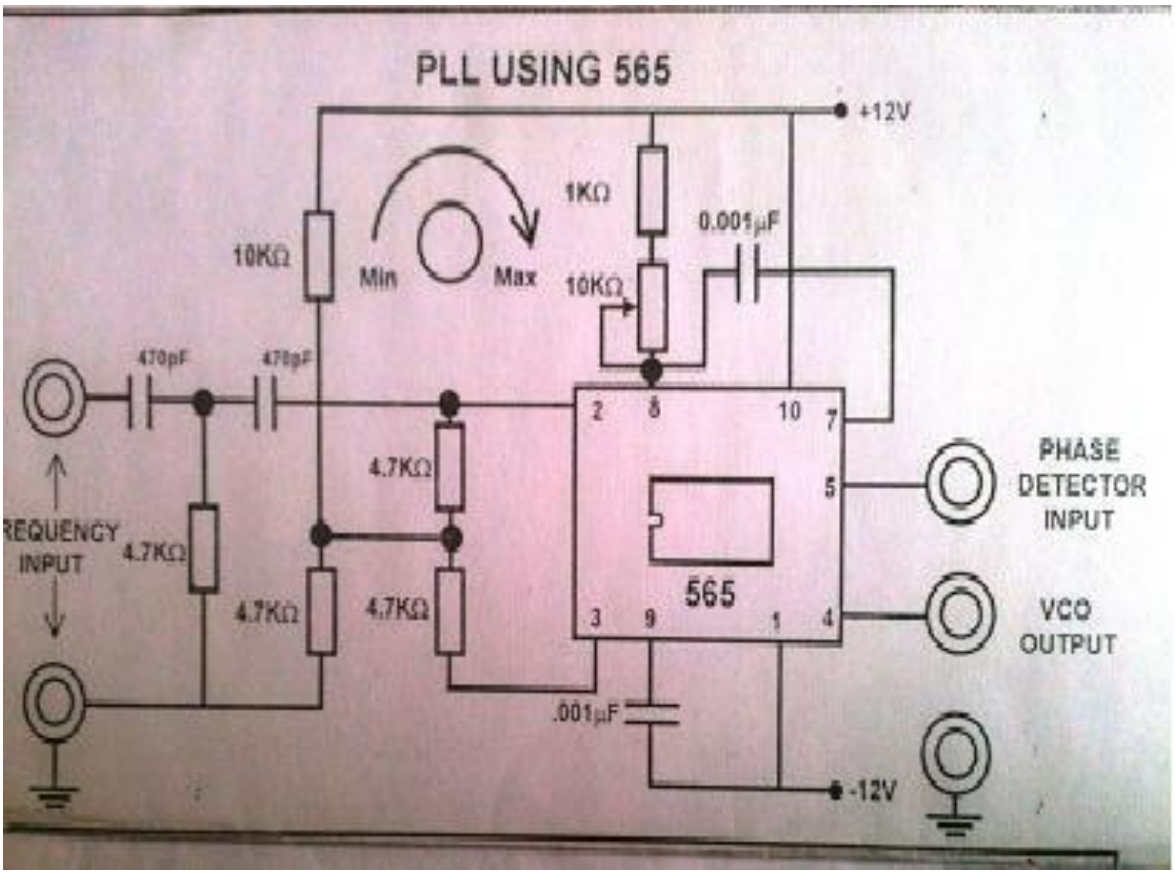
Theory:

The VCO generates an output frequency proportional to its input voltage. VCO often called as voltage to frequency converter. We often steer two types of outputs from VCO, one is square wave and the other is triangular wave. These VCOs are used in frequency modulation, tone generators, frequency shift keying, signal generators & function generators.

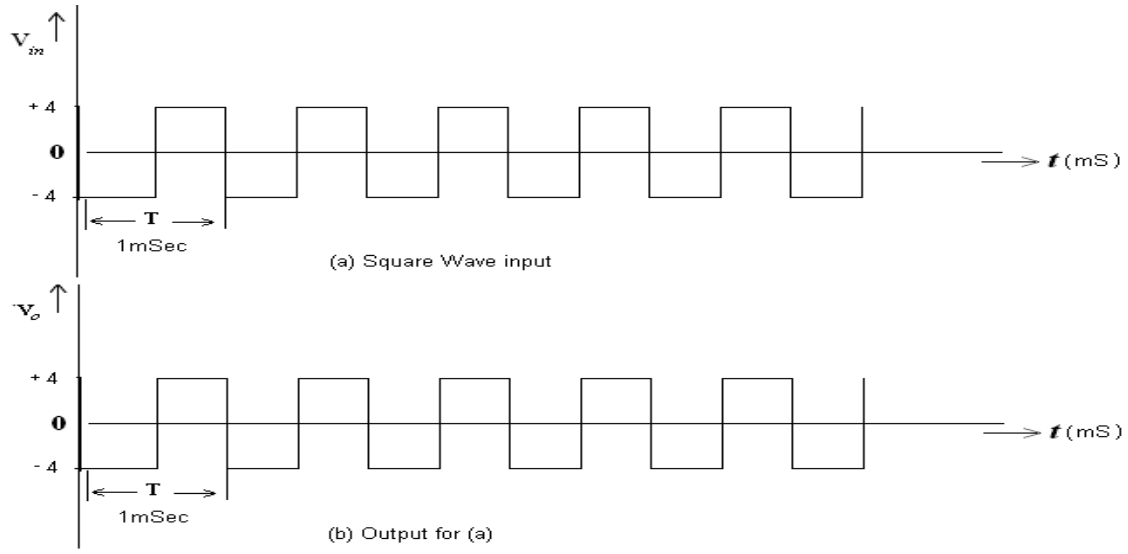
Refer to the VCO in the given figure. The frequency of operation is determined by external Resistor R1, Capacitor C1 and the voltage Vc is applied to the controlled terminal of pin-5.The triangular wave is generated by alternately charging the external capacitor C1 by one current source and then linearly discharging it by another. The discharge levels are determined by Schmitt trigger action. The Schmitt trigger also provides square wave output.

The typical amplitude of the triangular wave is 2.4V(P-P) and that of the square wave is 5.4V(P-P).

Circuit Diagram:



Experimented Observation:



Procedure:

1. Switch on the experimental board by connecting the power supply card to the mains.
2. Then check the VCO output at pin 4 of IC 565.
3. This is a square wave form the frequency of the waveform depends on CT(0.01µf) and Rs
4. Next short the pins 4&5 and give any signal of variable frequency and observe VCO output.
5. Change the input frequency and observe the VCO output on the CRO.
6. Between some frequencies the VCO output is locked to the input signal frequency this can be observed by increasing the frequency of the VCO out by changing input frequency.
7. Before or after that frequency range VCO output is not locked.
8. By changing the potentiometer provided on the board. Locking frequency range can be changed.

Result:

PLL are designed and output waveforms are observed.

11. VOLTAGE REGULATOR USING IC723, THREE TERMINAL VOLTAGE REGULATORS- 7805, 7809, 7912

Aim: To design a low voltage variable regulator of 2 to 7V using IC 723.

Apparatus required:

S. No	Equipment/Component name
1	IC 723
2	Resistors
3	DC Power Supply
4	Patch Chords
5	Voltmeter:0-25V, Ammeter: 0-50 namp

Theory:

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load current and input voltage variations. Using IC 723, we can design both low voltage and high voltage regulators with adjustable voltages.

For a low voltage regulator, the output V_O can be varied in the range of voltages $V_o < V_{ref}$, where as for high voltage regulator, it is $V_O > V_{ref}$. The voltage V_{ref} is generally about 7.5V. Although voltage regulators can be designed using Op-amps, it is quicker and easier to use IC voltage Regulators.

IC 723 is a general-purpose regulator and is a 14-pin IC with internal short circuit current limiting, thermal shutdown, current/voltage boosting etc. Furthermore, it is an adjustable voltage regulator which can be varied over both positive and negative voltage ranges. By simply varying the connections made externally, we can operate the IC in the required mode of operation. Typical performance parameters are line and load regulations which determine the precise characteristics of a regulator. The pin configuration and specifications are shown in Appendix-A.

Circuit Diagram:

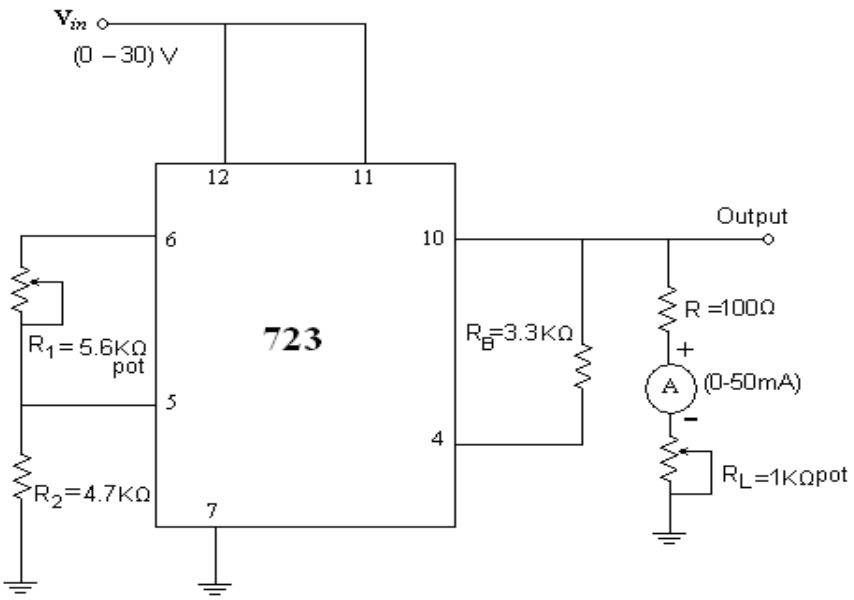


Fig1: Voltage Regulator

Design of Low voltage Regulator: -

Assume I_o= 1mA, VR=7.5V

R_B = 3.3 KΩ

For given V_o

$R_1 = (VR – V_O) / I_o$

$R_2 = V_O / I_o$

Procedure:

a) Line Regulation*:*

1. Connect the circuit as shown in Fig 1.
2. Obtain R_1 and R_2 for V_o=5V
3. By varying V_n from 2 to 10V, measure the output voltage V_o.
4. Draw the graph between V_n and V_o as shown in model graph (a)
5. Repeat the above steps for V_o=3V

b) Load Regulation*:* For V_o=5V

1. Set V_i such that V_O= 5 V
2. By varying R_L, measure I_L and V_o
3. Plot the graph between I_L and V_o as shown in model graph (b)
4. Repeat above steps 1 to 3 for V_O=3V.

Sample Readings:

a) Line Regulation:

V_o set to 5V

Vi(V)	Vo(V)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	

Vo set to 3V

Vi(V)	Vo(V)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	

b) Load Regulation:

Vo set to 5V

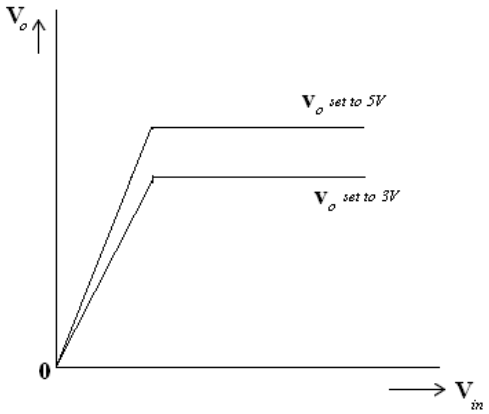
I_L (mA)	Vo(V)
46	
44	
40	
35	
28	
20	
18	
16	
12	
8	
6	
4	
2	

Vo set to 3V

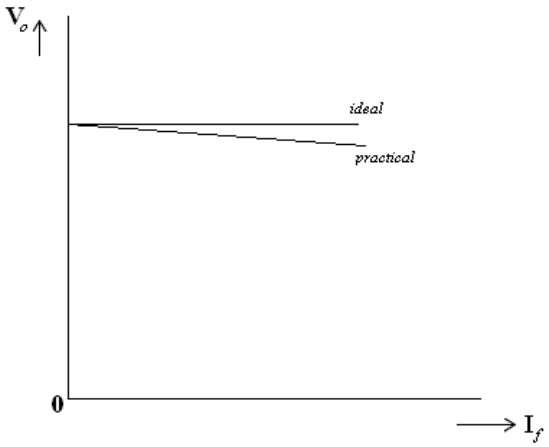
I_L (mA)	Vo(V)
24	
22	
20	
18	
16	
14	
12	
10	
8	
6	
4	
2	

Model graphs:

a) Line Regulation:



b) Load Regulation:



Precautions:

Check the connections before giving the power supply.
Readings should be taken carefully.

Results:

A low voltage variable Regulator of 2V to 7V using IC 723 is designed. Load and Line Regulation characteristics are plotted.

12. THREE TERMINAL VOLTAGE REGULATORS- 7805, 7809, 7912

Aim: To obtain the regulation characteristics of three terminal voltage regulators.

Apparatus required:

S. No	Equipment/Component Name
1	Bread board
2	IC7805
3	IC7809
4	IC7912
5	Multimeter
6	Milli ammeter
7	Regulated power supply
8	Connecting wires
9	Resistors pot

Theory:

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load current and input voltage. IC voltage regulators are versatile, relatively inexpensive and are available with features such as programmable output, current/voltage boosting, internal short circuit current limiting, thermal shunt down and floating operation for high voltage applications.

The 78XX series consists of three-terminal positive voltage regulators with seven voltage options. These ICs are designed as fixed voltage regulators and with adequate heat sinking can deliver output currents in excess of 1A.

The 79XX series of fixed output voltage regulators are complements to the 78XX series devices. These negative regulators are available in the same seven voltage options.

Typical performance parameters for voltage regulators are line regulation, load regulation, temperature stability and ripple rejection. The pin configurations and typical parameters at 25^0C are shown in Appendix-B.

Circuit Diagrams:

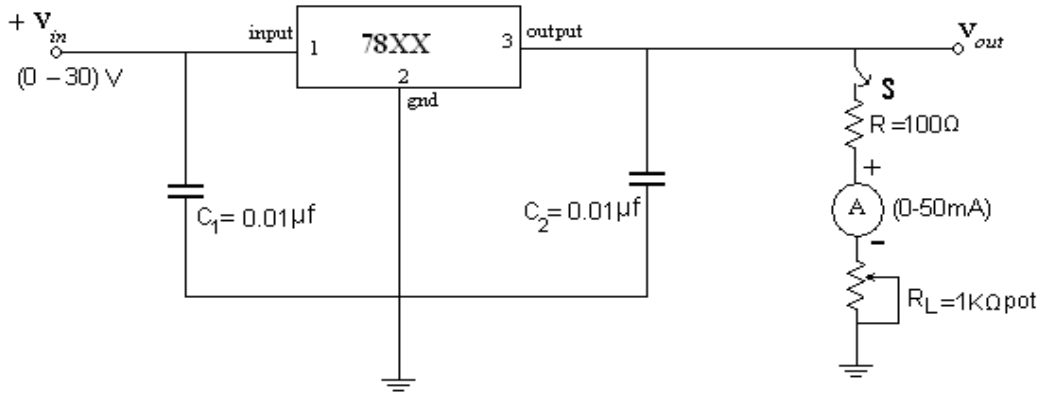


Fig 1: Positive Voltage Regulator

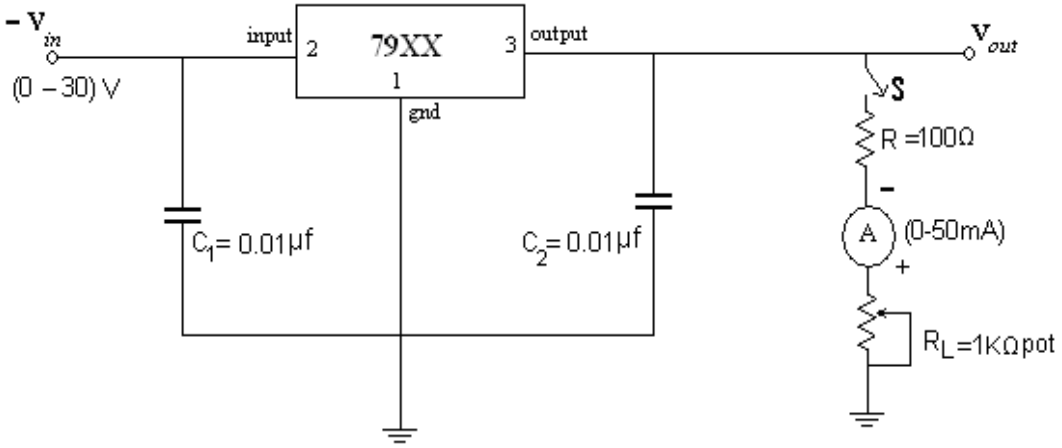


Fig 2: Negative Voltage Regulator

Procedure:

a) Line Regulation:

1. Connect the circuit as shown in Fig 1 by keeping S open for 7805.
2. Vary the dc input voltage from 0 to 10V in suitable stages and note down the output voltage in each case as shown in Table1 and plot the graph between input voltage and output voltage.
3. Repeat the above steps for negative voltage regulator as shown in Fig.2 for 7912 for an input of 0 to -15V.
4. Note down the dropout voltage whose typical value = 2V and line regulation typical value = 4mv for V_{in} =7V to 25V.

b) Load regulation:

1. Connect the circuit as shown in Fig 1 by keeping S closed for load regulation.
2. Now vary R_1 and measure current I_L and note down the output voltage V_o in each case as shown in Table 2 and plot the graph between current I_L and V_o.
3. Repeat the above steps as shown in Fig 2 by keeping switch S closed for negative voltage regulator 7912.

c) Output Resistance:

$$R_o = \frac{(V_{NL} - V_{FL})}{I_{FL}} \ \Omega$$

V_{NL} - load voltage with no load current

V_{FL} - load voltage with full load current

I_{FL} - full load current.

Sample readings:

a) Line regulation

1) IC 7805

Input Voltage V_i,(V)	Output Voltage V_o(V)
0	
5	
6	
7	
10	

b) Load Regulation

1) IC 7805

Load Current I_L(mA)	Output Voltage V_o(V)
44	
40	
30	
20	
16	
8	

2) IC 7809

Input Voltage V_i, (V)	Output Voltage V_o(V)
0	
5	
10	
12	
14	

2) IC 7809

Load Current I_L(mA)	Output Voltage V_o(V)
56	
48	
33	
25	
21	
15	

3)7912

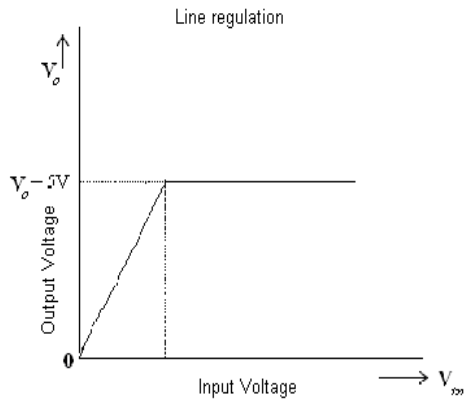
Input Voltage V_i, (V)	Output Voltage V_o(V)
0	
-10	
-12	
-14	
-15	

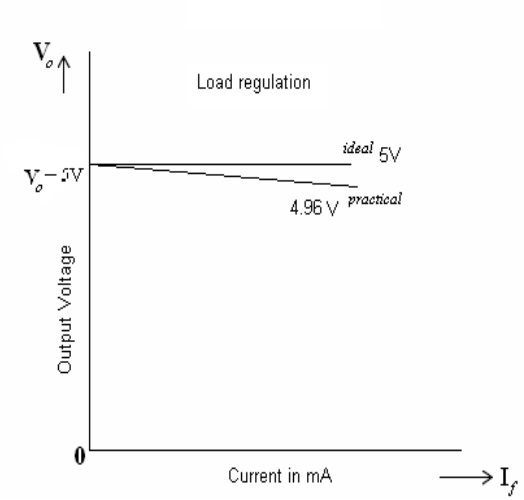
3) IC 7912

Load Current I_L(mA)	Output Voltage V_o(V)
56	
46	
38	
28	
24	
20	

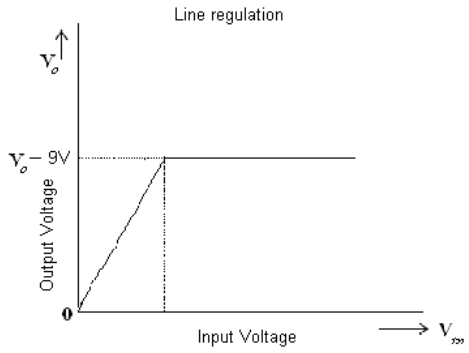
Graphs:

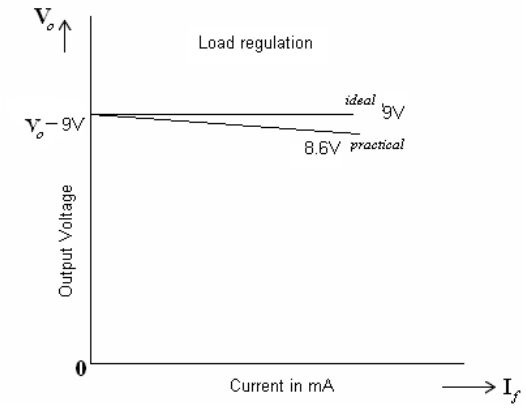
IC 7805



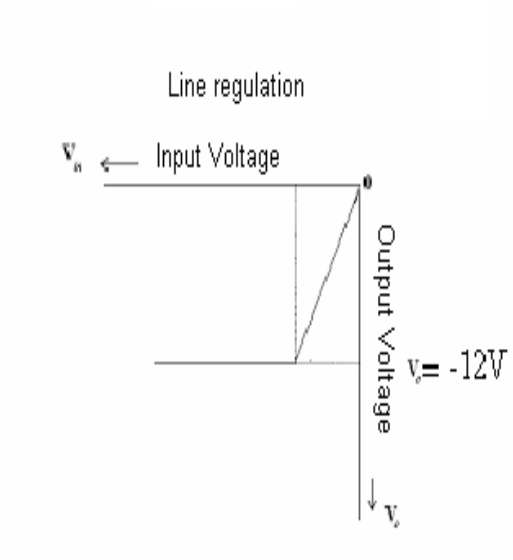


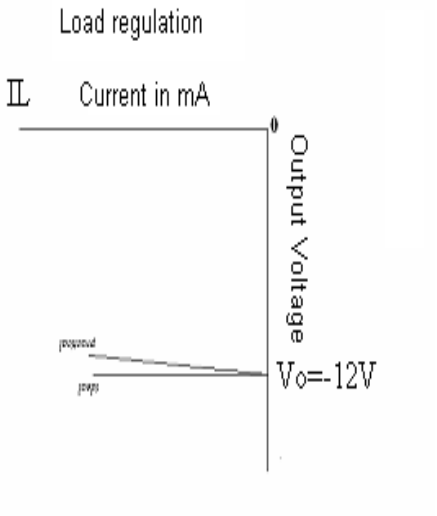
IC 7809





IC7912





$$\% \text{ load regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Result:

Line and load regulation characteristics of 7805, 7809 and 7912 are plotted

Inferences:

Line and load regulation characteristics of fixed positive and negative three terminal voltages are obtained. These voltage regulators are used in regulated power supplies.

Questions & Answers:

1. Mention the IC number for a negative fixed three terminal voltage regulator of 12V.
   Ans: IC 7912
2. Explain the significance of IC regulators in power supply
   Ans: To get constant dc voltages.
3. What is drop-out voltage?
   Ans: The difference between input and output voltages is called dropout voltage
4. What is the role of C_1 and C_2?

   Ans: C_1 is used to cancel the inductive effects.

   C_2 is used to improve the transient response of regulator.
4. What are C1 and C_2 called?
   Ans: Bypass capacitors

13. A/D AND D/A CONVERTERS.

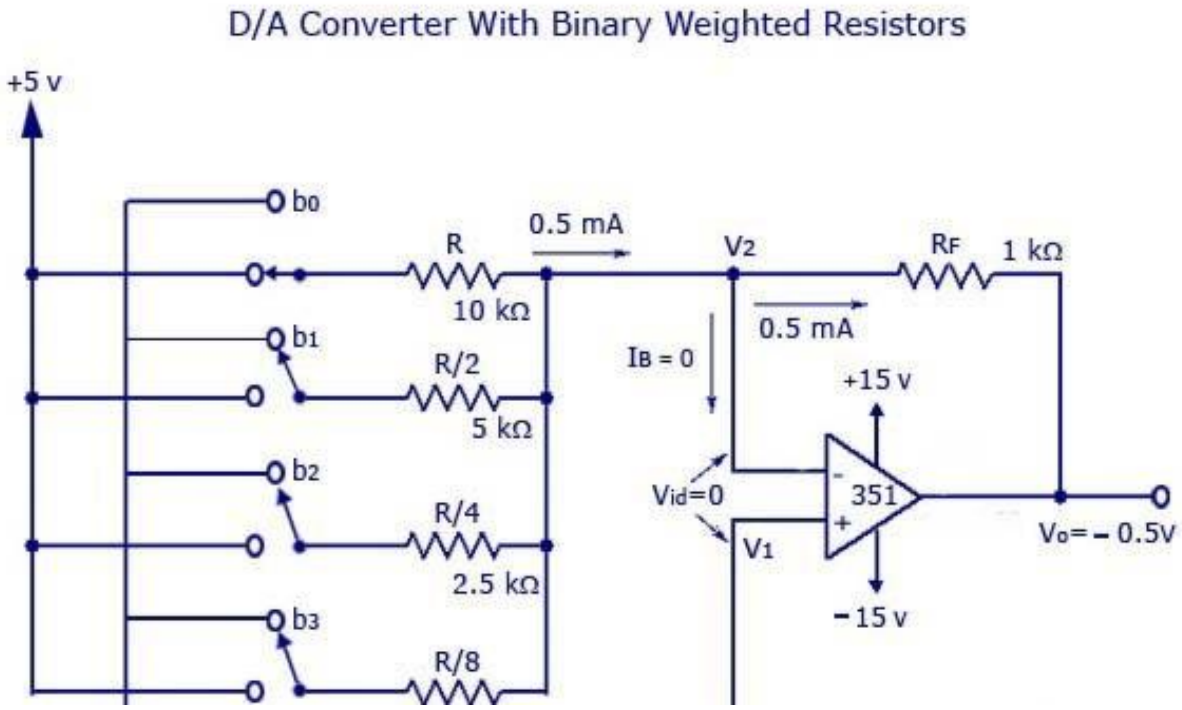
Aim: -To study a 4- bit R-2-R Ladder digital to analog converter.

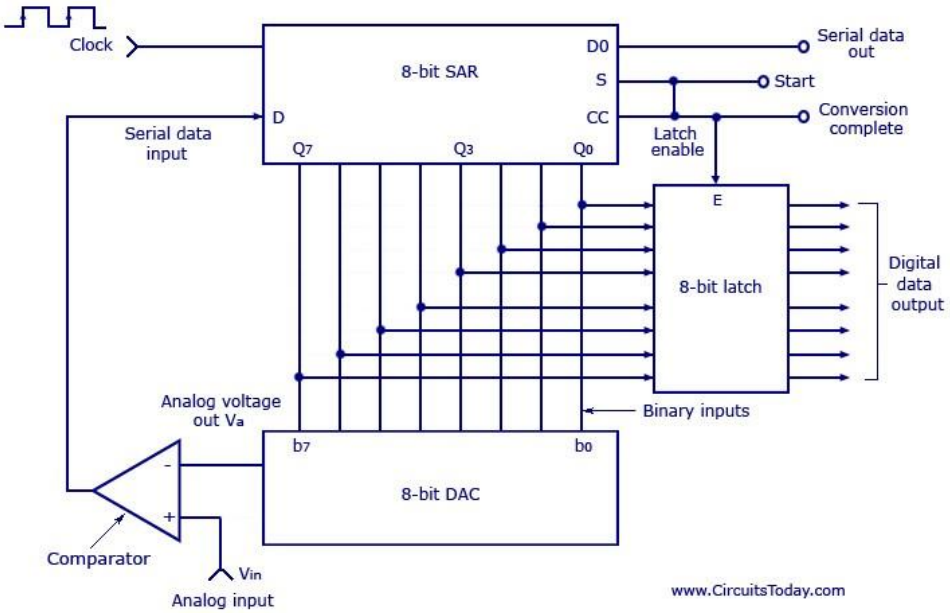
Apparatus required: -Experimental board on 8-bit R- 2R Digital to analog converter, digital voltmeter range 0-20 volt.

Theory-:

A circuit which can convert a binary number in to a corresponding voltage/current is called D to A converter(D/A or DAC).the input to a DAC will be a N-bit digital word and its output is an analog voltage or current. The various o/p in a DAC are in terms of a full- scale o/p voltage V0 (Fs) .the highest of 4-bit word is 1111and the number next to this is 10000.The o/p voltage corresponding to the LSB input(…….001) is V0 (LSB).similarly for MSB input (10000……..) it is Vo (MSB) and for max input (1111…….) it is vo (max) V0(LSB) = VO(Fs)/1 V0(MSB) = VO(Fs)/2 V (max)= V0(Fs)-V0(LSB) If V0 (Fs)= 10V V0(LSB)= 10/16= 0.625 Volt Vo(MSB)= 10/2= 5 volt V(max)= 10-0.625 =9.375 The methods of D to A conversion are based on generating current proportional to the positional value of a bit in the binary word. If the bit is high the current is allowed to flow and if the bit is low –then the current is dissolved.

Circuit Diagram-:





Successive Approximation Type Analog to Digital Converter

Procedure:

4- BIT R-2R DIGITAL-TO-ANALOG CONVERTOR: - 1. Switch on the supply and adjust the VREF= 10volt. 2. Connect VREF to T5 and digital voltmeter 0—20, volt between T5 –T6. 3.4-bit R-2R network with VREF=10 volt. 4. Now measure the voltage for each binary from 0000 to 1111 and verify the eqs.(1) to (3). You will find that the voltage 0.625 volt is added for each next binary digit. 5. Find out V0(LSB), V0(MSB) and V (max) theoretically and compare the results obtained practically. 6. Plot the observations for each binary no.and compare it with fig. and set any other value of VREF (say 10.24 volt) and repeat steps.

Observation: -

Digital Input	Analog Output(Volt)

Result-: Studied the 4-bit R-2R Ladder digital to analog converter.

Precautions-:

(1). Switch off the power supply when not in use.

(2) All the connections should be right and tight.

(3) Reading Should be taken carefully by pressing the right key corresponding to specific binary number.

Analog to Digital Conversion

AIM-: To study the process of 4-bit analog to digital conversion by counter method.

Apparatus Required-:

A/D Converter kit, connecting wires. THEORY-: A/D Comparator are the power inter phase b/w digital and analog words ADC in values transition of analog information in to equivalent digital information(word), there are so many connection techniques in given band counter method is adopted. The band layout designed is blocks verify the whole process which is described as follows. (A)Comparator-: Its basic function is to compare I/p analog voltage in) with the binary ladder o/p voltage (reference) o/p signal to reset the gate flip-flop. (B)Flip-flop_-: It is an RS flip-flop which is called gate flip-flop. Its instruction is to make count gate enables and disable, where it is set applying start signal. Its o/p goes logic 1 which allows count gate to pass I/P clock signal to the up counter. (C)Up counter-: It is a 4- bit counter the o/p of which is a digital equivalent of analog I/P initiated by start pluse. (D)Binary ladder and switched-: There is the scent of 4- bit digital to analog converter. the up-counter signal switch guard analog switches b/w applied reference and ground which produce the resultant o o/p is the form of reference o/p to the comparator. (E)Start and set mono- flops-: There are set of two mono – flops used to set the count gate flip-flop and to reset the counter.

Procedure Analog to Digital Convertor-:

1. Connect the given voltmeter across the analog voltage sockets and adjust input voltage to 1.00 volt with the given knob situated just under the voltmeter note the comparator status LED comes on disconnect the voltmeter from the analog input sockets and connect it with the ref –in socket

. 2. Apply a brief push on start key. it will start the conversion which is indicated by another two LEDs fitted with the gate. Input and output.

3. Note the data output LEDs fitted at the top of the board. Also check the change of voltage in analog meter.

Observation Table-:

Analog Input(Volt)	Reference Voltage (Volt)	Digital Output

Result-: Studied the 4-bit analog to digital converter is verified.

Precautions -: (1). Switch off the power supply when not in use.

(2). All the connections should be right and tight.

(3) Reading Should be taken carefully.

VIVA QUESTIONS

1. List the broad classification of ADCs?

2. List out some integrating type converters.

3. What are the main advantages of integrating type ADCs?

4. Define conversion time? 5. Define resolution of a data converter?

Inferences:

Variable voltage regulators can be designed by using IC 723.

Questions & Answers:

1. What is the effect of R_1 on the output voltage?

   Ans: R_1 decreases for an increase in the output voltage.

2. What are the applications of voltage regulators?

   Ans: Voltage regulators are used as control circuits in PWM, series type switch mode supplies, regulated power supplies, voltage stabilizers.

3. What is the effect of V_i on output?

   Ans: Output varies linearly with input voltage up to some value (o/p voltage+ dropout voltage) and remains constant.