J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

(UGC AUTONOMOUS)

Accredited by NAAC, Approved by AICTE & Permanently affiliated to JNTUH

Three Day Workshop on "Design Approaches for Front End VLSI Design"

(9th-11th Sept 2019)

Resource Person

Dr. Md. Salauddin,

Assoc. Professor, ECE Dept.

JBIET, Hyd.

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

(UGC Autonomous)

Yenkapally(V), Moinabad(M), P.O. Himayat Naagar, R.R. District, Hyderabad-500075

Phone No: 08413-235127, 235053, Fax: 08413-235753

REPORT ON THREE DAY WORKSHOP

"DESIGN APPROACHES FOR FRONT END VLSI DESIGN"

on

9th-11th September 2019

Vision of Institute:

To be a centre of excellence in engineering education, research and application of knowledge to benefit society with ethical values.

Mission of Institute:

1. To provide world class engineering education, encourage research and development.

2. To evolve innovative applications of technology and develop entrepreneurship.

3. To mould the students into socially responsible and capable leaders.

VISION

To be a guiding force enabling multifarious applications in Electronics and Communications Engineering, promote innovative research in the latest technologies to meet societal needs

MISSION

- To provide and strengthen core competencies among the students through expert training and industry interaction.
- To promote advanced designing and modeling skills to sustain technical development and lifelong learning in ECE.
- To promote social responsibility and ethical values, within and outside the department.

ABOUT THE DEPARTMENT:

The Department of Electronics and Communication Engineering was established in the year 1998 with an intake of 60 in B.Tech. The intake was increased to 90 in the year 2000 and 120 in the year 2004. The M. Tech program in VLSI System Design was introduced in 2005 with an intake of 18 and it was raised to 24 in 2014. The B.Tech. Program was accredited by NBA in 2006. The Department of ECE is best known for its talented and dedicated professionals renowned for their excellence in various specializations in the field of Electronics & Communication Engineering. The faculties have completed two consultancy research projects and one more project is ongoing. 6 faculties have patents including National and Australian Govt. whereas, there are more than 50 research articles published in peer reviewed Journal and Conferences for the last 3 years. ECE has also received AICTE grand under MODROB.

The Department is provided with state of the art technological tools incorporated in all the existing laboratories. For the last ten years, the students of ECE, who walked out of the portals of the institute successfully, holding their degrees, were immediately inducted into the MNCs of high reputation in India & abroad.

ABOUT THE WORKSHOP:

VLSI industry or exposure can be classified in two parts distinctively which are Front End and Backend. This paper mainly deals in FrontEnd part for Design Verification Methodology which will give Basic understanding of Universal System Verilog Architecture which can be used for any Design Verification. Before going to VLSI concepts we need to understand the difference in Hardware and Software languages which will in turn answer why HDL is for Designing and Verification. HDL have options such as VHDL, Verilog, System Verilog etc. where Verilog is preferred for writing Top module Design whereas System Verilog is used for other Testing Blocks. The base of Front End depends on HDL, which leads to one simple question in every mind why we can't use Software languages for writing codes for Hardware Design & its Verification. The answer to that question is very simple is that Software Languages does not have the concept of Time Constraint thus make it inappropriate to be used in place on HDL. HDL has many options to choose from namely VHDL, Verilog, System Verilog etc. Most of times a coder prefer Verilog over VHDL mainly because of improvement as well as Verilog feels easy for learning and grasping the basic contents which is required for coding. SV is preferred for writing codes for blocks required in Verification and Testing whereas Verilog is used for writing code for Top module Design. Firstly lets understand the basic role play of each i.e. Front – End & BackEnd in VLSI domain.

Banner:

JB INSTITUTE OF ENGINEERING & TECHNOLOGY

UGC Autonomous

Accredited by NAAC, Approved by AICTE & Permanently Affiliated to JNTUH

THREE DAY WORKSHOP ON

DESIGN APPROACHES FOR FRONT END VLSI DESIGN

By

Dr. Md. Salauddin

Assoc. Prof-ECE Dept, JBIET.

Venue: MNR Auditorium

Date: 9th-11th September 2019

Schedule:

DAY1:

- Introduction to VLSI based Embedded systems
- Introduction to Logic Families
- VLSI Design Flow
- Hardware Modeling Overview,
- HDL language concepts
- Modules and Ports
- Dataflow Modeling

- Introduction to Test benches
- Operators
- Procedural Statements
- Controlled Operation Statements

DAY 2:

- Coding for Finite State Machines
- Coding For Synthesis
- FPGA Architecture
- Basic Components of FPGA (LUT,CLB, Switch Matrix, IOB)
- FPGA Architecture of different families: 7series and UltraScale devices.
- FPGA Design Flow – Xilinx Vivado tool Flow,

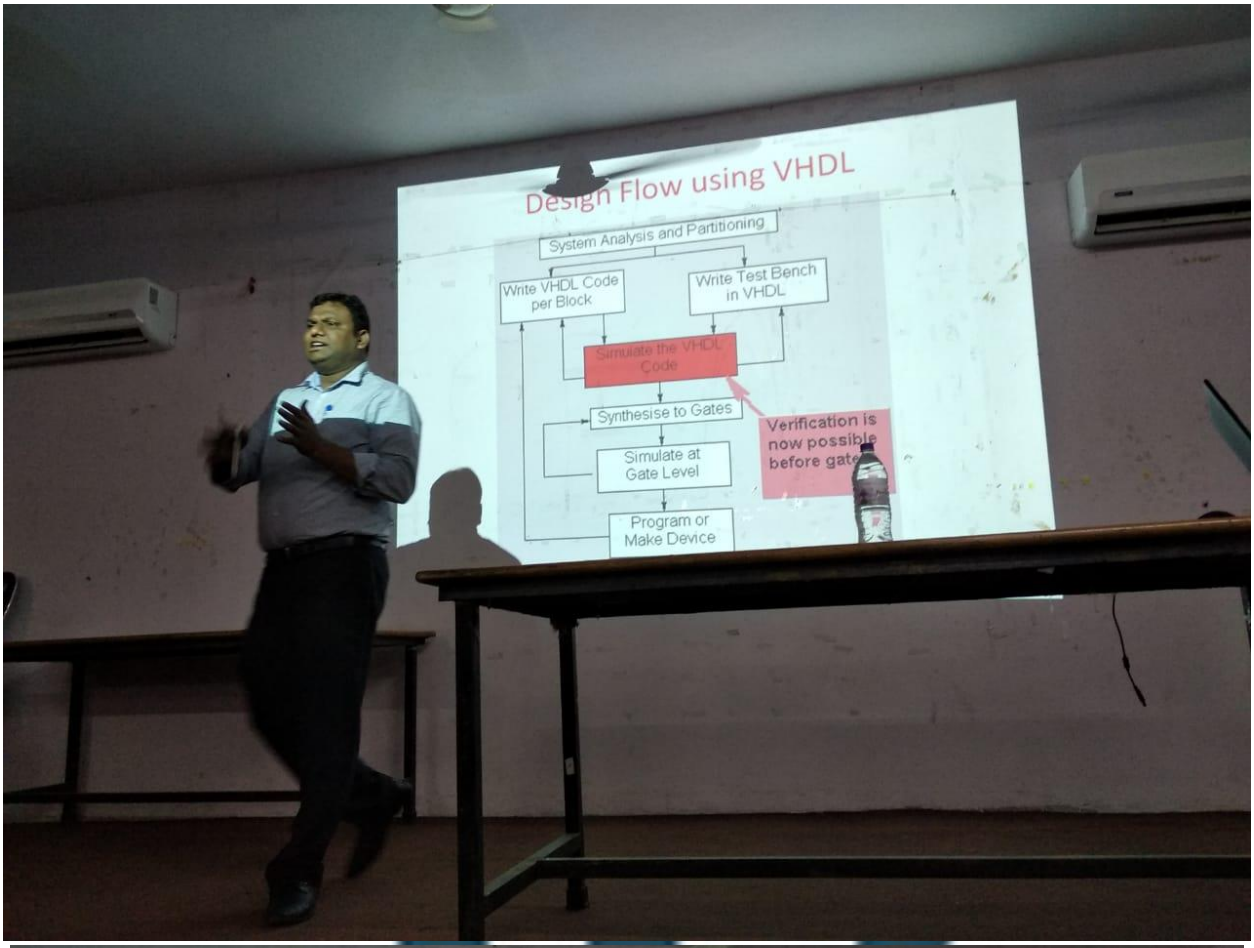
DAY 3:

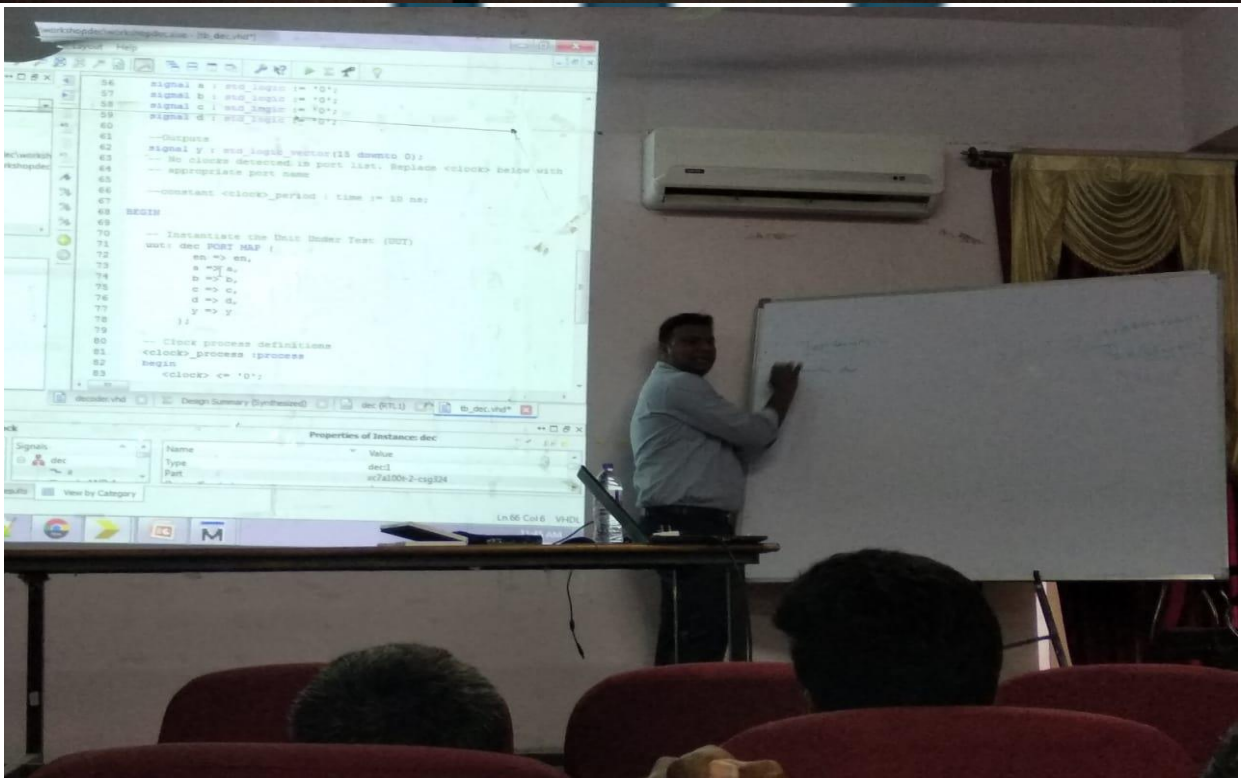
- Reading Reports, Implementing IP cores, Debugging Using Vivado Analyzer.
- Optimal FPGA Design HDL
- Coding Techniques for FPGA, FPGA Design Techniques, Synthesis
- Techniques, Implementation Options.

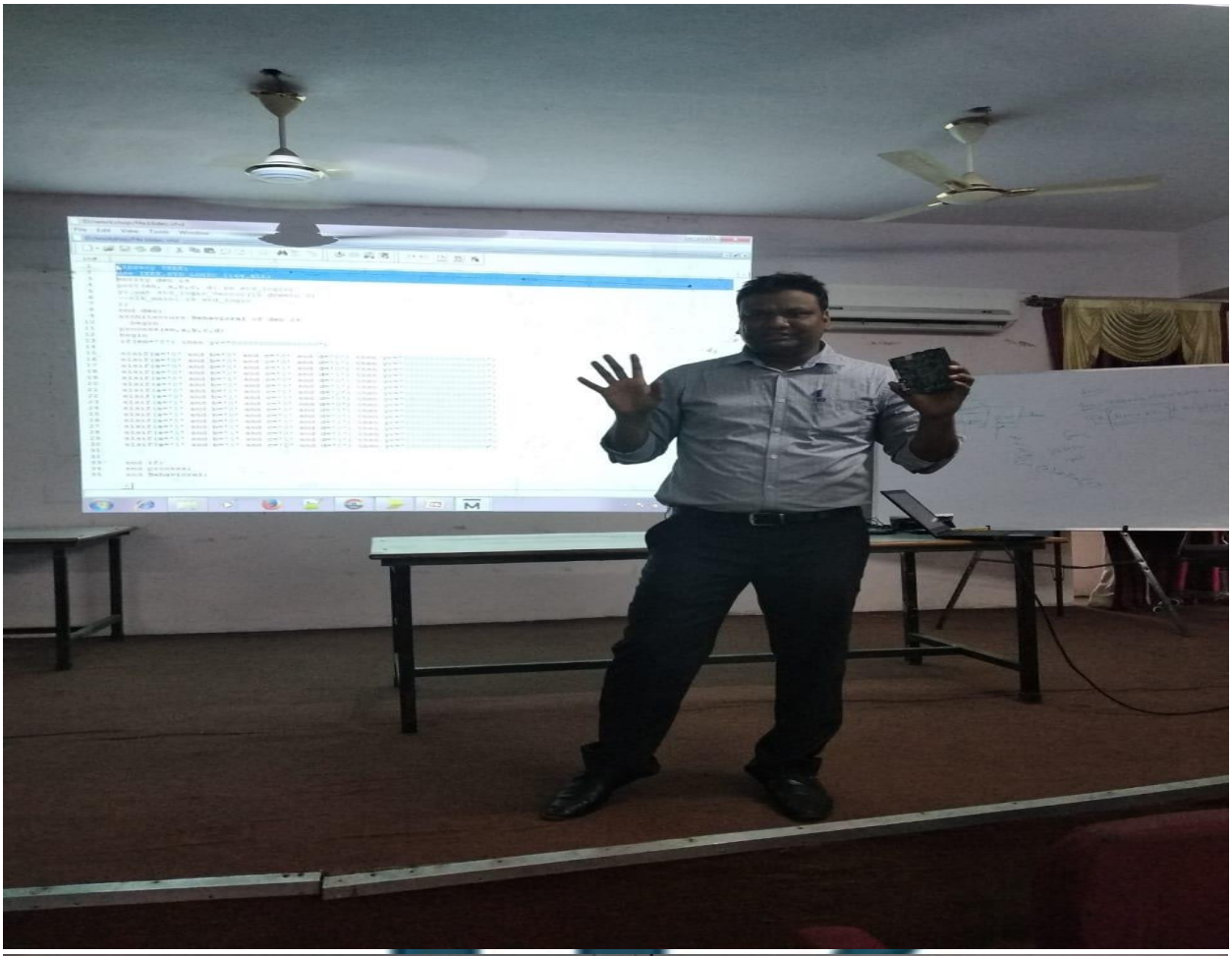
J.B. Institute of Engineering and Technology (JBIET) organized a three day workshop on **"DESIGN APPROACHES FOR FRONT END VLSI DESIGN "on** 9th- 11th September 2019 at MNR Auditorium, ECE Department, JBIET. The workshop focused on Front end VLSI design using FPGAs. The programme started at 10:00 am on 9th Sept.2019 with the welcome address by the principal Dr. Niraj Upadhayaya. The dignitaries on the dias were Prof. Dr. Niraj Upadhayaya, Principal-JBIET, Dr. Towheed Sulthana, HOD-ECE, Dr. Durai Pandy, Dean Academics.

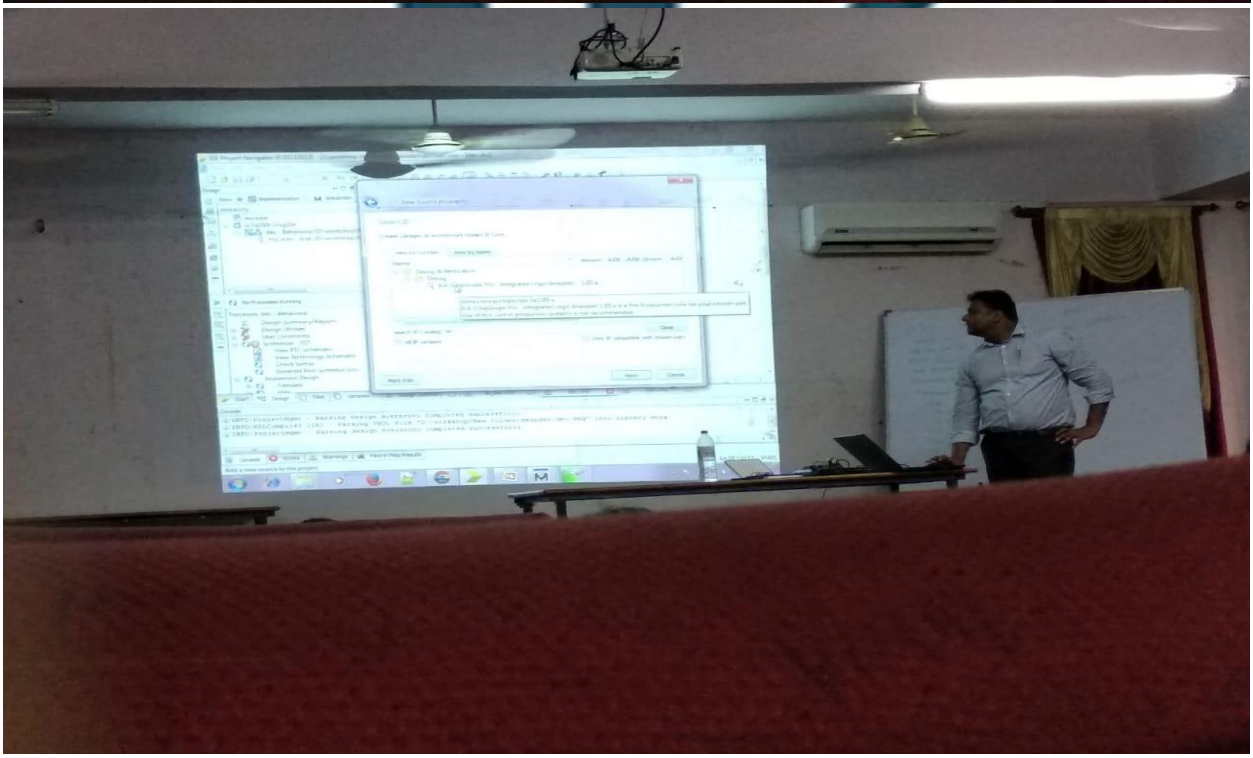
Dr. Towheed Sulthana, giving the opening remarks for the workshop

Opening remarks and introduction of the programme was given by **Dr. Niraj Upadhayaya, Principal.** He highlighted the applications of VLSI and importance of FPGA in the real time and the requirement of large scale production of nanomaterials. He mentioned that a large scale production of advanced digital devices is possible at our country. He emphasized the need of taking the laboratory level experiments to the real problems. Head of the Department , **Dr. Towheed Sulthana**, Dean Academics- Dr. Duraipandy have also congratulated for conducting 3-days hands on workshop on VLSI which will be very useful to their career. Also, they had deliberated the importance of Outcome Based Education and outcome of OBE. All Interested faculty and students were invited in workshop.


Design Flow using VHDL
System Analysis and Partitioning
Write VHDL Code per Block
Write Test Bench in VHDL
Simulate the VHDL Code
Synthesise to Gates
Verification is now possible before gate
Simulate at Gate Level
Program or Make Device







JB Institute of Engineering and Technology

(Autonomous)

Department of Electronics and communication Engineering

Three day workshop on Design Approaches for Front End VLSI Design

Student Feedback

Instructor: Dr.MD. SALAUDDIN Date: 07-07-2018

INSTRUCTIONAL

		Strongly Agree	Agree	Disagree	Strongly Disagree	NIA
a)	The instructor was knowledgeable about this subject_____					
b)	The instructor managed students participation well_____					
c)	The instructor explained concepts well._____					
d)	The instructor encouraged questions and was responsive to them._____					
e)	The instructor provided feedback and clarification during practice sessions._____					
f)	The instructor made my overall experience a positive one.___					
g)	The instructor advised me of the next class(es) that I should take._____					
h)	The instructor recommended the self-paced offering that Compliments this class._____					
i)	The Instructor gave ideas for further Mini/ Major Projects___					

PRACTICE ENVIRONMENT

		Strongly Agree	Agree	Disagree	Strongly Disagree	NIA
a)	The practice environment was set up in a satisfactory way_____					
b)	The performance of the software, hardware and network was satisfactory_____					
c)	Technical problems were resolved satisfactorily_____					

ABOUT STUDENT

Name_____

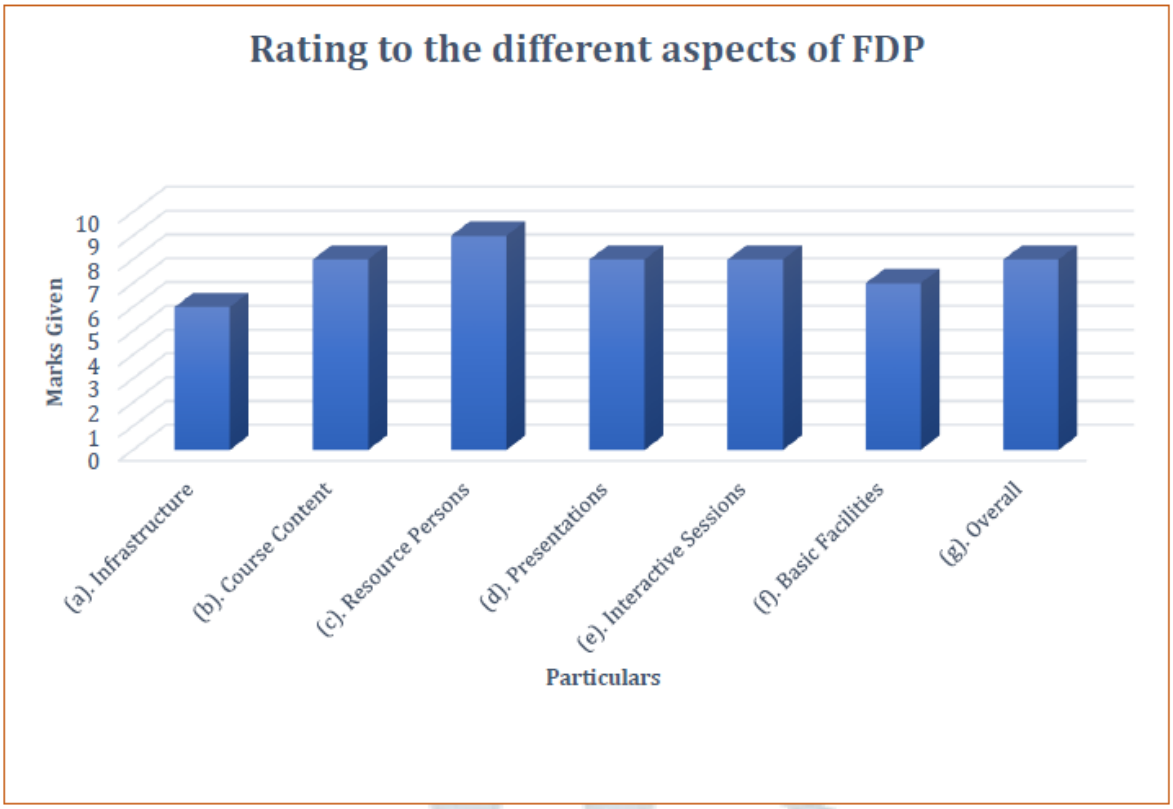
College_____

E-Mail ID_____

Address_____

Phone Number_____

FEEDBACK ANALYSIS:



THANK YOU