J.B. INSTITUTE OF ENGINEERING & TECHNOLOGY

UGC Autonomous
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Dept. of Electronics & Communication Engineering

Analog Circuits Lab Manual

II B.Tech I Semester
(2023-24)

J B Institute of Engineering & Technology

B. Tech Electronics & Communication Engineering

INSTITUTION VISION

To be a centre of excellence in engineering and management education, research and application of knowledge to benefit society with blend of ethical values and global perception.

INSTITUTION MISSION

1. To provide world class engineering education, encourage research and development.
2. To evolve innovative applications of technology and develop entrepreneurship.
3. To mould the students into socially responsible and capable leaders.

DEPARTMENT VISION

To be a guiding force enabling multifarious applications in Electronics and Communications Engineering, promote innovative research in the latest technologies to meet societal needs.

DEPARTMENT MISSION

1. To provide and strengthen core competencies among the students through expert training and industry interaction.
2. To promote advanced designing and modeling skills to sustain technical development and lifelong learning in ECE.
3. To promote social responsibility and ethical values, within and outside the department.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

1. Practice Technical skills widely in industrial, societal and real time applications.
2. Engage in the pursuit of higher education, delve into extensive research and development endeavours, and explore creative and innovative ventures in the domains of science, engineering, technology.
3. Exhibit professional ethics and moral values and capability of working with professional skills to contribute towards the need of industry and society.

PROGRAM OUTCOMES (POs) &PROGRAM SPECIFIC OUTCOMES (PSOs)

PO	Description
PO 1	**Engineering Knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	**Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	**Design / development of Solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	**Conduct investigations of complex problems:** Use research based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO 6	**The engineer and Society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO 8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
PO 9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO 10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO 11	**Project management and finance:** Demonstrate knowledge andunderstanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	**Lifelong learning:** Recognize the need for, and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological Change
Program Specific Outcomes	
PSO1	Carry out the Analysis and Design different Analog & Digital circuits withgiven specifications.
PSO2	Construct and test different communication systems for various applications.

AY: 202223 Onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	B. Tech ECE II YearI Sem			
Course Code: **L2142**	**Analog Circuit Laboratory (ECE)**	L	T	P	D
Credits: **1.5**		**0**	**3**	**0**	**0**

PreRequisites: NIL

Minimum Twelve experiments to be conducted:

List of Experiments:

1. Common Emitter Amplifier
2. Common Collector Amplifier
3. Two Stage RC Coupled Amplifier
4. Current Series and Voltage Shunt Feedback Amplifier
5. RC Phase Shift, Wien Bridge Oscillator using Transistors
6. Hartley and Colpitt's Oscillator
7. Class B Complementary Symmetry Amplifier
8. Class A Power Amplifier (Transformer less)
9. Bistable Multi-vibrator.
10. Monostable Multi-vibrator.
11. Astable Multi-vibrator.
12. Schmitt Trigger.
13. Bootstrap Sweep Circuit

Equipments required for Laboratories:

For Hardware design of Electronic Circuits

- RPS
- CRO
- Function Generators
- Multimeters
- Operating Systems Windows XP.
- Simulation Software (Multisim/Tinaroo) Package.

Course Outcomes:

- The student will be able to:

1. Analyze different types of Multistage Amplifiers.
2. Determine performance of Positive and Negative Feedback Amplifiers.
3. Evaluate efficiency of Different Power Amplifiers.
4. Analyze the various Multi-vibrators.
5. Develop the applications using Timebase generators.

COPO/PSO Mapping

Course Outcomes	Program Outcomes(POs)/Program Specific Outcomes(PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2				2								
CO2	3	2										2	3	2
CO3	2	2											2	2
CO4	2	2												
CO5		2											1	2
Average	1.8	2											1.2	1.2

1.Common Emitter Amplifier

Aim

1. To design a small signal voltage amplifier and measure the voltage gain.
2. To plot its frequency response and to obtain bandwidth.

Apparatus

I. NPN Bipolar Junction Transistor (BJT)

II. Resistors (as per design requirements)

III. Capacitors (as per design requirements)

IV. Signal Generator

V. Oscilloscope

VI. Breadboard and Connecting Wires

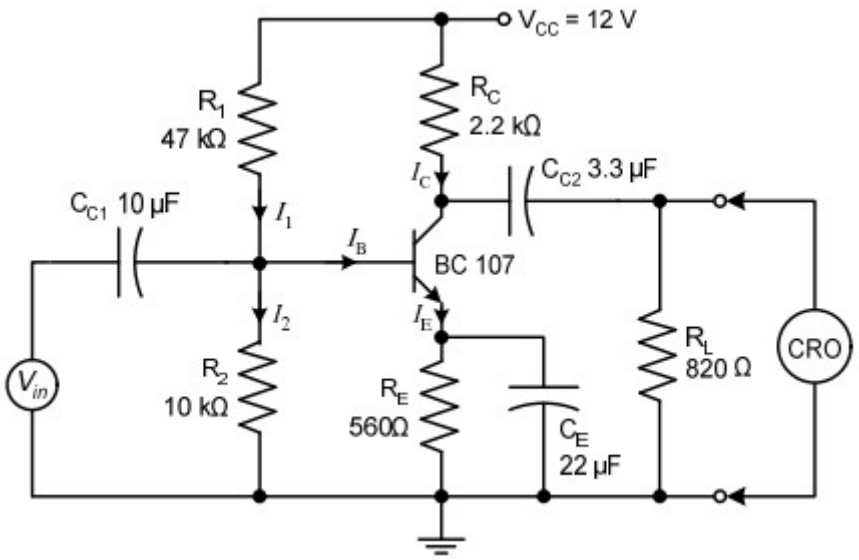
Theory

Amplifiers are classified as small signal amplifiers and large signal amplifiers depending on the shift in operating point, from the quiescent condition caused bythe input signal. If the shift is small, amplifiers are referred to as small signal amplifiers and if the shift is large, they are known as large signal amplifiers. In small signal amplifiers, voltage swing and current swing are small. Large signal amplifiers have large voltage swing and current swing and the signal power handled by such amplifiers remain large.

Voltage amplifiers come under small signal amplifiers. Power amplifiers are one in which the output power of the signal is increased. They are called large signalamplifiers. Figure shows the circuit diagram of a common emitter amplifier

Design

Design a common emitter amplifier with V_{CC}=12*Volt*, V_{CE}=6 Volt and $V_{RE} = 10\%\,\text{of}\,V_{CC}$ using the transistor BC 107. Assume for a frequency range of 500 Hz to 200 KHz.



Let's design a Common Emitter Amplifier with Voltage Divider Biasing using the BC107 transistor.

Given Parameters:

$V_{CC} = 12\ V$

$V_{CE} = 6\ V$

$V_{RE} = 10\%\ of\ V_{CC} = 1.2\ V$ (since V_{RE} is 10)

Frequency range: 500 Hz to 20 kHz

Step by Step Design:

1. Determine V_{RE}:

$$V_{RE} = 0.1 \times V_{CC} = 0.1 \times 12 = 1.2\ V$$

2. Determine I_C:

Assuming $I_C = I_E$, let's choose a value for I_C. A common value is $1\ mA$.

3. Determine R_E:

$$R_E = \frac{V_{RE}}{I_E} = \frac{1.2}{0.001} = 1200\ \Omega$$

4. Determine \(V_{RC}\) (Collector Voltage):

$$V_{RC} = V_{CC} - V_{CE} = 12 - 6 = 6\ V$$

5. Determine I_C(Collector Current):

   Use the relation $I_C = \frac{V_{RC}}{R_C}$. Choose a standard value for R_C.

   $$R_C = \frac{V_{RC}}{I_C} = \frac{6}{0.001} = 6000\ \Omega$$

   Choose a standard resistor value, e.g., $R_C = 5.6\ k\Omega$.

6. Determine V_{RB} (Base Voltage):

   $$V_{RB} = V_{CC} - V_{RE} = 12 - 1.2 = 10.8\ V$$

7. Choose R_1 and R_2 for Voltage Divider Biasing:

   The voltage across R_2 can be chosen to be approximately $0.1 \times V_{CC}$ for stability.

   $$R_2 = \frac{0.1 \times V_{CC}}{I_B}$$

   Assuming a base current (I_B) of 10% of I_C, let's choose $R_2 = 1\ M\Omega$.

   Then, calculate R_1 using the relation $V_{RB} = V_{CC} \times \frac{R_1}{R_1 + R_2}$:

   $$R_1 = \frac{V_{RB} \times R_2}{V_{CC} - V_{RB}}$$

8. Determine C_{in}(Input Capacitor):

   Choose C_{in} to block DC and allow AC. A common choice is $10\ \mu F$.

9. Determine C_{out} (Output Capacitor):

   Choose C_{out} to pass AC and block DC. A common choice is $100\ \mu F$.

Procedure

1. Connect the circuit as shown in circuit diagram.
2. Apply the input of 20mV peak to peak and 1 KHz frequency using Function Generator
3. Measure the Output Voltage Vo peak to peak for various load resistors.

4. Tabulate the readings in the tabular form.

5. The voltage gain can be calculated by using the expression $A_v = \frac{V_o}{V_i}$

6. For plotting the frequency response the input voltage is kept Constant at 20mV peak to peak and the frequency is varied from 100Hz to 1MHz Using functiongenerator.

7. Note down the value of output voltage for each frequency.

8. All the readings are tabulated and voltage gain in dB is calculated by Using The expression $A_v = 20\log\frac{V_o}{V_i}$

9. A graph is drawn by taking frequency on Xaxis and gain in dB on Yaxis on Semilog graph.

10. The band width of the amplifier is calculated from the graph using the expression,

$$Bandwidth = f_H - f_L$$

Where f_L lower cutoff frequency of CE amplifier, and Where f_H upper cutoff frequency of CE amplifier.

Observations

Voltage Gain

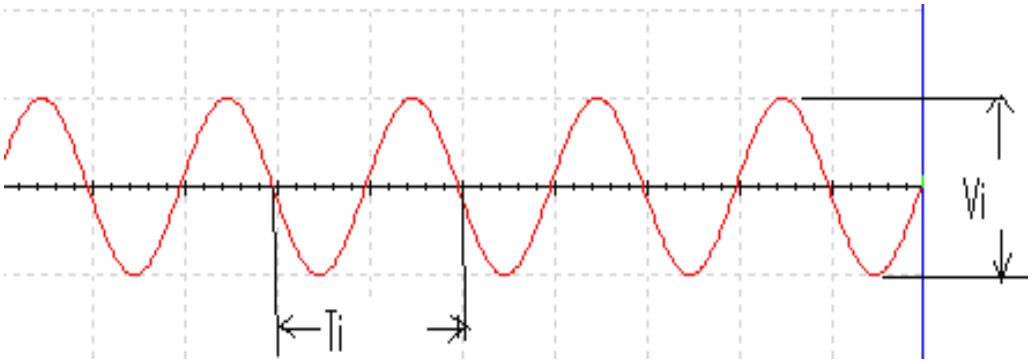
Load Resistance(KΩ)	Output Voltage (V_0)	Gain $A_V=(V_o/V_i)$	Gain In dB

Frequency Response

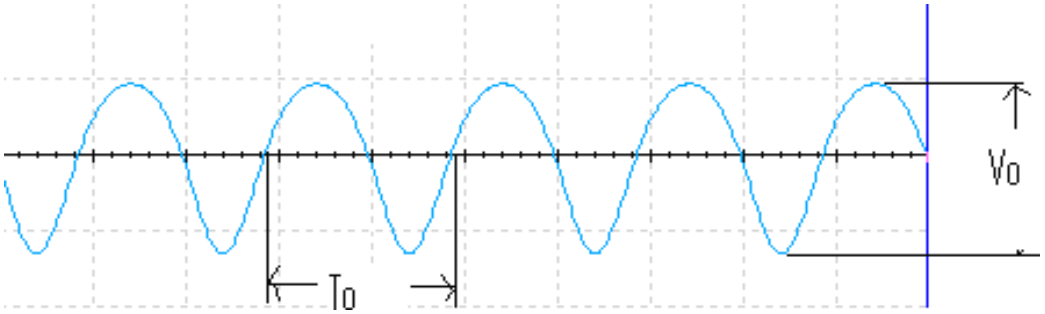
Frequency f(Hz)	V_o in (mV)	Gain= $\frac{V_o}{V_i}$	Gain in dB

Modelwave Forms

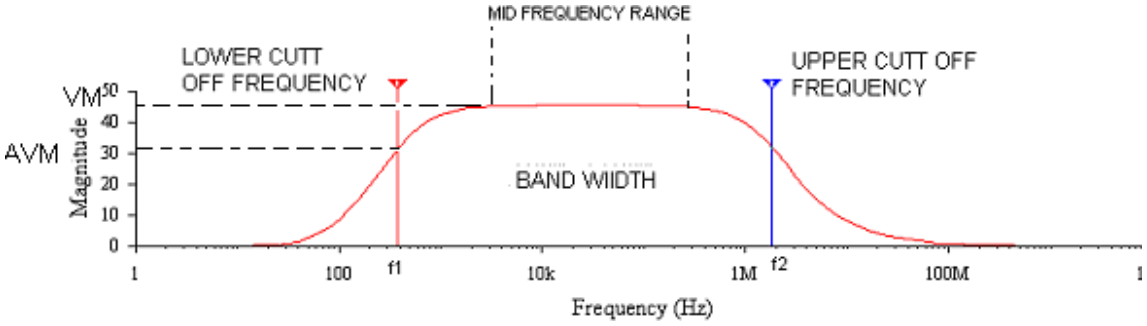
Input Wave Form:



Output Wave Form



Frequency Response



Result

The voltage gain and frequency response of the CE amplifier are obtained. Also gain bandwidth product of the amplifier is calculated.

Viva Questions

1. What is phase difference between input and output waveforms of CE amplifier?
2. What type of biasing is used in the given circuit?

3. If the given transistor is replaced by a pnp, can we get output or not?
4. What is effect of emitter bypass capacitor on frequency response?
5. What is the effect of coupling capacitor?
6. What is region of the transistor so that it is operated as an amplifier?
7. How does transistor acts as an amplifier?
8. Draw the h parameter model of CE amplifier?
9. What type of transistor configuration is used in intermediate stages of a multistage amplifier?
10. What is Early effect?

2. Common Collector Amplifier

Aim

1. To design a small signal voltage amplifier and measure the voltage gain.
2. To plot its frequency response and to obtain bandwidth.

Apparatus

I. NPN Bipolar Junction Transistor (BJT)

II. Resistors (as per design requirements)

III. Capacitors (as per design requirements)

IV. Signal Generator

V. Oscilloscope

VI. Breadboard and Connecting Wires

Theory

In the previous lab you design a common emitter (CE) amplifier. Voltage gain (Av) is easy to achieve with this type of amplifier. As you discovered the input impedance (RIN) of the CE is moderate to high (on the order of a few kilo Ohms). The output impedance (ROUT) is high (roughly the value of RC). This makes the common emitter amplifier a poor choice for 'driving' small loads.

A common collector (CC) amplifier typically has a high input impedance (typically in the hundred kilo Ohm range) and a very low output impedance (from 1 to ~tens of Ohms). This makes the common collector amplifier excellent for 'driving' small loads. As you discovered in lab 5, the common collector amplifier has a voltage gain of about 1, or unity. The common collector amplifier is considered a voltage buffer, as the voltage gain is unity, the voltage signal applied at the input will be duplicated at the output; for this reason the common collector amplifier is typically called a "emitter follow amplifier." The common collector amplifier can be thought of as a current amplifier.

When the common emitter amplifier is cascaded to a common collector amplifier, the CC can be thought of as an 'impedance transformer.' It can take the high output impedance of the CE amplifier and 'transform it' to a low output impedance capable ofdriving small loads.

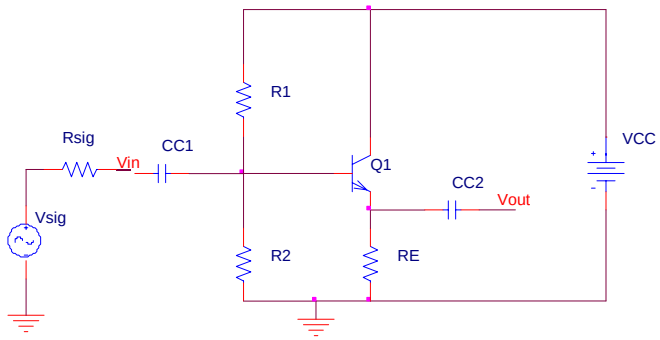


Figure 2.1 Common collector amplifier

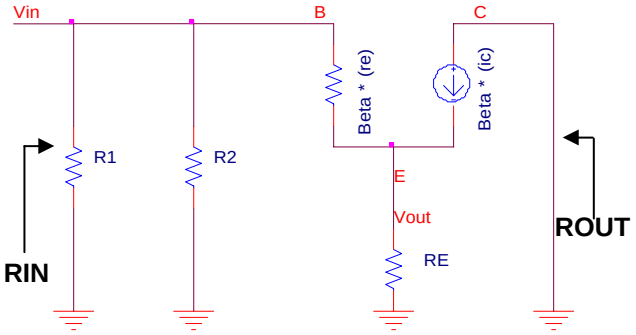


Figure 2.2 Small Signal (AC) equivalent (neglecting Rsig)

Figure 2.1 shows a typical configuration for a common collector amplifier. The input voltage is applied to the base while the output voltage is measured at the emitter.

From the AC equivalent of the common collector amplifier in figure 2.2, we can derive the input impedance, output impedance, and voltage gain:

RIN = R1 || R2 || [βre + (β+1) RE] (no load) (Remember: re = VT / IE, where VT = 26mV

ROUT = RE || re but re << RE → Zo ≈ re (notice this is VERY small)

$$Av = \frac{Vout}{Vin} = \frac{(\beta+1)ib * RE}{(\beta)(ib)(re)+(\beta+1)(ib)(RE)} \cong \frac{(\beta)ib * RE}{(\beta)ib(re+RE)} = \frac{RE}{(re+RE)}$$, but since re << RE, then $Av \approx 1$.

<u>Designing a common collector Amplifier</u>

Problem: Design a common collector Amplifier using the BC107 transistor that meets the following specifications:

IC = 1mA
VCC = 20 Volts
Rin = 70KΩ
RL = 510Ω
v*in* = 10mV @ 10kHz

Step 1) Determine the size of RE

- We typically make VE = ½ VCC, to ensure the largest possible symmetric output voltage swing (around VE)
- It is safe to assume that IE ≈ IC
- Calculate the value of RE

Step 2) Determine the "Q" point of the transistor

- Because you now know VCE & IC, you can use the same procedure from the "Designing a common emitter Amplifier Tutorial" to create an IV curve for the transistor & determine the Q point of the transistor. This will help you determine the necessary "base current" needed to achieve the specified IC.
- Use the Qpoint data to find DC values for: IB, VB, IE, β

Step 3) Use VCC, VB, IB, IE, and RIN, to find R1 and R2

- Follow the procedure from the "*Designing a common emitter Amplifier "* to generate the same 3 equations for VBB , RB and IB .
- Use the equation derived for **RIN.**
- Calculate R1 and R2 using the equations.

Step 4) Check your calculations

- Using the RIN equation, calculate RIN. Is it 70k?
- Using the ROUT equation, calculate ROUT, is it very small?

Step 5) Set values for CC1 & CC2

- The impedance of a capacitor Zc = 1/j2πfC, make CC1, CC2 look like a 'short' at 10kHz (the input frequency), and make sure the size you choose for CC1 and CC2 matches a capacitor value you have in your ECE lab.

Procedure

1. Connect the circuit as shown in circuit diagram.
2. Apply the input of 20mV peaktopeak and 1 KHz frequency using Function Generator
3. Measure the Output Voltage Vo peak to peak for various load resistors.
4. Tabulate the readings in the tabular form.
5. The voltage gain can be calculated by using the expression $A_V = V_0 / V_1$
6. For plotting the frequency response the input voltage is kept Constant at 20mV peak to peak and the frequency is varied from 100Hz to 1MHz Using functiongenerator.
7. Note down the value of output voltage for each frequency.
8. All the readings are tabulated and voltage gain in dB is calculated by Using The expression $A_V = 20 \log V_0 / V_1$
9. A graph is drawn by taking frequency on X axis and gain in dB on Yaxis on Semilog graph.

10. The band width of the amplifier is calculated from the graph using the expression,

$$Bandwidth = f_H - f_L$$

Where f_L lower cutoff frequency of CC amplifier, and Where f_H upper cutoff frequency of CE amplifier.

Observations

Voltage Gain

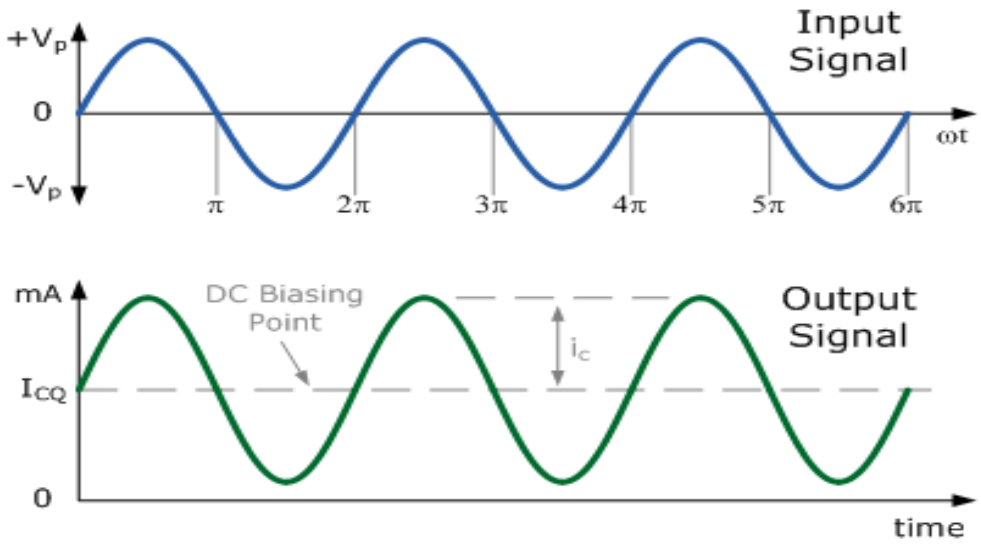
Load Resistance(KΩ)	Output Voltage (V_0)	Gain $A_V=(V_o/V_i)$	Gain In dB

Frequency Response

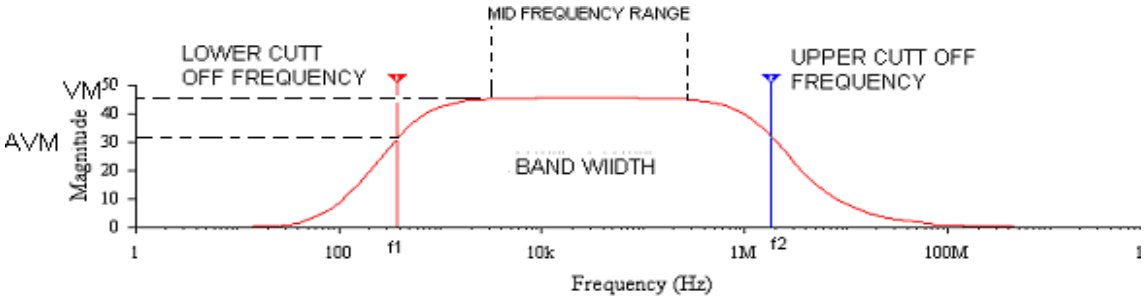
Frequency f(Hz)	V_o in (mV)	Gain= $\frac{V_o}{V_i}$	Gain in dB

Model wave Forms

Input Wave Form and Output Wave Form



Frequency Response



Result

The voltage gain and frequency response of the CC amplifier are obtained. Also gain bandwidth product of the amplifier is calculated.

Viva Questions

1. Define the voltage gain of a Common Collector amplifier.
2. Explain how the Common Collector configuration achieves a voltage gain less than unity.
3. Explain the purpose of introducing emitter resistance in the Common Collector configuration.
4. Define the load line of a transistor amplifier.
5. Sketch the load line for a Common Collector amplifier and explain how it is useful for understanding transistor operation.
6. Discuss the factors influencing the frequency response of the Common Collector amplifier.
7. Explain the purpose of capacitor coupling in the input and output of the Common Collector amplifier.
8. Discuss how capacitor coupling influences the amplifier's frequency response.
9. Define the Miller effect in the context of transistor amplifiers.
10. Discuss how the Miller effect influences the input and output capacitances of the Common Collector amplifier.
11. Explain the concept of AC load line analysis in transistor amplifiers.
12. Illustrate how the AC load line is used to determine the operating point and signal swing in the Common Collector configuration.
13. Compare the voltage gain and frequency response characteristics of the Common Collector amplifier with those of the Common Emitter.
14. Discuss the advantages and disadvantages of using the Common Collector configuration in specific applications.

3.Two Stage RC Coupled Amplifier

1. To design a Two Stage Amplifier and Plot the frequency response.
2. Calculate gain.
3. Calculate bandwidth.

Apparatus

i. NPN Bipolar Junction Transistor (BJT BC 107)

ii. Resistors (as per design requirements)

iii. Capacitors (as per design requirements)

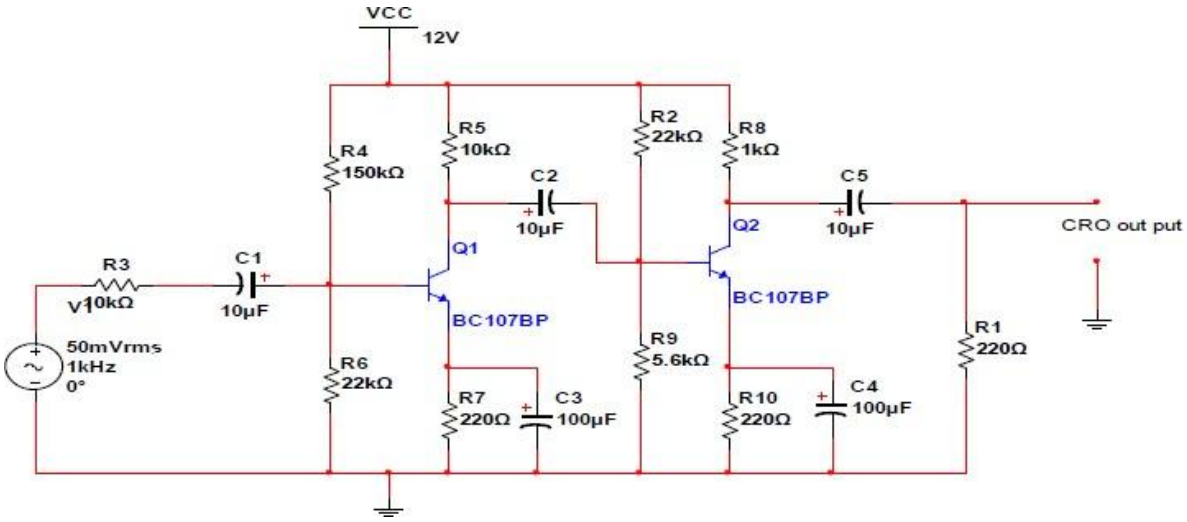
iv. Signal Generator

v. Oscilloscope

vi. Multimeter

vii.Breadboard and Connecting Wires

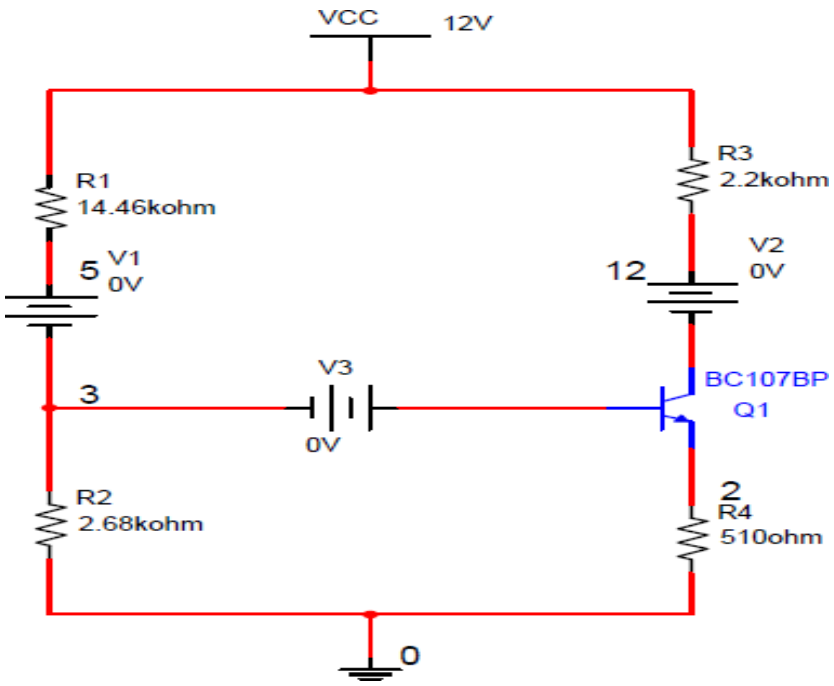
Circuit Diagram



Design

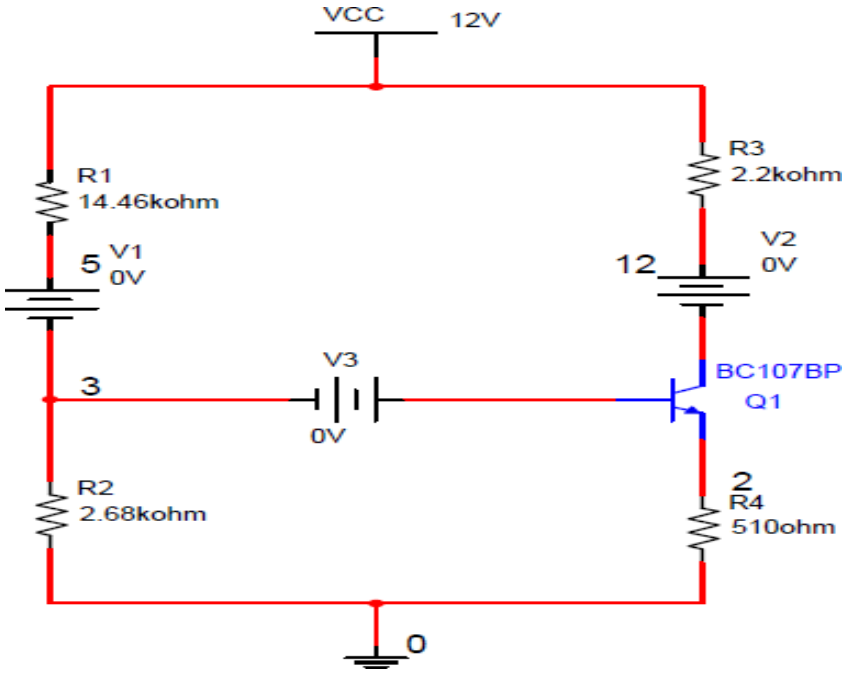
Design a single stage transistor amplifier with potential divider circuit (using an npn BC 107 transistors) with following specifications.

IC=2.32ma,VCE=5.7v,RC=2.2k,VCC=12v, I1=10IB and β=33.
IB=IC/β = 2.32/33=0.07ma
VCC=IC(RC+RE)+VCE ; 12=2.32(2.2+RE)+5.7 ; RE=0.51k
V2=VBE+ICRE ; V2=0.7+2.32*0.51=1.88v
V2=I1R2 ; R2=V2/(I1=10IB) ; 1.88/0.7=2.68k
I1=VCC/(R1+R2) ; (R1+R2)=12/0.7=17.14k ; R1=17.142.68=14.46k



Design a single stage 2nd transistor amplifier with potential divider circuit (using an npn si transistors) with following specifications.
IC=2.32ma,VCE=5.7v,RC=2.2k,VCC=12v, I1=10IB and β=33.

IB=IC/β = 2.32/33=0.07ma
VCC=IC(RC+RE)+VCE ; 12=2.32(2.2+RE)+5.7 ; RE=0.51k
V2=VBE+ICRE ; V2=0.7+2.32*0.51=1.88v
V2=I1R2 ; R2=V2/(I1=10IB) ; 1.88/0.7=2.68k
I1=VCC/(R1+R2) ; (R1+R2)=12/0.7=17.14k ; R1=17.142.68=14.46k



Cascade above two stages and find overall gain (choose C_c=4.7µf, C_e=470µf, h_{fe}=50) find the frequency response, DC operating points and parameter sweep of load resister.

ANALYSIS:

Stage2: $AI_2 = h_{fe}/(1+h_{oe}R_{L2})$; 50/(1+2/40) = 47.62

$R_{i2} = h_{ie}+h_{re}AI_2R_{L2}$;1.1+2.5e4*47.62*2 = 1.076k;

$Av_2 = AI_2*R_{L2}/R_{i2}$; 47.62*2/1.076 = 88.51

Stage1: R_{L1} = 2.2k||14.2||2.5||1.076 = 0.54k

AI_1 = 50/(1+0.54/40) = 49.3

R_{i1} = 1.1+2.5e4*49.3*0.54 = 1.106k

Av_1 = 49.3*0.54/1.106 = 24.07

Overall gain Av = Av_1*Av_2 = 24.07*88.51= 2130.4

Avs = Av*R_i'/(R_i'+R_S) ; R_i' = 1.106||33||5.1= 0.88k

=2130.4*0.88/(0.88+15) =118

Procedure:

1. Connect the circuit diagram as shown in figure.
2. Adjust input signal amplitude in the function generator and observe an amplified voltage at the output without distortion.
3. By keeping input signal voltage, say at 50mV, vary the input signal frequency from0 to 1MHz in steps as shown in tabular column and note the corresponding outputvoltages.

PRECAUTIONS:

1. Avoid loose connections and give proper input Voltage

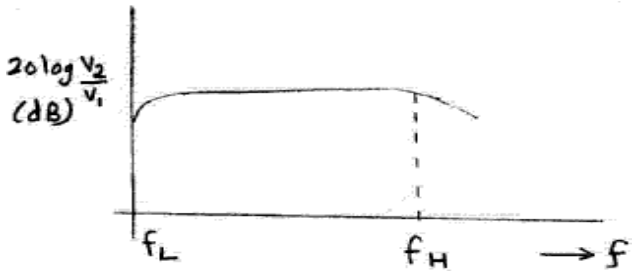
TABULAR COLUMN: Input = 50mV

Frequency (Hz)	Output Voltage(Vo)		Gain=V_0/V_i		Gain(in dB) =20log10(Vo/Vi)	
	With feedback	Without feedback	With feedback	Without feedback	With feedback	Without feedback
20						
40						
80						
100						
1K						
10k						
50k,100K						
1M						

RESULT:

1. Frequency response of Two stage RC coupled amplifier is plotted.
2. Gain =_____dB (maximum).
3. Bandwidth= fH-fL =_____Hz. At stage I
4. Bandwidth= fH-fL =_____Hz. At stage 2

Model wave Forms



Viva Questions

1. Explain the significance of using a two stage RC coupled amplifier over a single stage configuration.
2. Define the term "frequency response" in the context of an amplifier. Why is it essential to analyze the frequency response?
3. Discuss the impact of coupling capacitors on the low frequency response of the amplifier. How can this be addressed in design?
4. Explain the purpose of coupling capacitors in each stage of the RC coupled amplifier. How do they affect the overall performance?
5. Describe the significance of selecting appropriate values for coupling capacitors concerning the lower and upper cutoff frequencies.
6. How do bypass capacitors affect the amplifier's performance, especially in the context of signal coupling?
7. Analyze the effect of load resistance on the voltage gain of the RC coupled amplifier. How does it impact the overall performance?
8. Discuss the advantages and challenges of cascading multiple amplifier stages. How does it contribute to achieving higher overall gain?
9. Explain the role of decoupling capacitors in the power supply lines. How do they contribute to maintaining stable biasing conditions?
10. Discuss potential sources of signal distortion in a two stage RC coupled amplifier. How can distortion be minimized in the design?

4.Current Series and Voltage Shunt Feedback Amplifier

Aim

To design and test the current-series and voltage shunt feedback amplifier and to calculate the following parameters with and without feedback.

1. Mid band gain.
2. Bandwidth and cut-off frequencies.
3. Input and output impedance

Apparatus

i. Power supply (0-30)V
ii. Function Generator (0-20M)Hz
iii. CRO 1
iv. Transistor BC107
v. Resistor
vi. Capacitor
vii. Connecting Wire

Theory:

Series Feedback Amplifier

The current series feedback amplifier is characterized by having shunt sampling and series mixing. In amplifiers, there is a sampling network, which samples the output and gives to the feedback network. The feedback signal is mixed with input signal by either shunt or series mixing technique. Due to shunt sampling the output resistance increases by a factor of 'D' and the input resistance is also increased by the same factor due to series mixing. This is basically transconductance amplifier. Its input is voltage which is amplified as current.

Shunt Feedback Amplifier

In voltage shunt feedback amplifier, the feedback signal voltage is given to the base of the transistor in shunt through the base resistor R_B. This shunt connection tends to decrease the input resistance and the voltage feedback tends to decrease the output resistance. In the circuit R_B appears directly across the input base terminal and output collector terminal. A part of output is feedback to input through RB and increase in IC decreases IB. Thus negative feedback exists in the circuit. So this circuit is also called voltage feedback bias circuit. This feedback amplifier is known a trans resistance amplifier. It amplifies the input current to required voltage levels. The feedback path consists of a resistor and a capacitor.

Procedure

1. Connect the circuit as per the circuit diagram.
2. Keeping the input voltage constant, vary the frequency from 50Hz to 3MHz in regular steps and note down the corresponding output voltage.

3. Plot the graph: Gain (dB) Vs Frequency
4. Calculate the bandwidth from the graph.
5. Calculate the input and output impedance.
6. Remove Emitter Capacitance, and follow the same procedures (1 to 5).

Design

(i) Series Feedback Amplifier: Without Feedback:

$V_{CC} = 12V;\quad I_C = 1mA;\quad f_L = 50Hz;\quad S = 2;\ R_L = 4.7K\Omega$

$r_e = \frac{26mV}{I_c} =$

$V_{ce} = \frac{V_{cc}}{2} =$

$V_E = {}^{V_{CC}}/_{10}\ h_{ie} = h_{fe}r_e;$

Applying KVL output loop, we get $V_{cc} = I_E R_E + I_C R_C + V_{ce};$

$R_C =$

$R_L = 4.7K\Omega$

Since I_B is very small when compare with $I_C, I_C \approx I_E$

$R_E = \frac{V_E}{I_E};\qquad S = 1 + \frac{R_B}{R_E}$

$R_B =$

$V_B = \frac{V_{CC}R_2}{(R_1+R_2)}\quad R_B = R_1//R_2$

$R_1 = \qquad R_2 =$

$X_{Ci} = \frac{h_{ie}//R_B}{10}\quad C_i = \frac{1}{2\pi f X_{ci}}\qquad X_{Co} = \frac{R_C//R_L}{10}\quad C_o = \frac{1}{2\pi f X_{co}}$

With feedback (Remove the Emitter Capacitor, C_E):

Feedback factor, $\beta = -R_E =$

$G_m = -h_{fe} / (h_{ie} + R_E) =$

Desensitivity factor, $D = 1 + \beta G_m =$

Transconductance with feedback, $G_{mf} = G_m / D =$

Input impedance with feedback, $Z_{if} = Z_i D$

Output impedance with feedback, $Z_{of} = Z_o D$

(ii) Shunt Feedback Amplifier: Without Feedback:

$V_{cc} = 12V \quad I_c = 1mA; \quad A_v = 30; \quad R_f = 2.5K\Omega; \quad s = 2;$

$r_e = \frac{26mV}{I_c} =$

$\beta = \frac{1}{R_f} =$

$h_{fe} =$

$h_{ie} = h_{fe} r_e;$

$V_{ce} = \frac{V_{cc}}{2} =$

$V_E = {}^{V_{CC}}/_{10};$

Applying KVL to output loop, we get $V_{cc} = I_E R_E + I_C R_C + V_{ce};$

$R_C =$

Since I_B is very small when compare with $I_C, I_C \approx I_E$

$R_E = \frac{V_E}{I_E}; S = 1 + \frac{R_B}{R_E}$

$R_B =$

$$V_B = \frac{V_{CC} R_2}{(R_1 + R_2)} R_B = R_1 // R_2$$

$R_1 = \qquad R_2 =$

With feedback:

$$R_O = R_C // R_f R_i = (R_B // h_{ie}) R_f$$

$R_m = -(h_{fe}(R_B // R_f)(R_C // R_f))/((R_B // R_f) + h_{ie})$

Desensitivity factor, $D = 1 + \beta R_m \quad R_{if} = \frac{R_i}{D} \quad R_{of} = \frac{R_o}{D} R_{mf} = \frac{R_m}{D}$

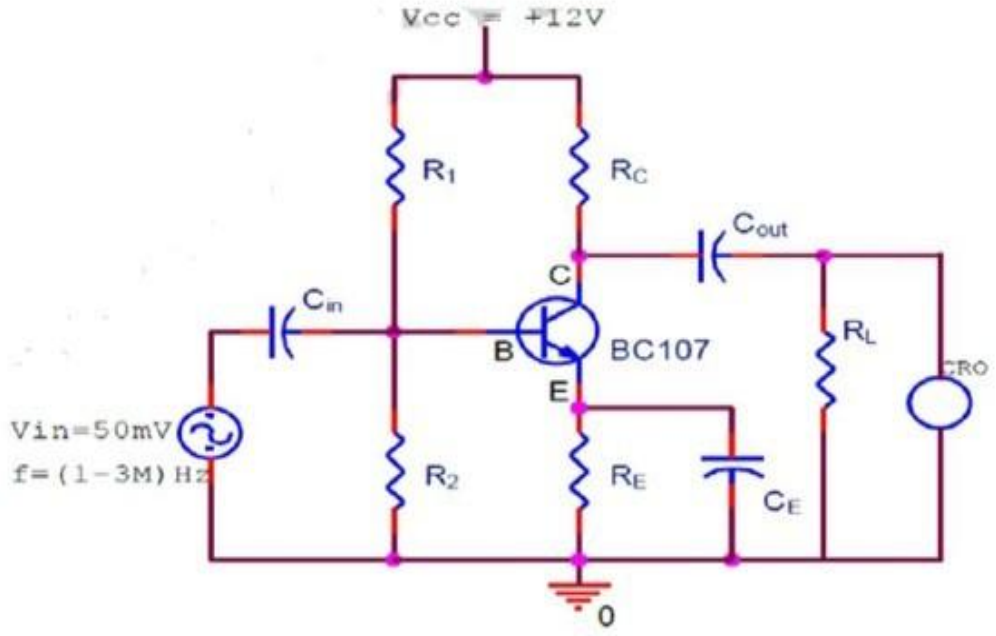
$X_{Ci} = \frac{R_{if}}{10} \quad C_i = \frac{1}{2\pi f X_{ci}} \quad X_{Co} = \frac{R_{of}}{10} \quad C_o = \frac{1}{2\pi f X_{co}}$

$R_{E'} = R_E // (\frac{R_B + h_{ie}}{1 + h_{fe}}) \quad X_{CE} = R_{E'}/10 \; C_E = \frac{1}{2\pi f X_{cE}}$

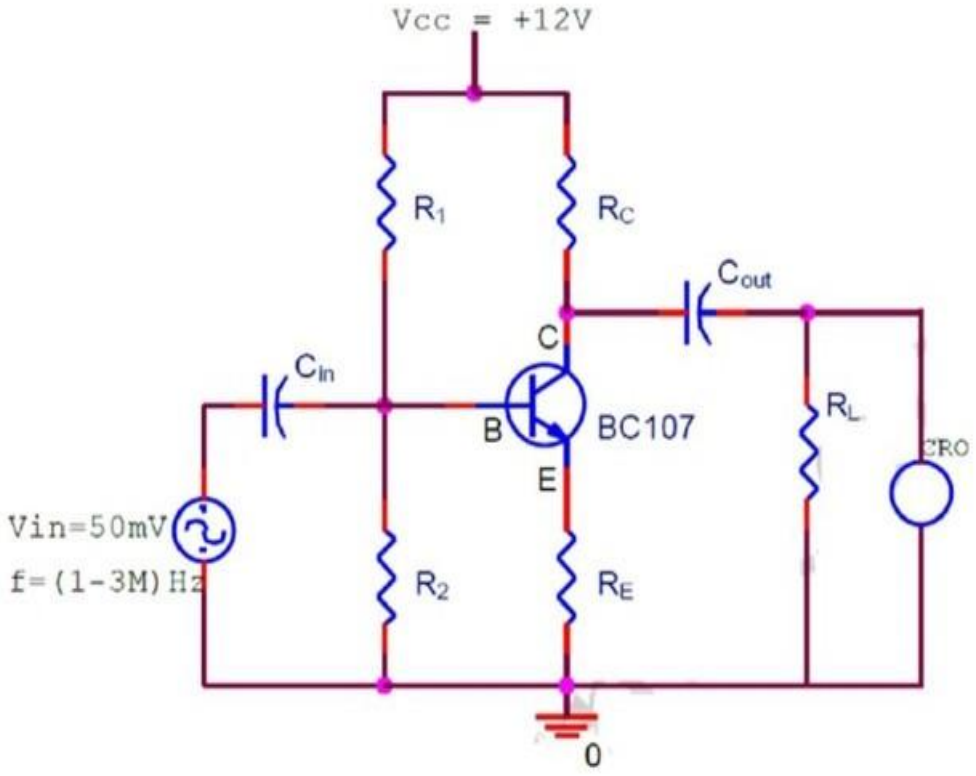
$$X_{Cf} = R_f/10 C_f = \frac{1}{2\pi f X_{cf}}$$

Circuit Diagram

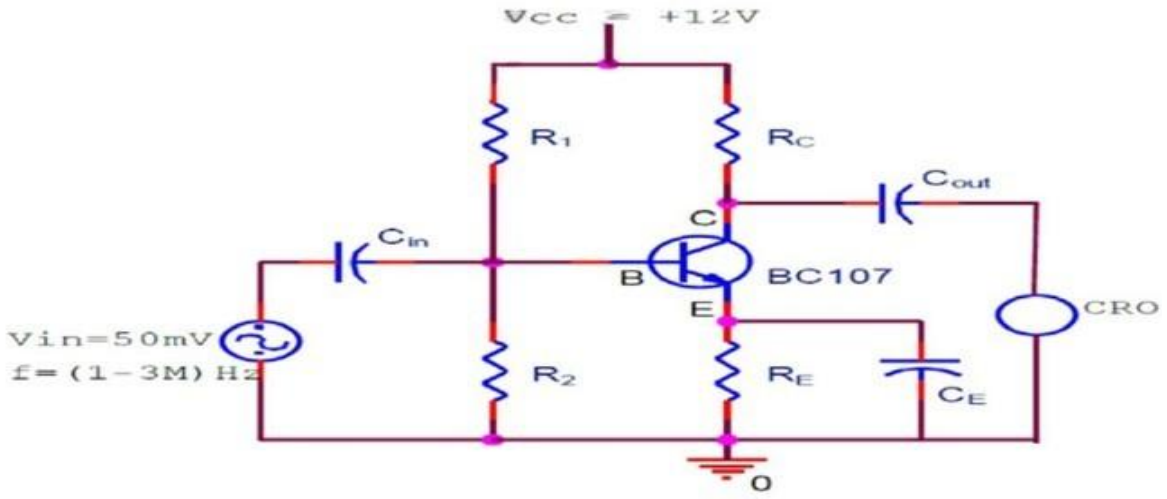
Series Feedback Amplifier: Without Feedback:



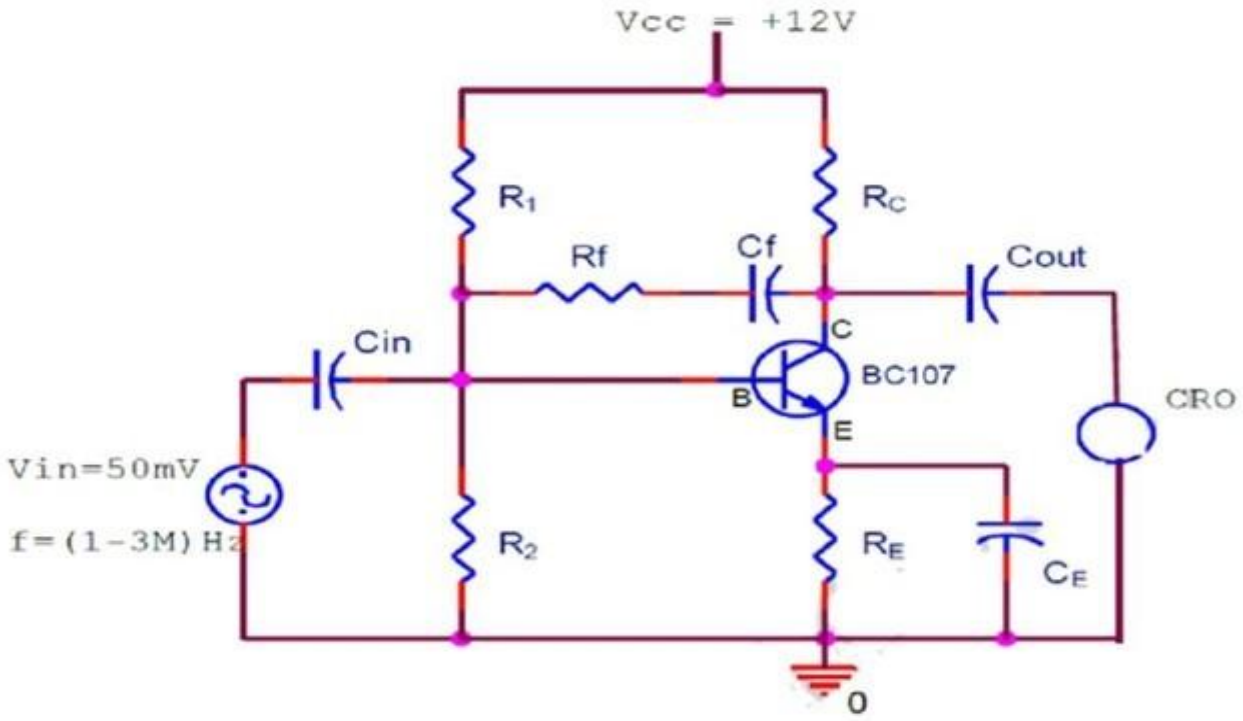
Series Feedback Amplifier: With Feedback:



Shunt Feedback Amplifier: Without Feedback:



Shunt Feedback Amplifier: With Feedback:



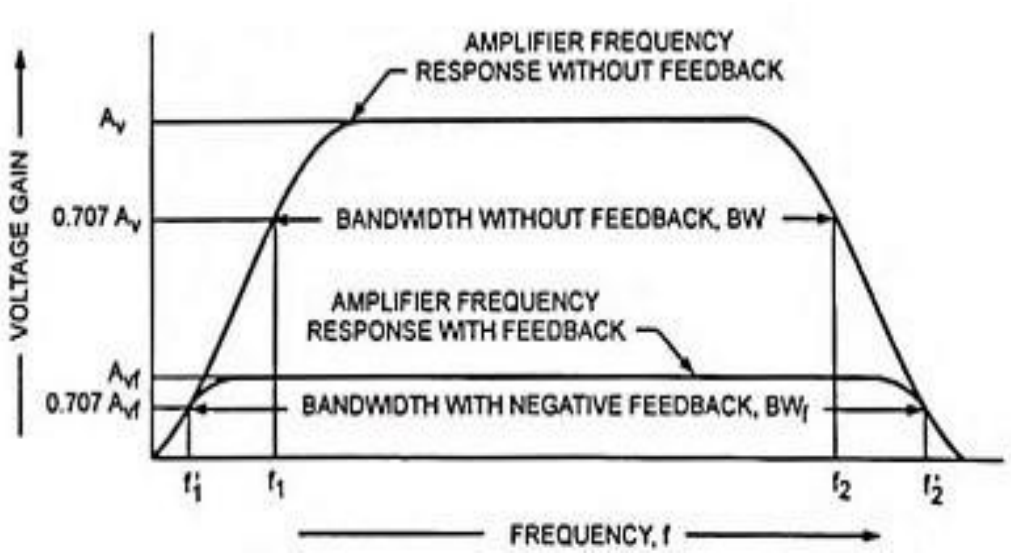
Observations

Without feed back

Frequency (Hz)	Vo (Volts)	Gain = V_0/V_i	Gain = 20 $\log(V_0/V_i)$ (dB)

With feed back

Frequency (Hz)	Vo (Volts)	Gain = V_0/V_i	Gain = 20 $\log(V_0/V_i)$ (dB)



Model Graphs

Viva Questions

1. What is feedback?
2. What is positive feedback?
3. Define amplification factor?
4. What is Q-point?
5. What is the difference between positive feedback and negative feedback?
6. Define Sensitivity?
7. What are the applications of feedback amplifiers?
8. What is the effect of current series feedback amplifier on the input impedance of the amplifier?
9. Mention the properties of negative feedback?
10. Give an example of negative shunt feedback?
11. Define voltage shunt feedback?
12. What is the effect of negative feedback on the bandwidth of an amplifier?

5.Wein Bridge Oscillator

Aim

To design a wein bridge oscillator and to draw its output waveform.

FACILITIES REQUIRED AND PROCEDURE

S.NO	APPARATUS	SPECIFICATION	QUANTITY
1.	Power supply	(0-30)V	1
2.	Function Generator	(0-20M)Hz	1
3.	CRO		1
4.	Transistor	BC107	1
5.	Resistor		
6.	Capacitor		
7.	Connecting Wires		

Theory

The Wien bridge oscillator employs a balanced wien bridge as the feedback network. Two stage CE amplifier provides 360 phase shift to the signal. So the Wienbridge need not introduce any phase shift to satisfy Barkausen criterion. The attenuation of the bridges calculated to be 1/3 at resonant frequency. So the amplifier stage should provide a gain of exactly 3 to make loop gain unity. Since the gain of two stage amplifier is the product of individual stages , overall gain becomes very high. But the gain will be trimmed down to 3 by negative feedback network. The emitter resistors of both stages are kept un bypassed . This provides a current series feedback which ensures the stability of operating point and reduction of gain. Frequency of oscillation is given by $f = 1/2\pi RC$

Procedure

1. Connections are made as per the circuit diagram.
2. Feed the output of the oscillator to a CRO by making adjustments in the Potentiometer connected in the positive feedback loop, try to obtain a stable sine wave.
3. Measure the time period of the waveform obtained on CRO. & calculate the frequency of oscillations.
4. Repeat the procedure for different values of capacitance.

Design

Given data

Design of R_c: $R_C = \frac{V_{RC}}{I_C} = 2.4K\Omega;$

Design of R_E: $R_E = \frac{V_{RE}}{I_E} = 600\Omega;$

Design of R_1 and R_2: $I_B = \frac{I_C}{h_{fe}} = 20\mu A;$

Assume the current through $R_1 is\ 10I_B$ and $R_2 is\ 9I_B$

$V_{R2} = V_{BE} + V_{RE} = 1.9V;$

$V_{R2} = 9I_B * R_2;$ $R_2 = 10.6K\Omega;$

$V_{R1} = V_{CC} - V_{R2} = 10.1V;$ $V_{R1} = 10I_B * R_1;$

$R_1 = 50K\Omega;$ f=1KHz;

$f=1/2\pi C_c(R_1//R_2//h_{fe}R_E)$

$C_c = 44\mu F;$

The required frequency of oscillation $f_C = \frac{1}{2\pi RC} = 10KHz;$

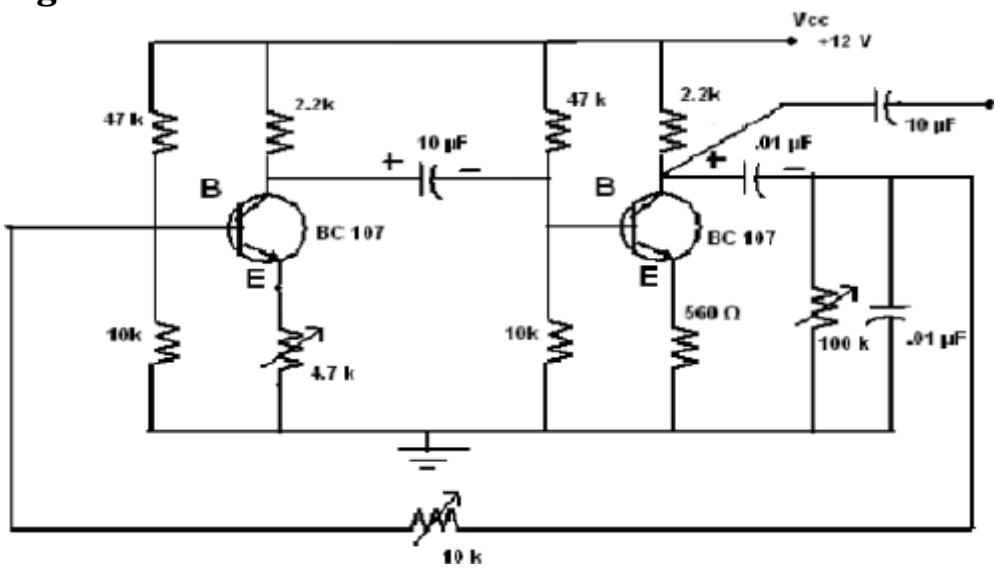
Take R=47KΩ and C=0.01μF;

Gain of the amplifier must be 3;

Negative feedback factor is given by $R_E/(R_E + R_3)$

$R_E/(R_E + R_3) = 3;$ $R_3 = 12K\Omega;$

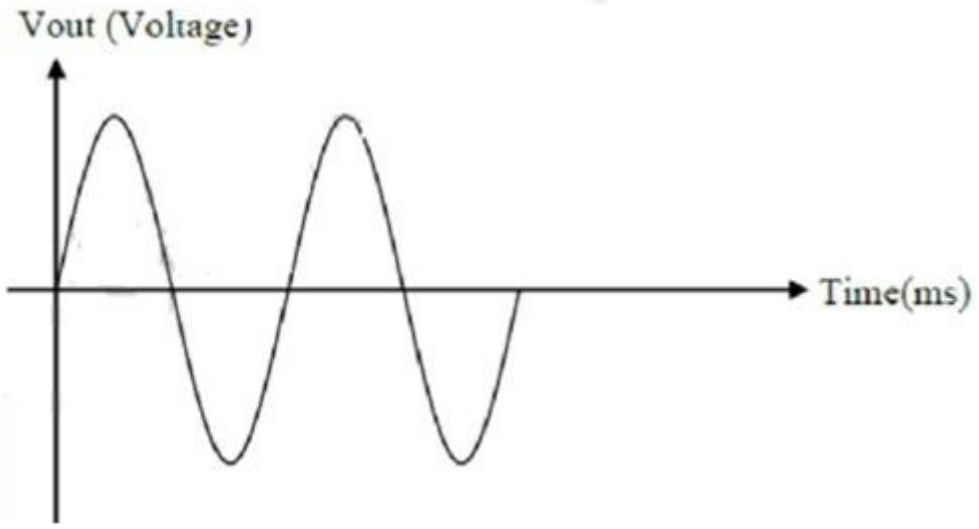
Circuit Diagram



Observations

Sl No	Amplitude	Time	Frequency

Model Waves



Result

Thus a Wienbridge oscillator is designed, verified and the output waveform is drawn.

Viva Questions

1. Define oscillator?
2. What is resonant frequency?
3. Define Q-point?
4. Define tuned amplifier?
5. State Barkhausen criteria?
6. What are the applications of Wein bridge oscillator?
7. What is the efficiency of Wein bridge oscillator?
8. How to produce sinusoidal output from Wein bridge oscillator?

6. Design Of Transistor RC Phase Shift Oscillator

Aim

To design and construct a RC phase shift oscillator for the given frequency with following data

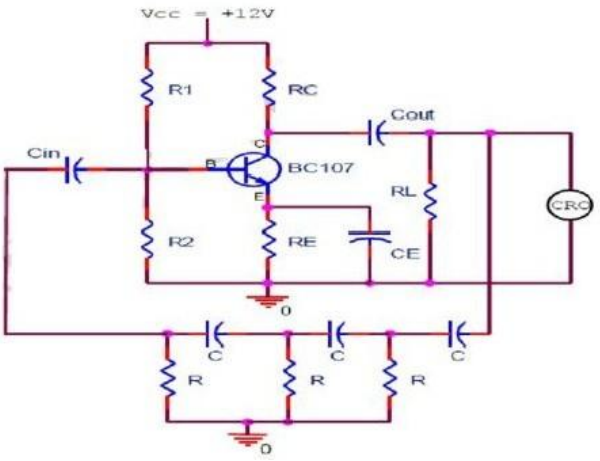
Apparatus Required

Sl.No	Apparatus	Specification	Quantity
1.	Power supply	(0-30)V	1
2.	Function Generator	(0-20M)Hz	1
3.	CRO		1
4.	Transistor	BC107	1
5.	Resistor		
6.	Capacitor		
7.	Connecting Wires		

Theory

In the RC phase shift oscillator, the required phase shift of 180 ˚ in the feedback loop from the output to input is obtained by using R and C components, instead of tankcircuit. Here a common emitter amplifier is used in forward path followed by threesections of RC phase network in the reverse path with the output of the last section being returned to the input of the amplifier. The phase shift Φ is given by each RC section Φ=tan¯1 (1/ωrc). In practice R-value is adjusted such that Φ becomes 60 . If the value of R and C are chosen such that the given frequency for the phase shift of each RC section is 60 ˚. Therefore at a specific frequency the total phase shift from base to transistor's around circuit and back to base is exactly 360 ˚ or . Thus the Barkhausen criterion for oscillation is satisfied.

Circuit Diagram



Design

$r_e = \frac{26mV}{I_c} =$

$\beta = \frac{1}{R_f} =$

$h_{fe} =$

$h_{ie} = h_{fe} r_e;$

$V_{ce} = \frac{V_{cc}}{2} =$

$V_E = {}^{V_{CC}}/_{10};$

Applying KVL to output loop, we get $V_{cc} = I_E R_E + I_C R_C + V_{ce};$

$R_C =$

Since I_B is very small when compare with $I_C, I_C \approx \mathrm{I_E}$

$R_E = \frac{V_E}{I_E};$ $S = 1 + \frac{R_B}{R_E}$

$R_B =$

$V_B = \frac{V_{CC} R_2}{(R_1 + R_2)}$ $R_B = R_1 // R_2$

$R_1 =$ $R_2 =$

Gain formula is given by $A_v = \frac{-h_{fe} R_{Leff}}{h_{ie}}$

$A_v = -29;$

$R_{Leff} = R_C // R_L;$

$R_L =$

$X_{Ci} = ([h_{ie} + (1 + h_{fe}) R_E] // R_B)/10 =$

$C_i = 1/2\pi f X_{Ci}$ $X_{CO} = {}^{RL_{eff}}/_{10};$ $C_o = 1/2\pi f X_{CO};$ $C_E = \frac{R_E}{10};$

$C_E = 1/2\pi f X_{CE}$ C=0.01μF; $f = 1/2\pi RC\sqrt{6}$

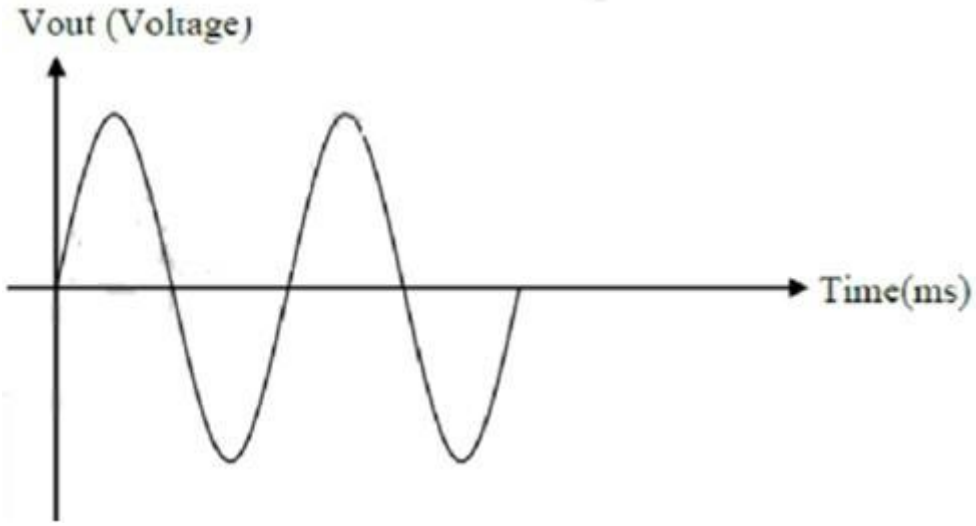
Procedure

1. Connections are made as per the circuit diagram.
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare with its theoretical frequency.

Observations

Sl No	Amplitude	Time	Frequency

Model Wave



Result

Thus RC phase shift oscillator is designed and constructed and the output sine wave frequency is calculated.

Viva Questions

1. What is oscillator circuit?
2. What are the different types of oscillators?
3. What are the conditions for oscillations?
4. Define frequency loop?
5. What are the applications of RC phase shift oscillator?
6. Why RC oscillator cannot generate high frequency oscillations?
7. What phase shift does RC phase oscillator produce?
8. How is phase angle determined in RC phase shift oscillator?
9. How can we get a maximum phase angle of 90^0 in RC phase shift oscillator?

7. Design Of Hartley And Colpitt Oscillator

Aim

To design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation.

A) Hartley Oscillator

B) Colpitts Oscillator

Apparatus Required

Sl.No	Apparatus	Specification	Quantity
1.	Power supply	(0-30)V	1
2.	Function Generator	(0-20M)Hz	1
3.	CRO	-	1
4.	Transistor	BC107	1
5.	Resistor		1
6.	Capacitor		3
	Inductance		2
7.	Connecting Wires		

Theory

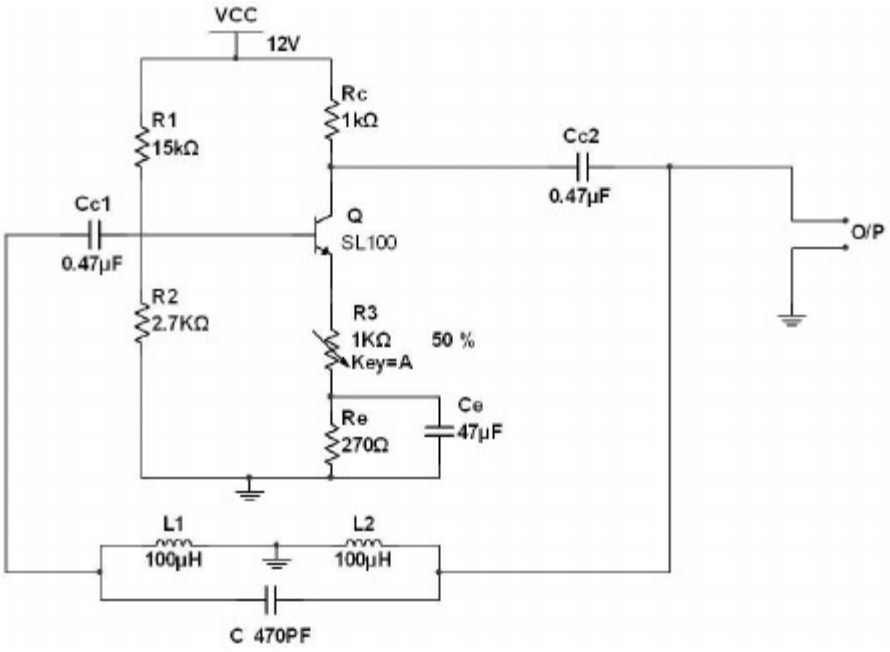
In the Hartley oscillator shown in Figure. Z1, and Z2 are inductors and Z3 is a capacitor. The resistors R and R2 and RE provide the necessary DC bias to the transistor. CE is a bypass capacitor CC1 and CC2 are coupling capacitors. The feedback network consisting of inductors L1 and L2, Capacitor C determine the frequency of the oscillator.

When the supply voltage +Vcc is switched ON, a transient current is produced in the tank circuit, and consequently damped harmonic oscillations are setup in the circuit. The current in tank circuit produces AC voltages across L1 and L2. As terminal 3 is earthed, it will be at zero potential.

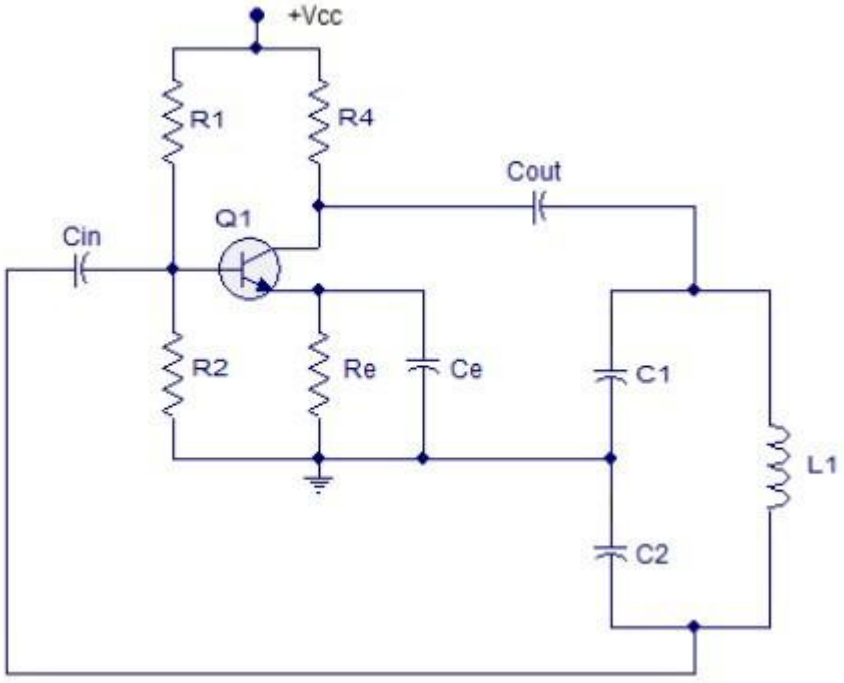
If terminal is at positive potential with respect to 3 at any instant, then terminal 2 will be at negative potential with respect to 3 at the same instant. Thus the phase difference between the terminals 1 and 2 is always 180. In the CE mode, the transistor provides the phase difference of 180 between the input and output. Therefore the total phase shift is 360. The frequency of oscillations is $f = 1/2\pi\sqrt{LC}$ where L= L1 + L2.

Circuit Diagram

Hartley Oscillator



Culprits Oscillator



Design

Given data

V_{CC}=12V ; I_C=4.5 mA; V_E=1.2 V ; V_{CE}=6 V ; h_{FE}=100.

Given V_E = 1.2V. Therefore $R_E = V_E / I_E \approx V_E / I_C$ =266.67Ω; **R_E=270Ω**

Writing KVL for the Collector loop we get, $V_{CC} = I_C R_C + V_{CE} + V_E$

$R_C = (V_{CC} - V_{CE} - V_E) / I_C = (12-6-1.2)V/4mA = 1.06K\Omega$; **$R_C$= 1 KΩ**

$h_{FE} R_E = 10R_2$

Assume **R_2=2.7KΩ,**

$V_B = (V_{cc} \times R_2) / (R_1 + R_2)$

Hence R1 = 14.14 KΩ ; **R1 = 15 KΩ**

Use **C_{C1}= 0.47μF**

Use **C_{C2}= 0.47μF**

Use **C_E=47μF**

Hartley Oscillator

Oscillator Frequency$f = cL_{eq.} = L_1 + L_2$Assume f = 500 KHz. With $L_1 = L_2$ =100μH, we get $L_{eq.} = L_1 + L_2$ = 200μH $L_{eq}.C = 1/(2\pi f)^2 = (\pi)^{-2} \times 10^{-12}$

This gives C = {1/ $(\pi)_2$ x 200μH} pF ≈500pF

Use C = 470 pF

For this capacitance value ***f*= 518.6 KHz**

Colpitts Oscillator

Tank Circuit Design: $f = \dfrac{1}{2\pi\sqrt{LC_{eq}}}$ Where $C_{eq} = \dfrac{C_1 C_2}{C_1 + C_2}$

Given Oscillation frequency f=1 MHz

Assume C_1=C_2 = 470 pF ∴ C_{eq}= 235 pF =2.35

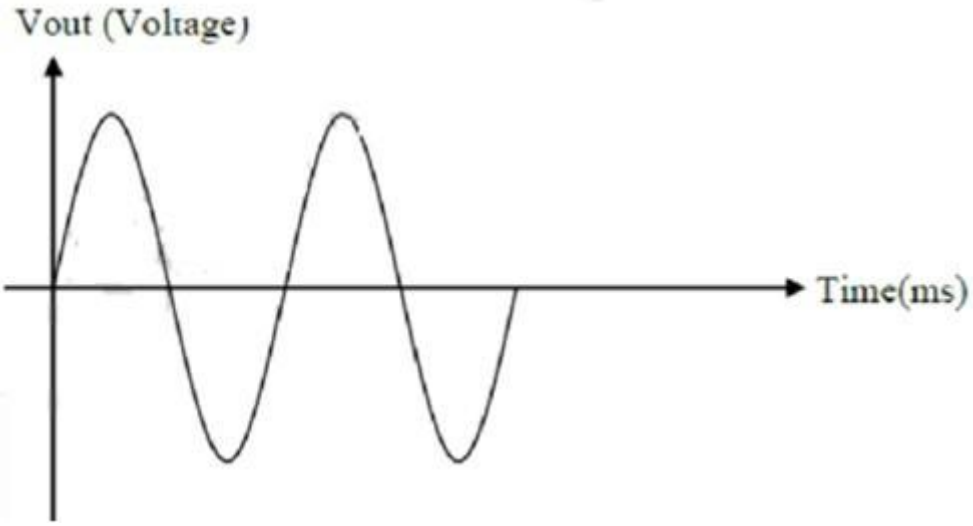
Then, $L = \dfrac{1}{4\pi^2 (f^2) C} = 119\ \mu H$

Use L = 100 μH, For this value of L, f= 1.04 MHz

Procedure

1. Connections are made as per the circuit diagram.
2. Switch on the Power Supply and check the D.C conditions by removing the coupling capacitor CC1 or CC2.
3. Connect the coupling capacitors and obtain an output waveform on the CRO. If the o/p is distorted vary 1- KΩ Potentiometer (R3) to get perfect SINE wave.
4. Measure the period of oscillation and calculate the frequency of oscillation.
5. Compare the measured frequency with re-computed theoretical value for the component values connected.

Model Wave



Observations

Hartley Oscillator

Sl No	Amplitude	Time	Frequency

Colpitts Oscillator

Sl No	Amplitude	Time	Frequency

Result

Thus oscillator is designed and constructed and the output sine wavefrequency is calculated.

Viva Questions

1. What is Hartley oscillator circuit?
2. What is Colpitts oscillator circuit?
3. What is the main function of biasing circuit?
4. Define Tank circuit?
5. What are the applications of Hartley oscillator?
6. State the advantage and disadvantage of Hartley Oscillator?
7. What is the purpose of bypass capacitor?
8. What are the applications of Colpitts oscillator?
9. State the advantage and disadvantage of Colpitts Oscillator.

8. Class-B Complementary-Symmetry Power Amplifier

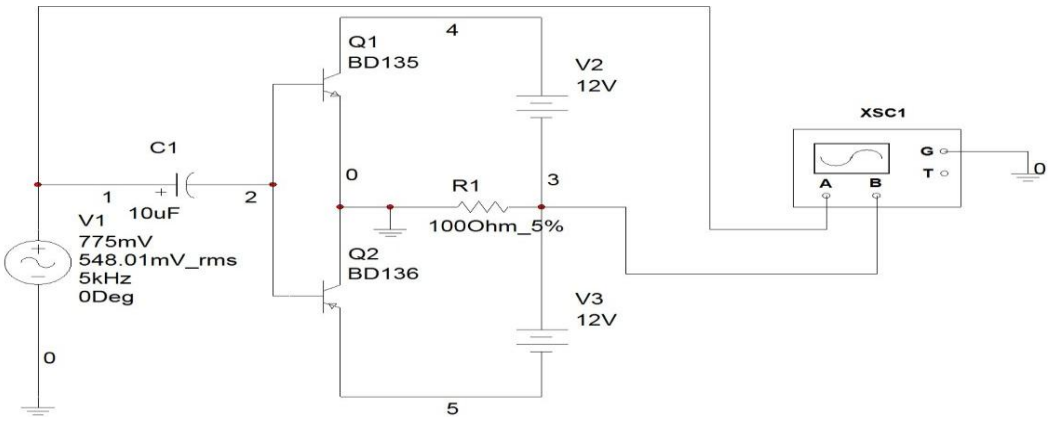
Aim:

To design a complementary-symmetry class-B push-pull power amplifier in order to achieve maximum output AC power and efficiency.

Apparatus

1. 1kΩ Resistor – 1No.
2. 220kΩ Resistor – 2No.
3. 18kΩ Resistor – 2 No
4. 1Ω Resistor – 2 No
5. 470Ω Resistor – 1No.
6. 10 μ F/ 25 V Capacitor – 2 No..
7. Transistors – BD 237(npn) – 1 No.
8. Transistors – BD 242C(pnp) – 1 No
9. CRO (Dual channel)
10. Regulated power supply
11. Function generator
12. Personal computer

Circuit Diagram:



Procedure:

1. Conncet the circuit s per the circuit diagram
2. Apply 4v p-p with 1KHZ frequency using function generator
3. Observe the output in CRO .
4. Note the cross over distortion in output.(outputVp-p)
5. Remove the collector connection and put ammeter.
6. Note the Idc value in the ammeter.
7. Using Pdc and Pac formulas find the efficiency.

Calculations:

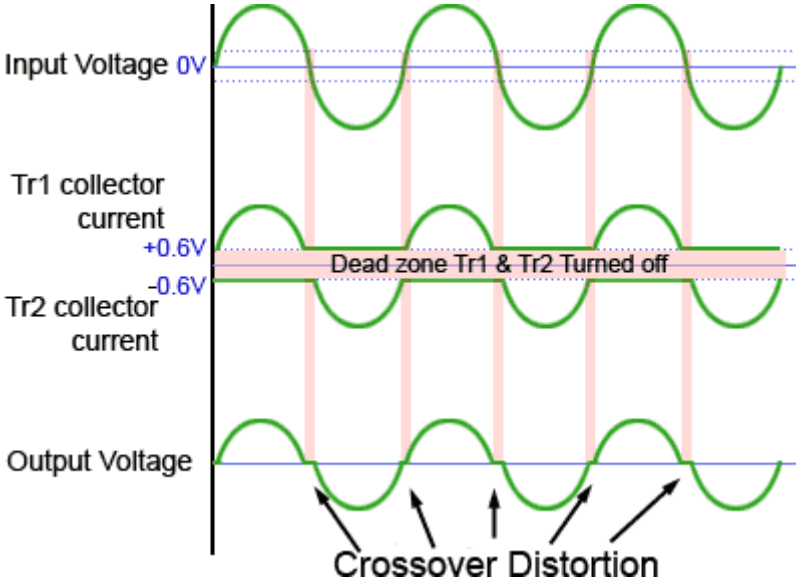
$P_{ac}=(V_p^2)/2R_C$

$P_{dc}=V_{cc}*I_c$

$\%Efficiency=\eta=(P_{ac}/P_{dc})*100$

$\%Efficiency=(V_o \square R_L)/(8R_L V_{cc} V_o).$

Expected Graph :



Result:

Thus the frequency response of a class B complementary symmetry power amplifier is designed and efficiency is calculated.

Viva Questions:

1. Differentiate between voltage amplifier and power amplifier?
2. Explain impedance matching provided by transformer?
3. Under what condition power dissipation is maximum for transistor in this circuit?
4. What is the maximum theoretical efficiency?
5. Sketch current waveform in each transistor with respective input signal?
6. How do you test matched transistors required for this circuit with DMM?
7. What is the theoretical efficiency of the complementary stage amplifier?
8. How do you measure DC and AC output of this amplifier?
9. Is this amplifier working in class A or B?
10. How can you reduce cross over distortion?

9.Class-A Power Amplifier

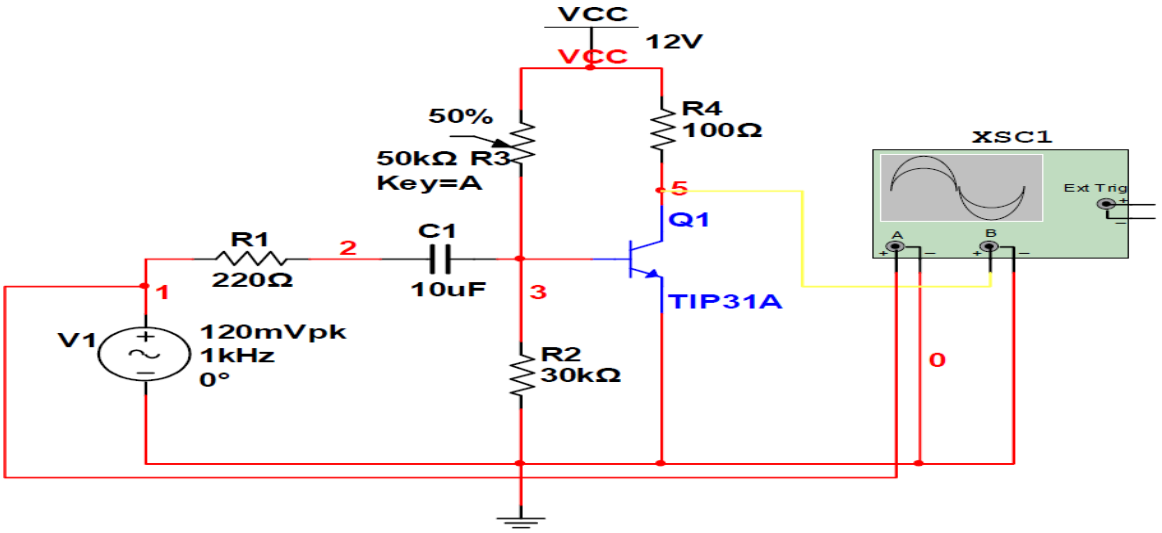
Aim:

To design a class-A power amplifier in order to achieve maximum output AC power and efficiency.

Apparatus

1. 1kΩ Resistor – 1No.
2. 220kΩ Resistor – 2No.
3. 18kΩ Resistor – 2 No
4. 1Ω Resistor – 2 No
5. 470Ω Resistor – 1No.
6. 10 µ F/ 25 V Capacitor – 2 No..
7. Transistors – BD 237(npn) – 1 No.
8. Transistors – BD 242C(pnp) – 1 No
9. CRO (Dual channel)
10. Regulated power supply
11. Function generator
12. Personal computer

Circuit Diagram:



Procedure:

8. Conncet the circuit s per the circuit diagram
9. Apply 4v p-p with 1KHZ frequency using function generator
10. Observe the output in CRO .
11. Note the cross over distortion in output.(outputVp-p)
12. Remove the collector connection and put ammeter.

13. Note the Idc value in the ammeter.
14. Using Pdc and Pac formulas find the efficiency.

Calculations:

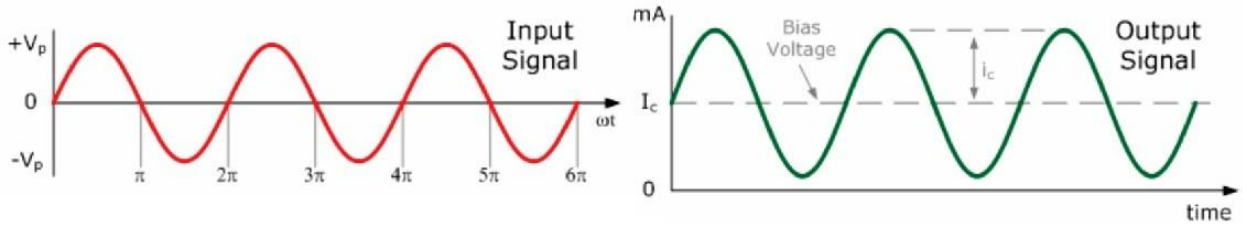
$P_{ac}=(V_p^2)/2R_C$

$P_{dc}=V_{cc}*I_c$

$\%Efficiency=\eta=(P_{ac}/P_{dc})*100$

$\%Efficiency=(V_o \square R_L)/(8 R_L V_{cc} V_o).$

Expected Graph :



Result:

Thus the frequency response of a class B complementary symmetry power amplifier is designed and efficiency is calculated.

Viva Questions:

1. Differentiate between voltage amplifier and power amplifier?
2. Explain impedance matching provided by transformer?
3. Under what condition power dissipation is maximum for transistor in this circuit?
4. What is the maximum theoretical efficiency?
5. Sketch current waveform in each transistor with respective input signal?
6. How do you test matched transistors required for this circuit with DMM?
7. What is the theoretical efficiency of the complementary stage amplifier?
8. How do you measure DC and AC output of this amplifier?
9. Is this amplifier working in class A or B?
10. How can you reduce cross over distortion?

10. Monostable Multi-vibrator

Aim

To design and construct monostable multi-vibrator using transistor and to plot the out put waveform.

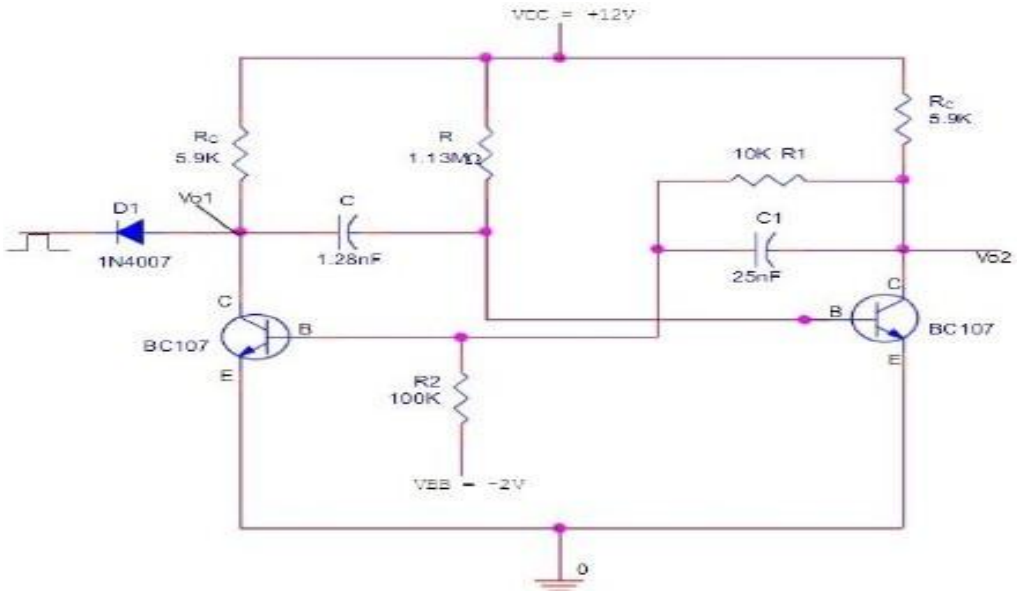
Apparatus Required

S.No	Apparatus	Specification	Quantity
1.	Power supply	(0-30V)	1
2.	CRO		1
3.	Resistor	4.9KΩ, 1.6MΩ	3
4.	Capacitor	0.45nF	2
5	Transistor	BC107	2
6	Connecting wires		

Theory

Monostable Multi-vibrator has two states which are (i) quasi-stable state and (ii) stable state. When a trigger input is given to the monostable Multi-vibrator, it switches between two states. It has resistor coupling with one transistor. The other transistor has capacitive coupling. The capacitor is used to increase the speed of switching. The resistor R2 is used to provide negative voltage to the base so that Q1 is OFF and Q2 is ON. Thus an output square wave is obtained from monostable multi-vibrator.

Circuit Diagram



Design

Given data

V_{CC}=12V , V_{BB}=−5 V , I_C=2mA , V_{CE} (Sat)=0.2 V , f =1 KHz , h_{fe}=100

$$R_C = \frac{V_{CC} - V_{CE(sat)}}{I_C}$$

$$I_{B2(\min)} = \frac{I_{C2}}{h_{fe}} =$$

$$Select\ I_{B2} > I_{B2(\min)}$$

$$I_{B2} =$$

$$R = \frac{V_{CC} - V_{BE(Sat)}}{I_{B2}}$$

$$T = 0.69RC$$

$$C = T/0.69R =$$

$$V_{B1} = \frac{-V_{BB}R_1}{R_1 + R_2} + \frac{V_{CE(Sat)}R_2}{R_1 + R_2}$$

$$\frac{-V_{BB}R_1}{R_1 + R_2} = \frac{V_{CE(Sat)}R_2}{R_1 + R_2}$$

(V_{B1} is very less)

$$V_{BB}R_1 = V_{CE(Sat)}R_2$$

$$R_2 = 10R_1$$

Let $R_1 = 10K\Omega$, then $R_2 = 100K\Omega$

Choose C1 = 25pF.

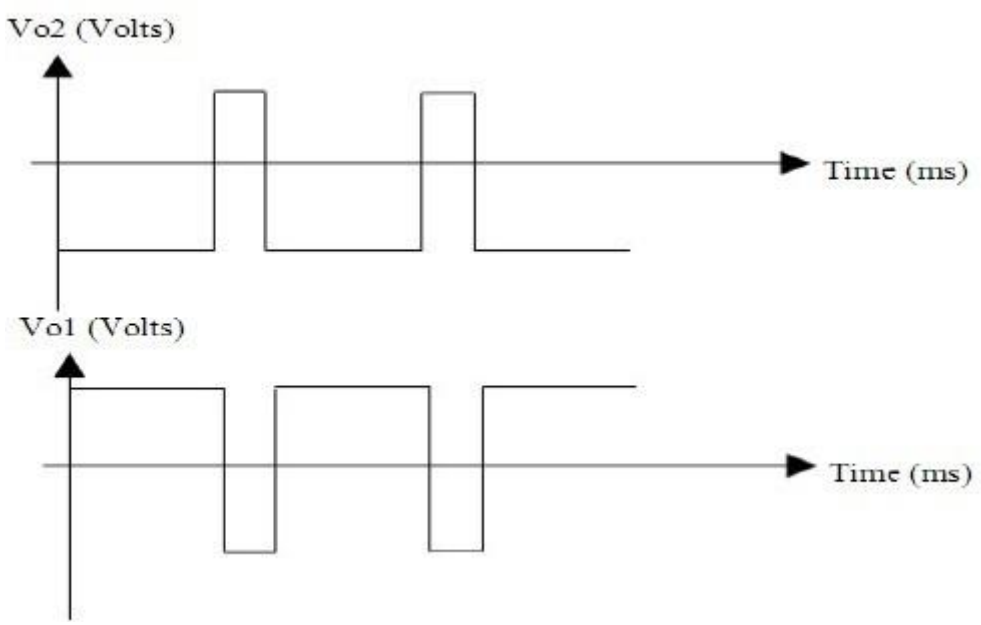
Procedure

1. Connect the circuit as shown in the circuit diagram.
2. Switch on the power supply.
3. Set the input trigger using trigger pulse generator.
4. Observe the output waveform in CRO.

Observations

Width (ms)	V_{c1}			V_{c2}		
	$T_{ON}\,(ms)$	$T_{OFF}\,(ms)$	Voltage(V)	$T_{ON}\,(ms)$	$T_{OFF}\,(ms)$	Voltage(V)

Models Graphs



Result

Thus the bistable Multi-vibrator is designed and constructed using transistor and its out put waveform is plotted.

Viva Questions

1. Define duty-cycle.
2. Give methods for obtaining symmetrical square wave.
3. Why monostable multi-vibrator is called one-shot vibrator?
4. What are the other names of monostable multi-vibrator?
5. Why monostable multi-vibrator is called gating circuit?
6. What is the difference between a retriggerable one shot and a non retriggerable one shot?

11.Bistable Multi-vibrator

Aim

To design and construct monostable multi-vibrator using transistor and to plot the out put waveform.

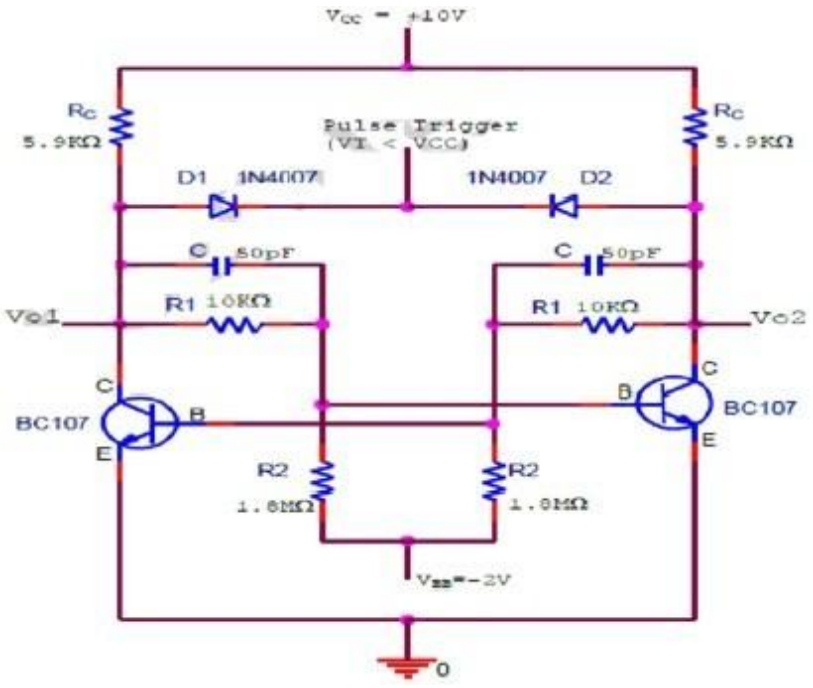
Apparatus Required

S.No	Apparatus	Specification	Quantity
1.	Power supply	(0-30V)	1
2.	CRO		1
3.	Resistor	4.9KΩ, 1.6MΩ	3
4.	Capacitor	0.45nF	2
5	Transistor	BC107	2
6	Connecting wires		

Theory

The bistable multi-vibrator has two stable states. The multi-vibrator can exist indefinitely in either of the two stable states. It requires an external trigger pulse to change from one stable state to another. The circuit remains in one stable state until an external trigger pulse is applied. The bistable multi-vibrator is used for the performance of many digital operations such as counting and storing of binary information. The multi-vibrator also finds an applications in generation and pulse type waveform.

Circuit Diagram



Design

Frequency of oscillator F=1//2πRC.

Assume C and find R to prevent loading of the amplifier by RC network R1≤10R.

Given data

$V_{CC}=12V$, $V_{BB}=-5\,V$, $I_C=2mA$, $V_{CE}(Sat)=0.2\,V$, $V_{BE}(Sat)=0.7\,V$, $h_{fe}=315$

$$R_C=\frac{V_{CC}-V_{CE(sat)}}{I_C}=5.9\,K\,\Omega$$

$R \leq h_{fe}\,R_C$

R = 1.8MΩ.

Let R1 = 10KΩ, C1 = C2 = 50pF

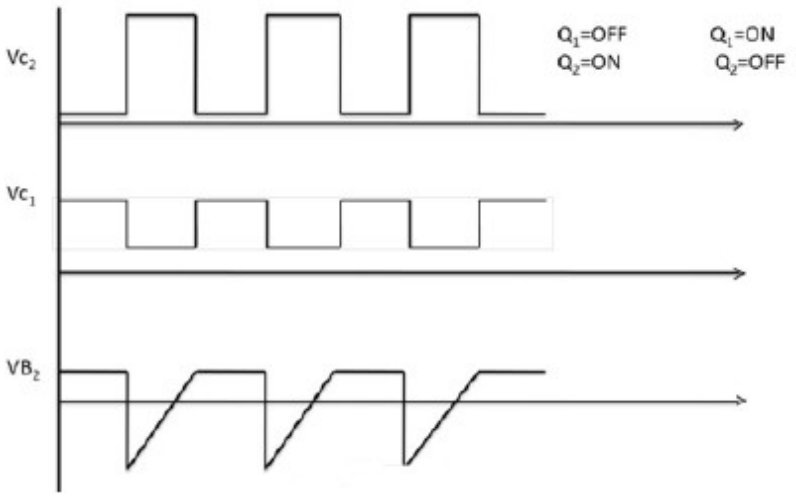
Procedure

5. Connect the circuit as shown in the circuit diagram.
6. Switch on the power supply.
7. Set the input trigger using trigger pulse generator.
8. Observe the output waveform in CRO.

Observations

Width (ms)	V_{c1}			V_{c2}		
	$T_{ON}(ms)$	$T_{OFF}(ms)$	Voltage(V)	$T_{ON}(ms)$	$T_{OFF}(ms)$	Voltage(V)

Models Graphs



Result

Thus the bistable Multi-vibrator is designed and constructed using transistor and its out put waveform is plotted.

Viva Questions

1. Why astable multi-vibrator is called a free-running oscillator?
2. Explain the function rest.
3. Define the term duty cycle.
4. Why does one of the transistors start conducting ahead of other?
5. What finally decides the shape of the waveform for bistable multi-vibrator?
6. What happened if positive pulse is given to a transistor in bistable multi-vibrator?

12. Astable Multi-vibrator

Aim

1. To study the operation and observe the wave forms of Astable Multi-vibrator.
2. To Design an Astable Multi-vibrator to generate a square wave of 1KHz frequency using Transistor.

Apparatus Required

1.	CRO 0 to 20 MHz (Dual Channel)	1 No.
2.	Function Generator 1Hz to 1 MHz	1 No.
3.	Bread board	1 No.
4.	Resistor (1K, 10K)	2 Nos. each
5.	Capacitors (0.1μF)	2 No.'s
6.	Transistor (BC 107)	2 No.'s
7.	Regulated DC Power Supply 0 to 30V (Dual)	1 No.
8.	Connecting wires	
9.	Bread board	

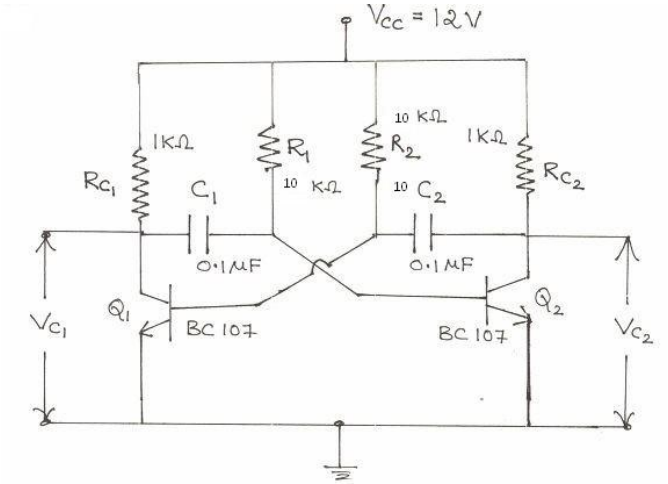
Theory

The bistable multi-vibrator has two stable states. The multi-vibrator can exist indefinitely in either of the two stable states. It requires an external trigger pulse to change from one stable state to another. The circuit remains in one stable state until an external trigger pulse is applied. The bistable multi-vibrator is used for the performance of many digital operations such as counting and storing of binary information. The multi-vibrator also finds an applications in generation and pulse type waveform.

When the power is applied, due to some imbalance in the circuit, the transistor Q2 conducts more than Q1 i.e. current flowing through transistor Q2 is more than the current flowing in transistor Q1. The voltage VC2 drops. This drop is coupled by the capacitor C1 to the base by Q1 there by reducing its forward base-emitter voltage and causing Q1 to conduct less. As the current through Q1 decreases, VC1 rises. This rise is coupled by the capacitor C2 to the base of Q2. There by increasing its base- emitter forward bias. This Q2 conducts more and more and Q1 conducts less and less, each action reinforcing the other. Ultimately Q2 gets saturated and becomes fully ON and Q1 becomes OFF. During this time C1 has been charging towards VCC exponentially with a time constant T1 = R1C1. The polarity of C1 should be such that it should supply voltage to the base of Q1. When C1 gains sufficient voltage, it drives Q1 ON.

Then VC1 decreases and makes Q2 OFF. VC2 increases and makes Q1 fully saturated. During this time C2 has been charging through VCC, R2, C2 and Q2 with a time constant T2 = R2C2. The polarity of C2 should be such that it should supply voltage to the base of Q2. When C2 gains sufficient voltage, it drives Q2 On, and the process repeats.

Circuit Diagram



Design

The period T is given by

T = T1 + T2 = 0.69 (R1C1 + R2C2)

For symmetrical circuit, with R1 = R2 = R & C1 = C2 = C

T = 1.38 RC

Let VCC = 12V; hfe = 51 (for BC107), VBESat = 0.7V; VCE Sat = 0.3V Let C = 0.1F & T = 1mSec.

10-3 = 1.38 x R X 0.1 X 10-6

R = 7.24K (Practically choose 10K) i.e., R1 and R2 resistors.

Let ICmax=10mA

RC = = 1.17K (1K is selected for Rc1 and Rc2)

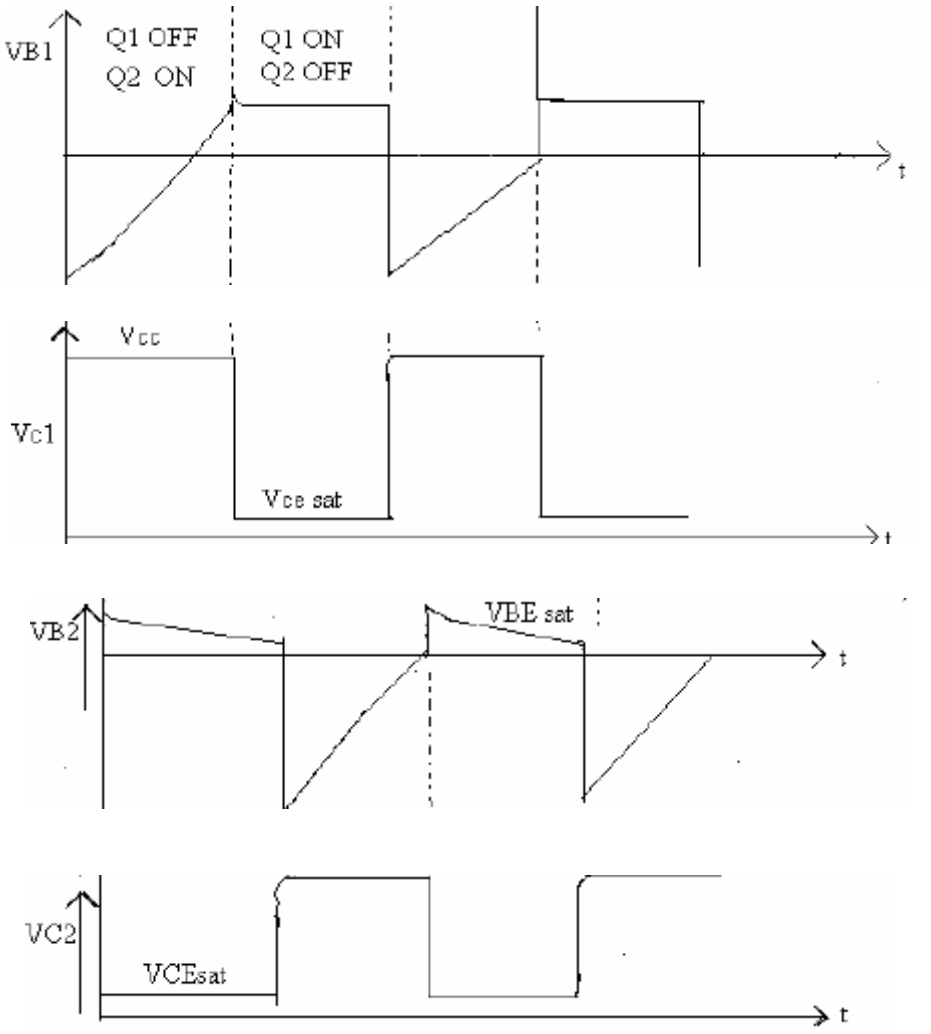
Procedure

1. Make then connections as per the circuit diagram.
2. Observe the Base Voltage and Collector Voltages of Q1 & Q2 on CRO in DC mode and measure the frequency (f = 1/T).
3. Trace the waveforms at collector and base as each transistor with the help of dual trace CRO and plot the waveforms.
4. Verify the practical output frequency with theoretical values f = 1/T, where T = 1.38 RC

Observations

Width (ms)	V_{c1}			V_{c2}		
	$T_{ON}(ms)$	$T_{OFF}(ms)$	Voltage(V)	$T_{ON}(ms)$	$T_{OFF}(ms)$	Voltage(V)

Models Graphs



Theoretical calculations:

F = 1/ T = (1/1.38RC)

R = 10KΩ, C = 0.1μF

Result

An Astable Multi-vibrator is designed; the waveforms are observed and verified the results theoretically.

Viva Questions

1. What are the other names of Astable Multi-vibrator?
2. Define quasi stable state?
3. Is it possible to change time period of the waveform with out changing R & C?
4. Why Astable Multi-vibrator is called free running oscillator?
5. Explain charging and discharging of capacitors in an Astable Multi-vibrator?
6. How can an Astable Multi-vibrator be used as VCO?
7. What are symmetrical triggering and unsymmetrical triggering?
8. What are the applications of Astable Multi-vibrator?
9. How can Astable Multi-vibrator be used as a voltage to frequency converter?
10. Which Multi-vibrator has two quasi-stable states?
11. What is the formula for frequency of oscillations? Design R and C for a frequency of 2KHz of a symmetric Astable oscillator.
12. What is duty cycle?

13. Schmitt Trigger

Aim

1. To design the circuit of Schmitt trigger with UTP=2.2V and LTP=1V.
2. To obtain square wave from sine wave.
3. To obtain UTP and LTP values practically

Apparatus Required

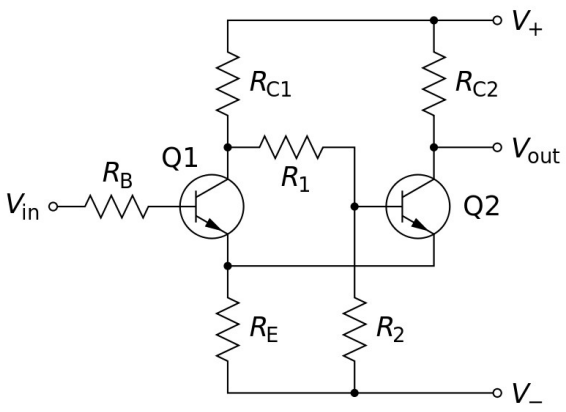
1. CRO 0 to 20 MHz (Dual Channel)	1 No.
2. Function Generator 1Hz to 1 MHz	1 No.
3. Bread board	1 No.
4. Resistor (1KΩ, 2.3KΩ,330Ω)	2 Nos Each
5. Resistor (1.2KΩ)	3 Nos
6. Capacitors (0.1μF)	2 Nos
7. Transistor (BC 107)	2 Nos
8. Regulated DC Power Supply 0 to 30V (Dual)	1 No.
9. Connecting wires	
10. Bread board	

Theory

In digital circuits fast waveforms are required i.e, the circuit remain in the active region for a very short time (of the order of nano seconds) to eliminate the effects of noise or undesired parasitic oscillations causing malfunctions of the circuit. Also if therise time of the input waveform is long, it requires a large coupling capacitor. Therefore circuits which can convert a slow changing waveform (long rise time) in to a fast changing waveform (small rise time) are required. The circuit which performs this operation is known as “Schmitt Trigger”.

In Schmitt trigger circuit, the output is in one of the two levels namely low or high. When the input voltage is raising above the UTP (upper threshold point) i.e. V1, the output changes to high level. Similarly when a falling output voltage passes through a voltage V2 known as lower threshold point (LTP), the output changes to low. The level of the output changes V1 is always greater than V2.The differences of these two voltages is known as “Hysteresis”.

Circuit Diagram



Design

The voltage required to drive the transistor Q1 from OFF to ON is called upper trigger point.

UTP = V1 = V1 — 0.1

Where V1 = V = (VCCR2)/ (R1+R2+RC1)

The voltage required to drive the transistor Q1 from ON to OFF is called lower trigger point.

LTP = V2= VBE(active)+ (V1-Vc2)Re/(aRcth+Re)

Where Rcth =(RC1(R1+R2))/(R1+R2+RC1)

a =R2/(R1+R2)

Choose BC107 transistor with hfe= 200

Let Vcc=12V, R1=2.2Kohms , R2=1.2Kohms

Set UTP = V1 — 0.1 then 2.2= V1 — 0.1 then V1= 2.3V

But V1= (12X15)/(2.2+1.5+RC1)

RC1= 4.12Kohms = 4Kohms

Rcth = (4X 103(2.2+1.5))/(2.1+1.2+4.4K) = 1.97Kohms

a= 0.3529

LTP =V2= VBE(active)+ (V1-V?2) .Re/(aRcth+Re)

= 0.7+(2.3-0.6).330/(0.35X1.97K+330)

= 1.21V

VE=V1-VBE= 2.3-0.7 = 1.6V

IB2= VE/RE(1+hfe) = 1.6/330(1+200) = 0.0030A

IC2 = hfeIB2 =0.6V

When Vin < V2, output =1

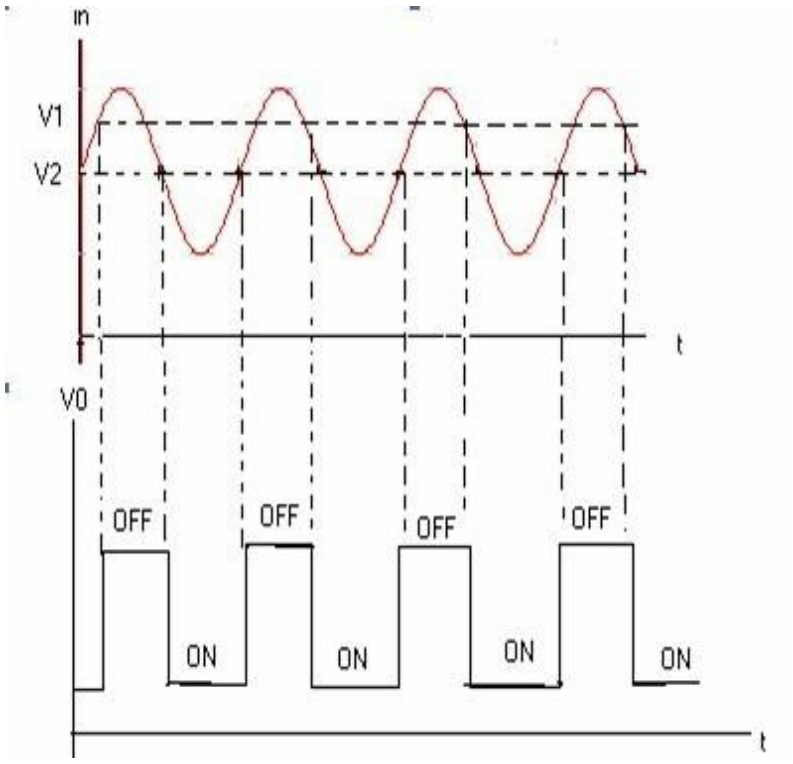
(VC-output)/IC2 = RC2

(12-1)/0.6 = RC2= 18.33%u2126

Procedure

1. Connect the circuit diagram as shown in circuit diagram.
2. Apply a sine wave input of 15 Vp-p amplitude and 1 KHz frequency to thecircuit
3. Observe the output voltage on CRO.
4. Obtain the output voltage at which LOW to HIGH transition occurs and measure the corresponding input voltage. This input voltage is called UTP (Upper threshold point)
5. Now, Obtain the output voltage at which HIGH to LOW transition occurs and measure the corresponding input voltage. This input voltage is called LTP (Lower threshold point).
6. Compare these practical values with theoretical values.

Models Graphs



Result

Schmitt trigger circuit with the given values is designed; and the response is observed.

Viva Questions

1. What is Schmitt Trigger?
2. What are the applications of Schmitt Trigger?
3. Define hysteresis action?
4. Why Schmitt Trigger is called a squaring circuit?
5. Define UTP? Write its expression.
6. Define LTP? Write its expression.
7. What is the difference between a Binary and Schmitt Trigger?
8. How noise can be eliminated on a given signal using Schmitt Trigger?
9. Explain how a Schmitt Trigger converts a sine wave to a square wave?
10. A Schmitt trigger exhibits hysteresis when loop gain is____.

14. Bootstrap Sweep Circuit

Aim

1. To design a Boot-strap Sweep Circuit.
2. To obtain a sweep wave form.

Apparatus Required

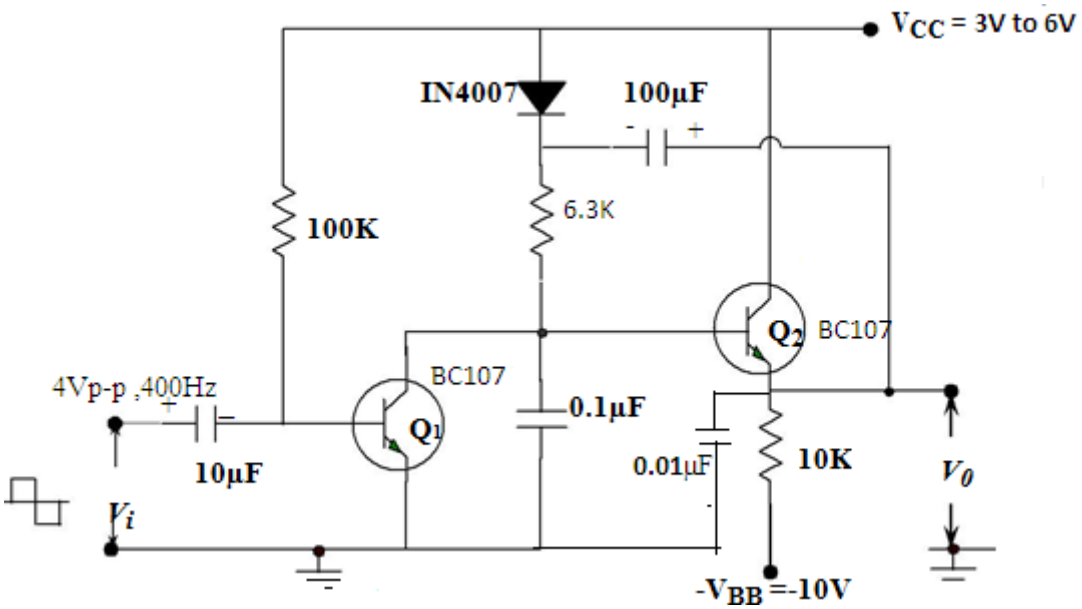
1.	CRO 0 to 20 MHz (Dual Channel)	1 No.
2.	Function Generator 1Hz to 1 MHz	1 No.
3.	Bread board	1 No.
4.	Resistor (5.6KΩ, 10KΩ,100KΩ)	2 Nos Each
5.	Resistor (1.2KΩ)	3 Nos
6.	Capacitors (0.1μF, 10μF, 100μF)	2 Nos
7.	Transistor (BC 107)	2 Nos
8.	IN4007 Diode – 1 No.	1No
9.	Regulated DC Power Supply 0 to 30V (Dual)	1 No.
10.	Connecting wires	
11.	Bread board	

Theory

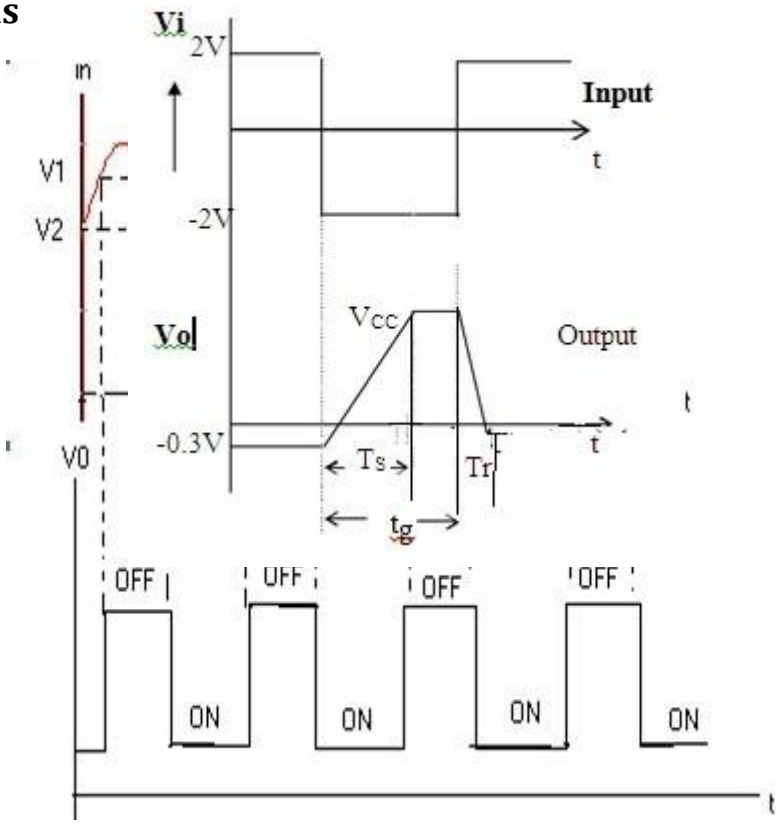
The input to Q1 is the gating waveform. Before the application of the gating waveform, at t = 0, transistor Q1 is in saturation. The voltage across the capacitor C and at the base of Q2 is VCE(sat). To ensure Q1 to be in saturation for t = 0, it is necessary that its current be at least equal to ICE / hFE so that Rb < hfeR.

With the application of the gating waveform at t = 0, Q1 is driven OFF. The current IC1 now flow into C and assuming unity gain in the emitter follower V0. When the sweep starts, the diode is reverse biased, as already explained above, the current through R is supplied by C1. The current VCC / R through C and R now flows from base to emitter of Q2.if the output V0 reaches the voltage VCC in a time TS / Tg, then from above we have TS = RC.

Circuit Diagram



Models Graphs



Result

Boot strap sweep circuit with the given values is designed; and the response is observed.

Viva Questions

1. Define (a) Voltage time base generator, (b) current time base generator (c) linear time base generator.
2. What is the relation between the slope error, displacement error and transmission error?
3. What are the various methods of generating time base wave-form?
4. Which amplifier is used in Boot-strap time base generator?
5. Which type of sweep does a bootstrap time-base generator produce?
6. What is the gain of the amplifier used in Bootstrap time base generator?
7. What is retrace time? Write the formula for the same for Bootstrap time base generator.
8. What is the formula for sweep amplitude in Bootstrap time base generator?
9. To have less flatness time of sweep signal, then the gate signal time has to be __.
10. A Bootstrap sweep circuit employs___type of feedback.