IC APPLICATIONS

NOTES

III BTECH, ECE

1ST SEMESTER(2022–23)

R20

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(UGC AUTONOMOUS)

Accredited by NAAC & NBA, Approved by AICTE, Permanently
Affiliated to JNTUH

Bhaskar Nagar, Yenkapally (v), Moinabad (m),

Hyderabad-500075, Telangana, India

AY 2020-21 Onwards	J. B. Institute of Engineering and Technology (UGC Autonomous)	B.Tech: ECE III Year – ISem			
Course Code: J314C	IC APPLICATIONS	L	T	P	D
Credits: 3		3	0	0	0

Syllabus

Pre-requisite: Electronic devices and circuits

Switching Theory & Logic Design, Pulse & Digital Circuits

Course Objectives:

1. To introduce the basic building blocks of linear integrated circuits.
2. To teach the linear and non – linear applications of operational amplifiers.
3. To introduce the theory and applications of analog multipliers and PLL.
4. To introduce the concepts of waveform generation and introduce some special function ICs.
5. To understand and implement the working of basic digital circuits

MODULE 1:

Unit 1: Introduction to Linear Integrated Circuits

Ideal and Practical Op-Amp, Op-Amp Characteristics, DC and AC Characteristics, Features of 741 Op-Amp, Modes of Operation - Inverting, Non-Inverting, Differential

Unit 2: Non-Linear Applications of OP-AMP

Instrumentation Amplifier, AC Amplifier, Differentiators and Integrators, Comparators, Schmitt Trigger, Introduction to Voltage Regulators, Features of 723 Regulator,
Three Terminal Voltage Regulators.

MODULE 2:

Unit 1: Introduction to IC-555 Applications

Introduction to Active Filters, Characteristics of Band pass, Band reject and All Pass Filters, Analysis of 1st order LPF & HPF Butterworth Filters, Waveform Generators – Triangular, Saw tooth, Square Wave, IC555 Timer -Functional Diagram, Monostable, and Astable Operations, Applications.

Applications

IC565 PLL – Block Schematic, Description of Individual Blocks, Applications.

UNIT-1

Integrated circuits and operational Amplifier

Definition of IC : The Integrated circuit (or) IC is a miniature, low cost electronic circuit consisting of active and passive components that are inseparably joined together on a single crystal chip of silicon.

Advantages of IC's :

1. Miniaturization and hence increased equipment density
2. Cost reduction due to batch processing
3. Increased system reliability due to elimination of soldered joints
4. Improved functional performance
5. Increased operating speeds
6. Reduction in power consumption.

Classification of IC's :

I **Based on mode of operation :**

a) Digital IC's b) Linear IC's

a) **Digital IC's :** Digital IC's are complete functioning logic networks that are equivalents of basic transistor logic circuits.

Ex : Gates, counters, multiplexers, demultiplexers, shift registers.

Linear Ic's: Linear Ic's are equivalents of discrete transistor networks, such as amplifiers, filters, frequency multipliers and modulators that often require additional external components for satisfactory operation.

Ex: op-Amps

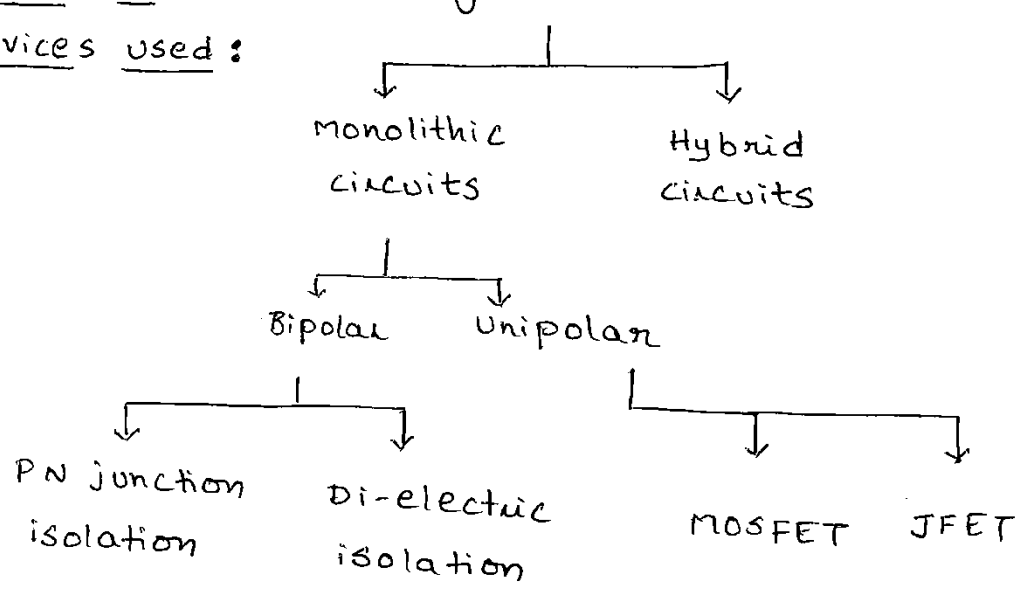
II Based on Fabrication

a) Monolithic Ic's b) Hybrid Ic's

a) Monolithic Ic's: In monolithic Ic's all components (active and passive) are formed simultaneously by a diffusion process. then a metallization process is used in interconnecting these components to form the desired circuit.

b) Hybrid Ic's: In Hybrid Ic's, passive components (such as resistors and capacitors) and the interconnections between them are formed on an insulating substrate. the substrate is used as a chassis for the integrated components. Active components such as transistors and diodes as well as monolithic integrated circuits, are then connected to form a complete circuit.

(iii) Based on devices used:



IC chip size and circuit complexity:

The concept of IC was introduced at the begining of 1960 by both Texas instruments and Fairchild Semi Conductors. Since that time, the size and complexity of IC's have increased rapidly as shown by the brief chronology.

1. Invention of Transistor		1947
2. Development of Si Transistor		1955 - 1959
3. Si planar Technology	junction transistor diode	1959
4. First IC, small scale integration	3 to 30 gates/chip approx. (or) 100 transistors / chip (Logic Gates, Flipflops)	1960 - 65

5. Medium scale Integration (MSI)	30 to 300 gates/chip (or) 100 to 1000 transistors per chip. (counters, MUX's, Adders)	1965 - 1970
6. Large scale Integration (LSI)	300 to 3000 gates/chip (or) 1000 to 20000 transistors per chip (8 bit µP's, ROM, RAM)	1970 - 1980
7. Very large scale Integration (VLSI)	More than 3000 gates/chip (or) 20,000 - 1000000 transistors/Chip (16 and 32 bit µP's)	1980 - 1990
8. Ultra large scale integration (ULSI)	10^6 to 10^7 transistors/chip (special procesors, virtual reality machines, smart sensors)	1990 - 2000
9. Giant - scale Integration	> 10^7 transistors/chip	

Manufacturers Designations for integrated circuits

Each manufacturer uses a specific code and assigns a specific type number to the IC's it produces. That is, each manufacturer uses its own identifying initials followed by its own type number.

For example, the 741 type of internally compensated op-Amp was originally manufactured by Fairchild and is sold as the μA741, where μA represents the identifying initials used by fairchild. Initials used by some of the well known manufacturers of Linear IC's are as follows

Fairchild	: μA, μAF
National Semiconductor	: LM, LH, LF, TBA
Motorola	: MC, MFC
Texas instruments	: SN
RCA	: CA, CD
signetics	: N/S, NE/SE, SU
Burr Brown	: BB

Fairchild's original μA741 is also manufactured by various other manufacturers under their own designations, as follows.

National semiconductor	LM741
Motorola	MC1741
RCA	CA3741
Texas Instruments	SN52741
Signetics	N5741.

Temperature ranges of Ic's :

All Ic's manufactured fall in to one of the three basic temperature grades.

1. Military temperature range $-55^{\circ}c$ to $125^{\circ}c$
2. Industrial temperature range $-20^{\circ}c$ to $+85^{\circ}c$
3. Commercial temperature range $0^{\circ}c$ to $+70^{\circ}c$.

Applications of IC

Ic's have become a vital part of modern electronic circuit design. They are used in

1. Computer Industry
2. Automobile Industry
3. Home appliances
4. Communication
5. Control systems

where they permit miniaturization and superior performance not possible with discrete components.

OPERATIONAL AMPLIFIER (OP-AMP)

* An Important Linear IC is operational Amplifier.
* The operational Amplifier is a multi terminal device which internally is quite complex.
* OP-Amp is a direct coupled high gain Amplifier
* OP-Amp can be used to amplify both a.c and d.c signals.
* It is used to perform a Variety of mathemati-cal operations such as Addition, subtraction, log, Antilog, Differentiation, Integration etc. Hence the Due to its use in perforning mathematical operations, it has been given a name 'operational Amplifier'
* Earlier op-Amps were designed by using Vaccum tubes, Hence the op-Amps were bulky, power consuming and expensive.
* Between 1964 to 1968 the popular 741 integrated circuit op-Amp was introduced by Robert.j.widlar
* The IC version of op-Amp uses BJT's and FET's which are fabricated along with the other supporting components on a single semiconductor chip.

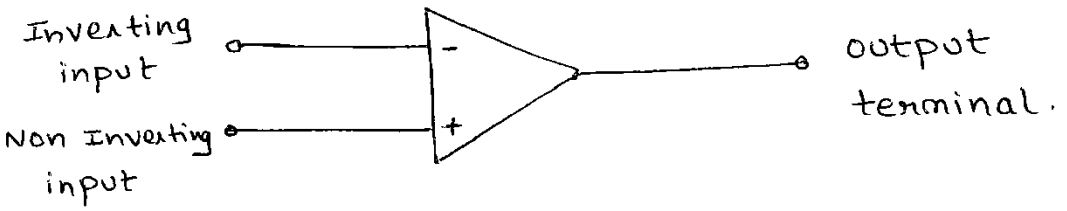
Advantages: Low cost, small size, Versatile, flexible

Applications :

Communications, computers, power and signal sources, process control, displays and measuring systems.

Op-Amp Symbol and Terminals :

Op-Amp symbol : The circuit schematic of an Op-Amp is a triangle as shown in figure below. It has two input terminals and one output terminal



Packages :

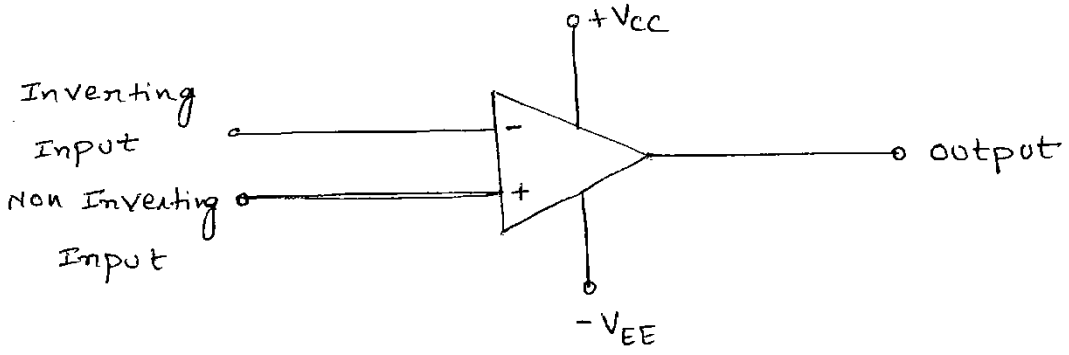
There are three popular packages available

1. The metal can (TO) package
2. The flat package (or) flat pack
3. the dual-in-line package (DIP)

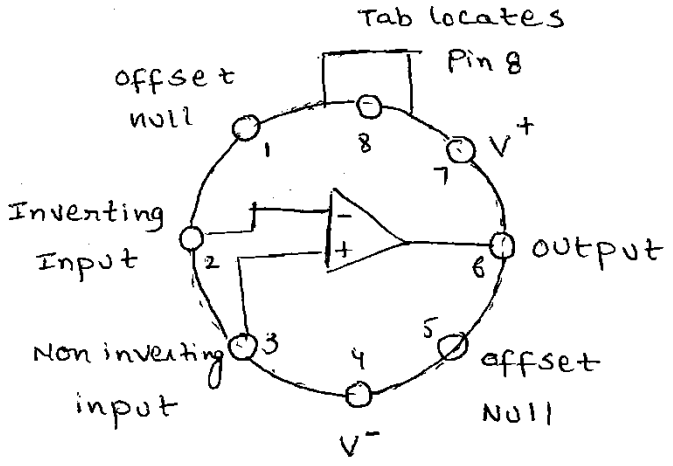
Op-Amp Terminals :

Op-Amps have five basic terminals, that is

1. Two input terminals
2. one output terminal
3. Two power supply terminals.

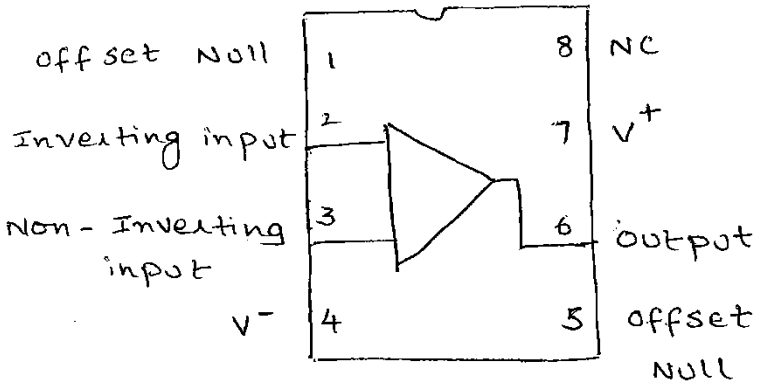


The IC 741 8-Pin Metal Can is shown in figure below.



Fig(a): 8 Pin Metal can

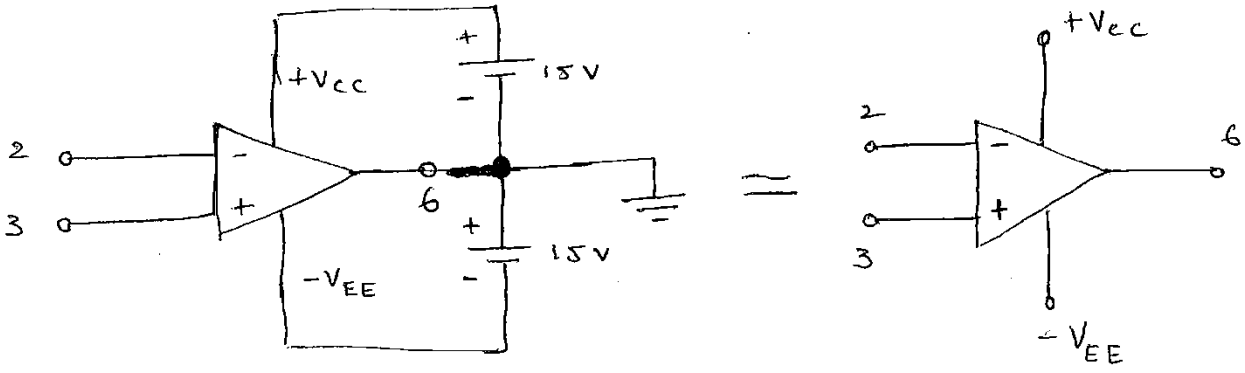
The IC 741, 8 Pin Mini DIP is shown in figure(b) below.



(b) 8-Pin Mini DIP

Power Supply connections:

The $+V_{CC}$ and $-V_{EE}$ power supply terminals are connected to two dc voltage Sources. The $+V_{CC}$ is connected to the positive terminal of one source and $-V_{EE}$ is connected to the negative terminal of other source. where the two sources are 15 V batteries each. These are typical values, but in general, the power supply voltage may range from about ± 5 V to ± 22 V. the common terminal of $+V_{CC}$ and $-V_{EE}$ is connected to a reference point or ground.

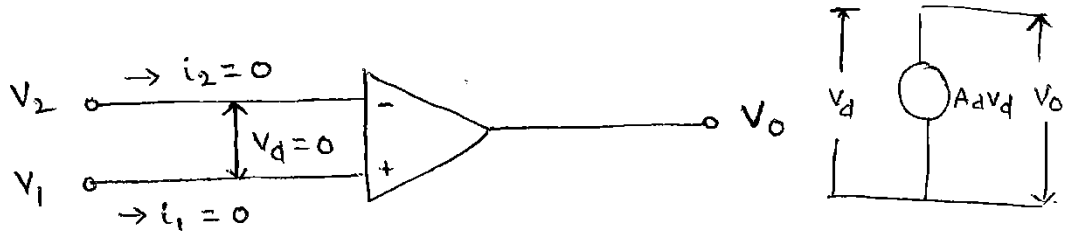


The Ideal operational Amplifier:

The schematic symbol of an op-Amp is shown in figure below. the - and + symbols at the input refer to inverting and non inverting input terminals respectively.

ie if $V_1 = 0$, output V_o is 180° out of phase with input signal V_2.

And when $V_2 = 0$. output V_o will be inphase with the input signal applied at V_1.



Fig(a): Ideal op-Amp

The op-Amp is said to be ideal if it has the following characteristics.

1. Infinite voltage gain $A_{OL} = \infty$

Since gain is ∞, the voltage between the inverting and non inverting terminals ie differential input voltage $V_d = V_1 - V_2$ is essentially zero for finite output voltage V_o.

$$A_{OL} = \frac{V_o}{V_d} = \infty \quad \Rightarrow \quad V_d = 0 = V_1 - V_2$$

2. Infinite input resistance $(R_i = \infty)$:

Because of infinite input resistance the ideal op-Amp draws no current at both the input terminals ie. $i_1 = i_2 = 0$. so that almost any signal source can drive it and there is no loading of the preceding stage.

3. zero output Resistance $[R_o = 0]$

so the output can drive an infinite number of other sources.

4. Infinite Band width $[BW = \infty]$

so that any frequency signal from 0 to ∞ Hz can be amplified with out attenuation

5. offset voltage $V_{of} = 0$

ie when $V_1 = V_2 = 0$, $V_o = 0$

6. common mode Rejection Ratio (CMRR) $= \infty$

7. slew rate (SR) $= \infty$

so the output voltage changes occur simultaneously with input voltage changes.

practical op-Amp [Equivalent circuit of op-Amp]:

The ideal op-Amp characteristics can never be realized in practice. There are practical op-Amps that can be made to approximate some of these characteristics using a negative feedback arrangement.

the physical Amplifier is not a ideal one so the characteristics of practical op-Amp are

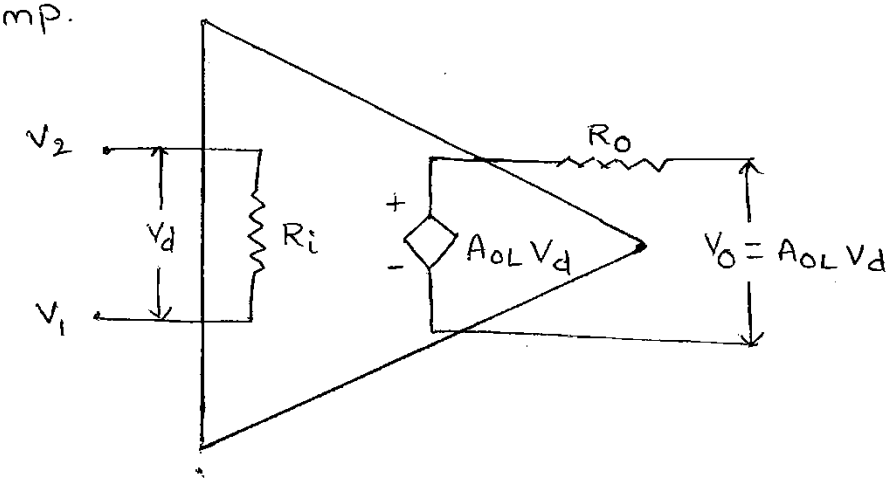
open loop voltage Gain $A_{OL} \neq \infty$

Input Impedance $R_i \neq \infty$

output Impedance $R_O \neq 0$

offset voltage V_{of} is finite if $V_1 = V_2 = 0$

Figure Below shows the equivalent circuit of an op-Amp.



For the above circuit $A_{OL} \neq \infty$, $R_i \neq \infty$ and $R_O \neq 0$. It can be seen that op-Amp voltage controlled voltage source and $A_{OL} V_d$ is an equivalent thevinin voltage Source and R_O is the thevinin equivalent resistance looking back in to the output terminal of an op-Amp.

The equivalent circuit is useful in analyzing the basic operating principles of op-Amps. For the above circuit, the output voltage is

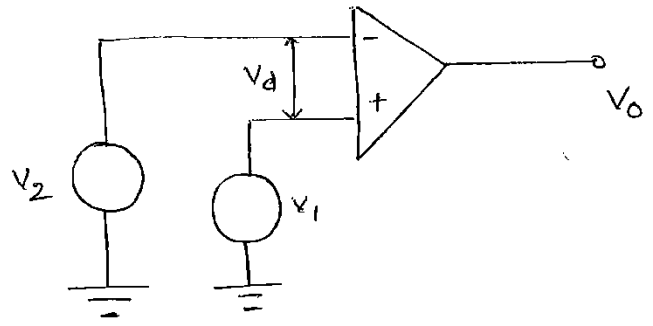
$$V_O = A_{OL} V_d$$

$$V_O = A_{OL} (V_1 - V_2)$$

The equation shows that the op-Amp amplifies the difference between the two input voltages.

open loop operation of op-Amp : (op-Amp without feedback)

The simplest way to use an op-Amp is in the open loop mode



Refer to the above figure, where signals V_1 and V_2 are applied at non inverting and inverting input terminals respectively.

Since the gain is infinite, the output voltage V_o is either at its positive saturation voltage ($+V_{sat}$) or negative saturation voltage.

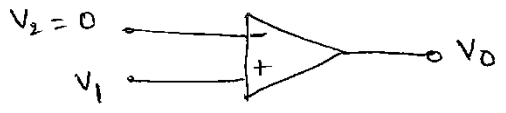
$$\text{If} \quad V_1 > V_2 \Rightarrow V_o = +V_{sat} \simeq +V_{cc}$$

$$V_1 < V_2 \Rightarrow V_o = -V_{sat} \simeq -V_{cc}$$

Here the output assumes one of the two possible output states, that is $+V_{sat}$ or $-V_{sat}$ and the amplifier acts as a switch only.

This has limited number of applications such as voltage comparator, zero Crossing detector etc. open loop op-Amps are not used in linear applications.

For practical op-Amp (open loop)



Assume $A_{OL} = 10^5$

$$V_o = A_{OL} V_d = A_{OL} (V_1 - V_2)$$

$$V_o = A_{OL} V_1$$

case 1:

If $V_1 = 1\,\mu V \Rightarrow V_o = 10^5 \times 10^{-6} = 0.1\,V$

case 2:

If $V_1 = 1\,mV \Rightarrow V_o = 10^5 \times 10^{-3} = 100\,V$

Consider case (2): output voltage 100 V is not possible, because output voltage cannot be greater than supply voltage. So output is saturated

$$\text{so} \quad V_o = +V_{sat} \simeq +V_{cc}$$

similarly If $V_1 = 0$

case 1: If $V_2 = 1\,\mu V \Rightarrow V_o = -A_{OL} V_2 = -0.1\,V$

case 2: If $V_2 = 1\,mV \Rightarrow V_o = -V_{sat} \simeq -V_{cc}$.

Open loop op-Amp configurations:

There are three open loop op-Amp configurations

1. Differential Amplifier
2. Inverting Amplifier
3. Non inverting Amplifier.

1. Differential Amplifier:

Figure shows the open loop differential Amplifier in which input signals V_{in1} and V_{in2} are applied to the positive and Negative input terminals.

since the Op-Amp amplifies the difference between the two input signals, this configuration is called the differential amplifier.

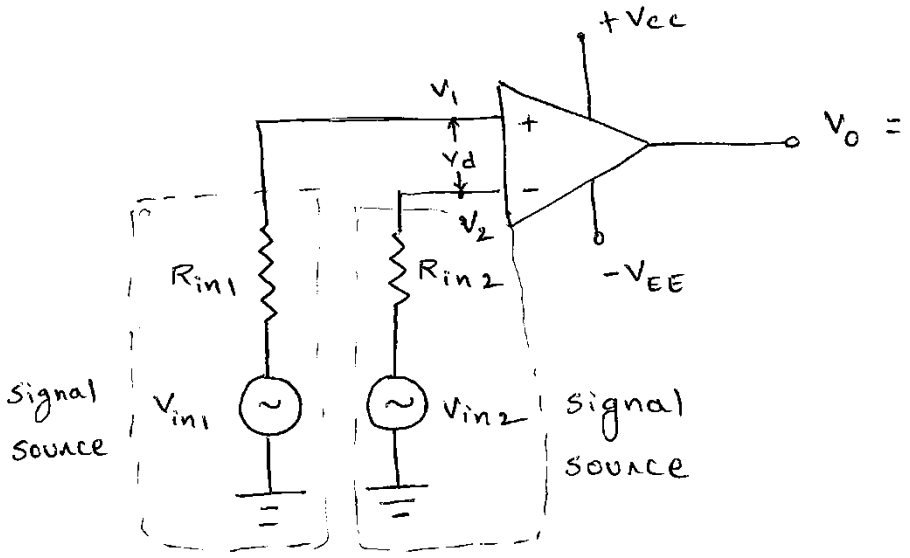


Fig: open loop differential Amplifier

$$V_o = A\, V_d$$

$$V_o = A\,(V_1 - V_2)$$

R_{in1}, R_{in2} are negligible compared to the input resistance (R_i) of the op-Amp

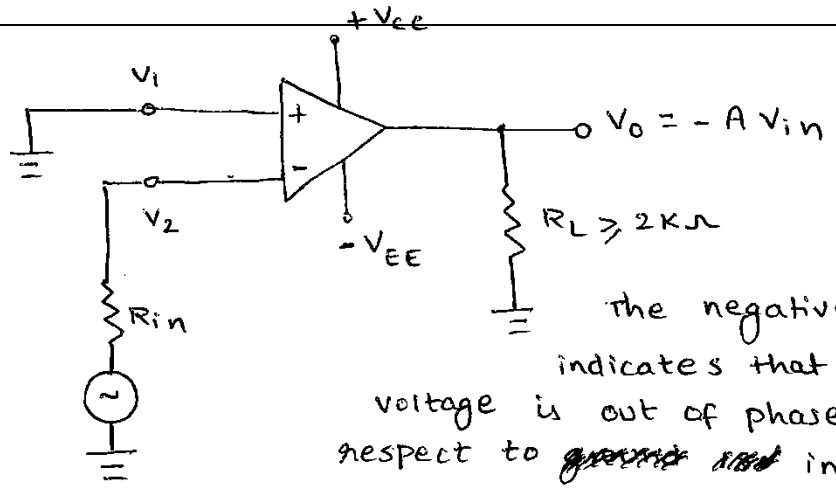
so $V_{in1} = V_1$, $V_{in2} = V_2$

$$\therefore \quad V_o = A\,(V_{in1} - V_{in2})$$

② Inverting Amplifier:

Here $V_{in} = 0$, $V_2 = V_{in}$

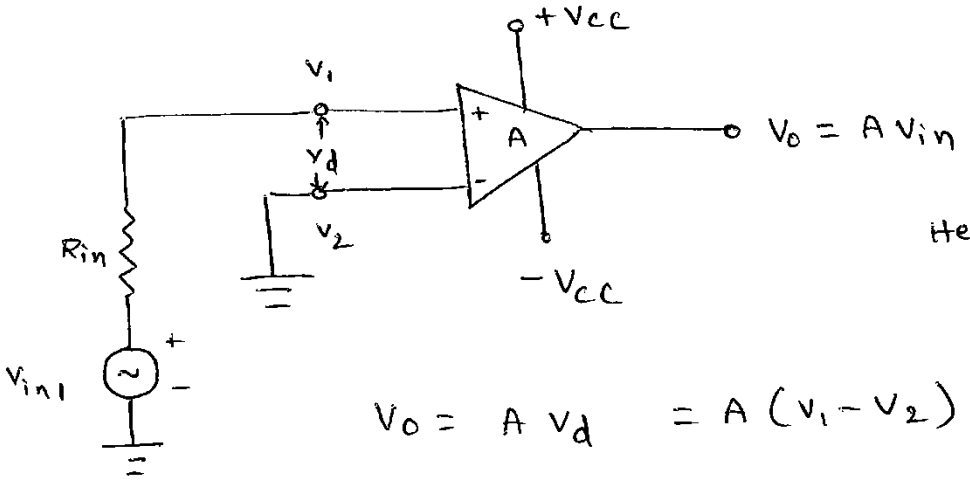
$$V_o = A\, V_d = A\,(V_1 - V_2) = -A\, V_{in}.$$



the negative sign indicates that the output voltage is out of phase with respect to ~~ground~~ ~~1800~~ input by 180°

Fig: open loop Inverting Amplifier

3) Non Inverting Amplifier:



Here $V_1 = V_{in}$

$V_2 = 0$

$$V_o = A V_d = A (V_1 - V_2)$$

$$V_o = A V_1 = A V_{in}$$

output voltage is inphase with the input voltage

Problem:

Determine the output voltage in each of the following cases for the open loop differential amplifier shown in figure above.

a) $V_{in1} = 5\mu V$ dc , $V_{in2} = -7\mu V$ dc

b) $V_{in1} = 10$ mV rms , $V_{in2} = 20$ mV rms

The op-Amp is a 741 with the following specifications : $A = 200000$, $R_i = 2M\Omega$, $R_o = 75\Omega$, $+V_{cc} = 15V$, $-V_{EE} = -15V$ and output voltage swing $= \pm 14V$.

(i) $V_o = A V_d = A (V_{in1} - V_{in2})$

$= A \{ 200000 \left(5 \times 10^{-6} - (-7) \times 10^{-6} \right)$

$= 2.4V$ dc

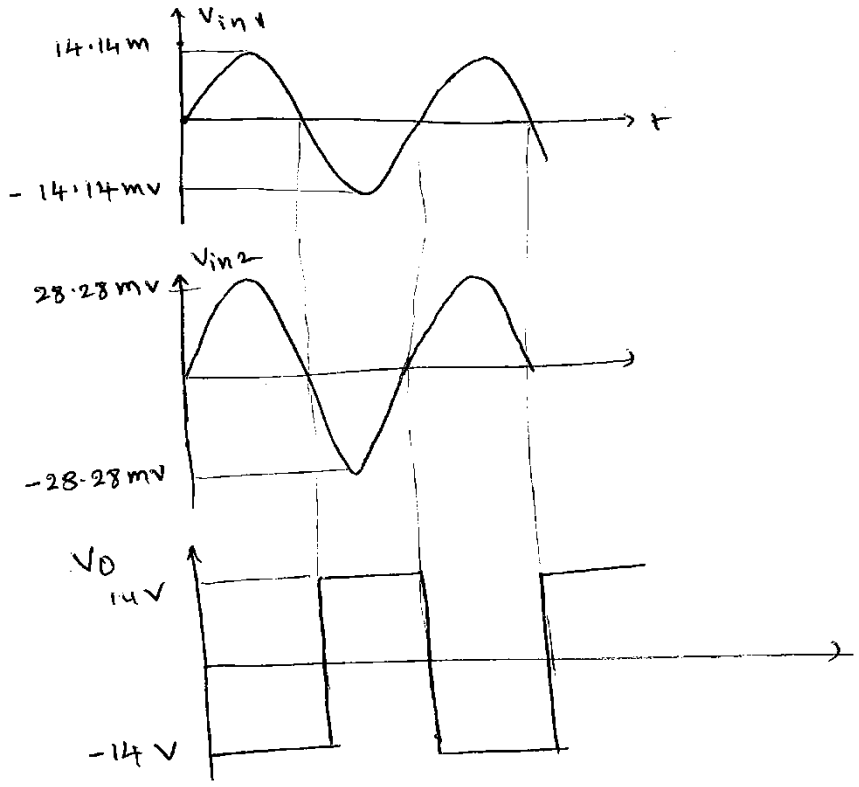
(ii) $V_o = A V_d$

$V_o = 200000 \left[10 \times 10^{-3} - (20 \times 10^{-3}) \right] = -2000 V$ rms

Now op-Amp saturates at $\pm 14V$.

$V_{in1} = 10mV$ rms $= 10\sqrt{2}$ mV $= 14.14$ mV

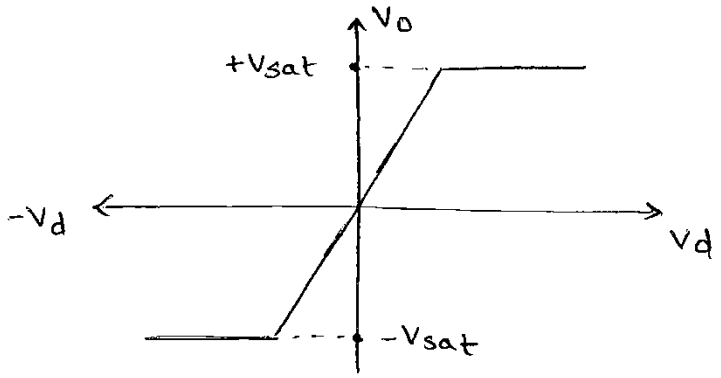
$V_{in2} = 20mV$ rms $= 20\sqrt{2}$ mV $= 28.28$ mV.



Ideal Voltage Transfer Curve:

Basic op-Amp equation $V_o = A V_d = A(V_1 - V_2)$

The plot of V_o Vs V_d is shown in figure below. Keeping gain A Constant.



Here Fig: Ideal voltage transfer curve

Here Ideal because output offset voltage is assumed to be zero.

From the graph we can say that the ouput voltage is directly proportional to the input difference voltage only until it reaches the saturation voltages and that thereafter output voltage remains constant.

Feedback in Ideal op-Amp: (Negative feedback)

The utility of an op-Amp can be greatly increased by providing Negative feed back. The output in this case is not driven in to saturation and the circuit behaves in a linear manner. There are two basic feed back connections used. In order to understand the operation of these

circuits, we make two realistic simplying assumptions.

1. the current drawn by either of the input terminals (non inverting and inverting) is negligible

2. the differential input voltage V_d between non-inverting and inverting input terminals is essentially zero.

Inverting Amplifier:

The circuit of Inverting Amplifier circuit is shown in figure below.

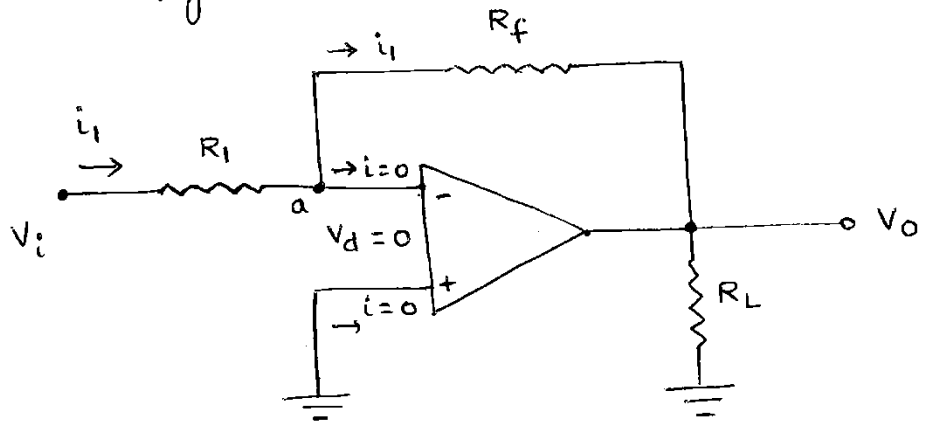


Fig: Inverting Amplifier

The output voltage V_o is fedback to the inverting input terminal through the $R_f - R_1$ network where R_f is the feedback resistor. Input signal V_i (ac or dc) is applied to the inverting input terminal through R_1 and non inverting input terminal of op-Amp is grounded.

Analysis:

For simplicity, assume an ideal op-Amp. As $V_d = 0$, node 'a' is at ground potential and the current i_1 through R_1 is

$$i_1 = \frac{V_i}{R_1} \longrightarrow (1)$$

Also since op-Amp draws no current, all the current flowing through R_1 must flow through R_f. The output voltage

From the circuit

$$i_1 = \frac{V_i - V_a}{R_1} = \frac{V_i - 0}{R_1} = \frac{V_i}{R_1} \longrightarrow (2)$$

$$i_1 = \frac{V_a - V_o}{R_f} = \frac{0 - V_o}{R_f} = -\frac{V_o}{R_f} \longrightarrow (3)$$

(2) = (3) $\quad \frac{V_i}{R_1} = -\frac{V_o}{R_f} \Rightarrow A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$.

The negative sign indicates a phase shift of 180° between V_i and V_o.

Also since inverting input terminal is at Virtual ground, the effective input impedance is R_1. The value of R_1 should be kept fairly large to avoid loading effect.

Problem :

Design an Amplifier with a gain of -10 and input resistance equal to 10 KΩ.

Solution:

Since the gain of the amplifier is negative, an inverting amplifier has to be made.

The gain of inverting amplifier is $A_{CL} = \frac{-R_f}{R_1}$

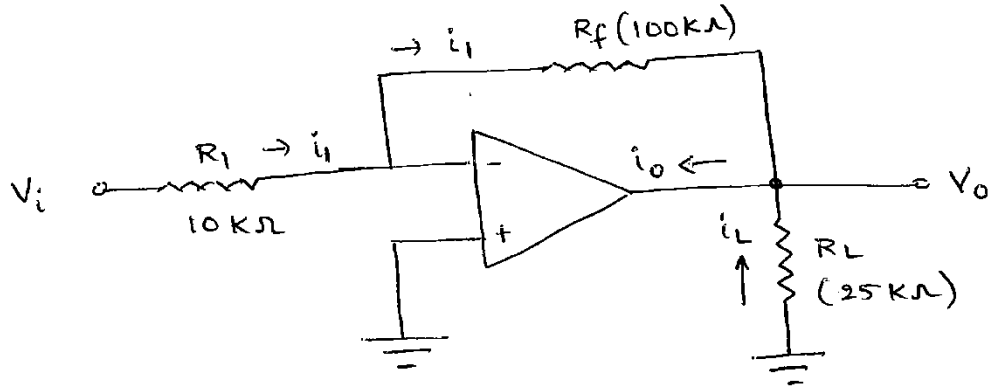
$$-10 = \frac{-R_f}{R_1} \Rightarrow$$

Choose $R_1 = 10K\Omega$

$$R_f = -A_{CL} \cdot R_1 = -(-10) \times 10K\Omega = 100K\Omega.$$

Problem:

For the circuit shown in figure below $R_1 = 10K\Omega$, $R_f = 100K\Omega$, $V_i = 1V$. A load of $25K\Omega$ is connected to the output terminal. Calculate (i) i_1 (ii) V_o (iii) i_L and total current i_o in the output pin.



Solution:

a) $i_1 = \frac{V_i}{R_1} = \frac{1}{10K\Omega} = 0.1mA$

b) $V_o = \frac{-R_f}{R_1} V_i = -\frac{100K\Omega}{10K\Omega} \times 1V = -10V$

c) $i_L = \frac{-V_o}{R_L} = \frac{-(-10V)}{R_L} = 0.4mA.$

d) Total current $i_o = i_1 + i_L = 0.1 + 0.4$

$i_o = 0.5mA.$

In an inverting amplifier, for a +ve input output will be -ve, therefore the direction of i_o is as shown in figure above

Practical Inverting Amplifier:

For a practical op-Amp the expression for the closed loop voltage gain should be calculated using the low frequency model of inverting Amplifier. The equivalent circuit of a practical inverting amplifier is shown in figure below.

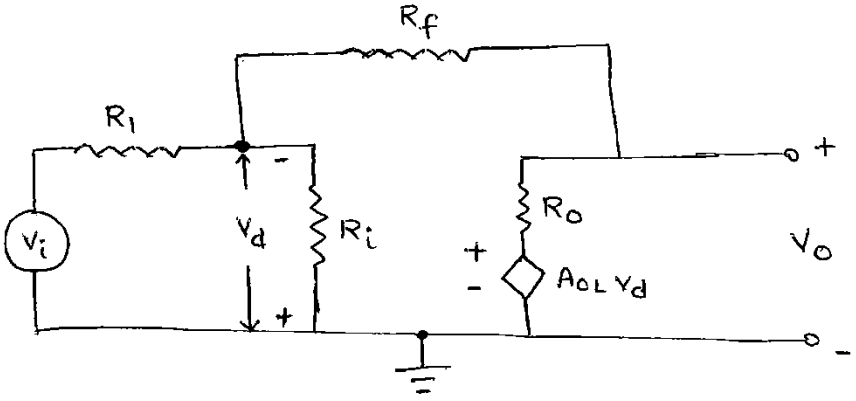
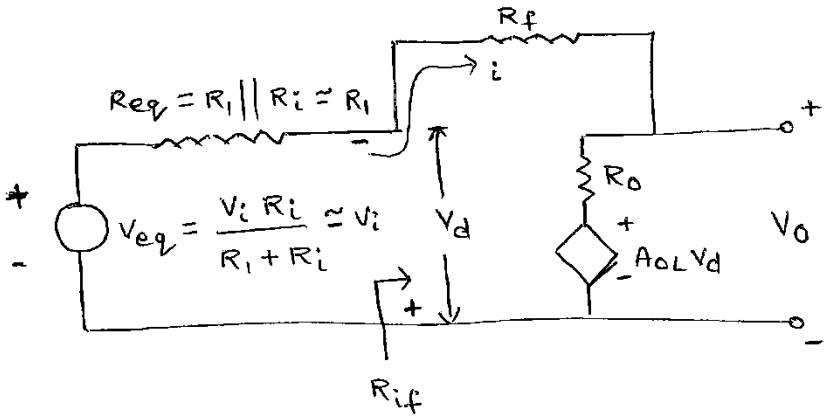


Fig: Equivalent circuit of a practical op-Amp inverting Amplifier

This circuit can be simplified by replacing the signal source V_i and resistors R_1 and R_i by thevinin's equivalent as shown in figure below, which is analysed to calculate the exact expression for closed loop gain A_{CL} and input impedance R_{if}.



Fig(b): Simplified circuit by using thevinin's Equivalent.

Fig: Simplified circuit by using thevinin's equivalent

the input impedance R_i of an op-Amp is usually much greater than R_1, so we may assume

$V_{eq} \simeq V_i$ and $R_{eq} = R_1$.

From the output loop in figure (6)

$$V_o = iR_o + A_{OL} V_d \longrightarrow (1)$$

Also $$V_d + iR_f + V_o = 0 \longrightarrow (2)$$

Putting the value of V_d from eq (2) to eq (1) and simplifying

$$V_o = iR_o + A_{OL}\left(-iR_f - V_o\right)$$

$$V_o\left(1 + A_{OL}\right) = i\left(R_o - A_{OL} R_f\right) \longrightarrow (3)$$

Also the KVL Loop equation gives

$$V_i = i(R_1 + R_f) + V_o \longrightarrow (4)$$

Putting the value of i from eq (3) in eq (2) and solving for closed loop gain

$$A_{CL} = \frac{V_o}{V_i}$$

$$V_i = \frac{V_o(1 + A_{OL})}{R_o - A_{OL} R_f}\left(R_1 + R_f\right) + V_o$$

$$V_i = \frac{V_o(1 + A_{OL}) + V_o R_o - A_{OL} R_f V_o}{R_o - A_{OL} R_f}$$

$$V_i(R_o - A_{OL} R_f) = V_o(R_o$$

$$V_i\left(R_o - A_{OL} R_f\right) = V_o\left(1 + A_{OL}\right)\left(R_1 + R_f\right) + V_o R_o - V_o A_{OL} R_f$$

$$V_i\left(R_o - A_{OL} R_f\right) = V_o R_1 + V_o R_f + V_o A_{OL} R_1 + V_o A_{OL} R_f + V_o R_o - V_o A_{OL} R_f$$

$$V_i\left(R_0 - A_{OL}R_f\right) = V_0\left(R_0 + R_f + R_1\left(1+A_{OL}\right)\right)$$

$$A_{CL} = \frac{V_0}{V_i} = \frac{R_0 - A_{OL}R_f}{R_0 + R_f + R_1\left(1+A_{OL}\right)}$$

[If $A_{OL} >> 1$,

$$A_{CL} = \frac{R_0 - A_{OL}R_f}{R_0 + R_f + A_{OL}R_1}$$ and $A_{OL}R_1 >> R_0 + R_f$, $R_0 = 0$

$$A_{CL} = \frac{-R_f}{R_1}$$]

Input Resistance R_{if} :— from fig(b)

$$R_{if} = \frac{V_d}{i}$$

writing the loop equation and solving for R_{if}

$$V_d + i\left(R_f + R_0\right) + A_{OL}V_d = 0$$

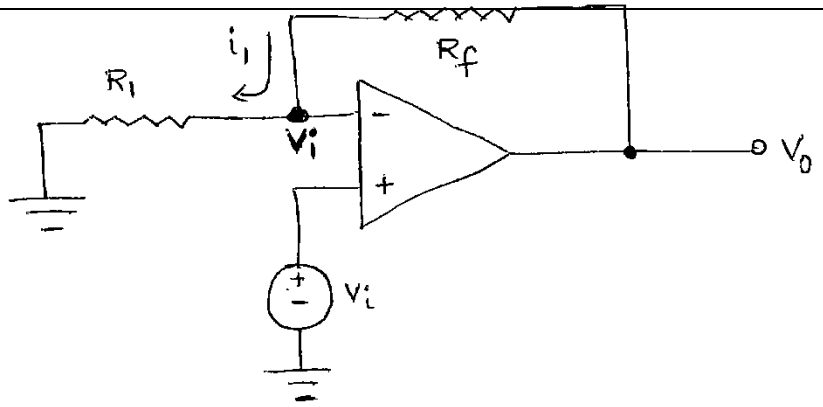
$$V_d\left(1+A_{OL}\right) = -\left(R_f + R_0\right)i$$

$$\therefore R_{if} = \frac{V_d}{i} = \frac{-\left(R_f + R_0\right)}{1 + A_{OL}}$$

Non inverting Amplifier:

If a signal (ac or dc) is applied to the non-inverting input terminal and feedback is given as shown in figure below.

the circuit amplifies with out inverting the input signal. Such a circuit is called non-inverting amplifier. It may be noted that it is also a negative feed-back system as feed back is being fed back to the inverting input terminal.



$$i_1 = \frac{V_0 - V_i}{R_f} \longrightarrow (1)$$

$$i_1 = \frac{V_i}{R_1} \longrightarrow (2)$$

$$\frac{V_0 - V_i}{R_f} = \frac{V_i}{R_1} \Rightarrow \frac{V_0}{R_f} = V_i\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

$$\Rightarrow \frac{V_0}{V_i} = R_f\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

$$A_{CL} = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

Problem: Design an Amplifier with a gain of +5 using one OP-Amp.

Solution: Since the gain is positive, the amplifier is Non-inverting Amplifier.

Assume $R_1 = 10K\Omega$

$$A_{CL} = 1 + \frac{R_f}{R_1}$$

$$5 = 1 + \frac{R_f}{R_1} \Rightarrow R_f = 4R_1$$

$$R_f = 4 \times 10K\Omega = 40K\Omega.$$

problem: In the circuit shown in figure below let $R_1 = 5K\Omega$, $R_f = 20K\Omega$ and $V_i = 1V$. A load resistor of $5K\Omega$ is connected at the output. calculate

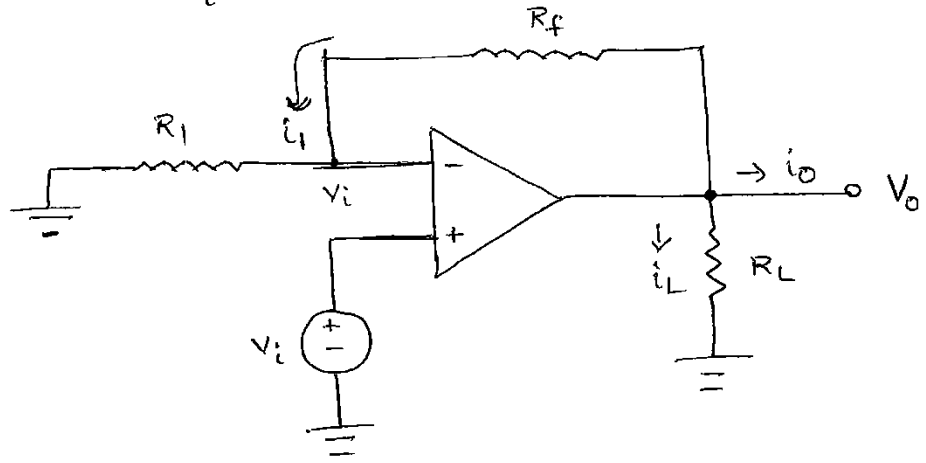
(i) V_o (ii) A_{CL} (iii) the load current i_L (iv) the output current i_o indicating proper direction of flow.

Solution:

(i) $$V_o = \left(1 + \frac{R_f}{R_1}\right) V_i = \left(1 + \frac{20K\Omega}{5K\Omega}\right)(1V) = 5V$$

(ii) $$A_{CL} = \frac{V_o}{V_i} = \frac{5V}{1V} = 5$$

(iii)



(iii) $$i_L = \frac{V_o}{R_L} = \frac{5}{5K\Omega} = 1mA$$

(iv) $$i_1 = \frac{V_i}{R_1} = \frac{1}{5K\Omega} = 0.2mA$$

(iv) $$i_o = i_L + i_1 = 1mA + 0.2mA = 1.2mA$$

The op-Amp output current i_o flows outwards from the output junction.

Practical Non-Inverting Amplifier :

The analysis of practical non-inverting Amplifier can be performed by using the equivalent circuit shown in figure below.

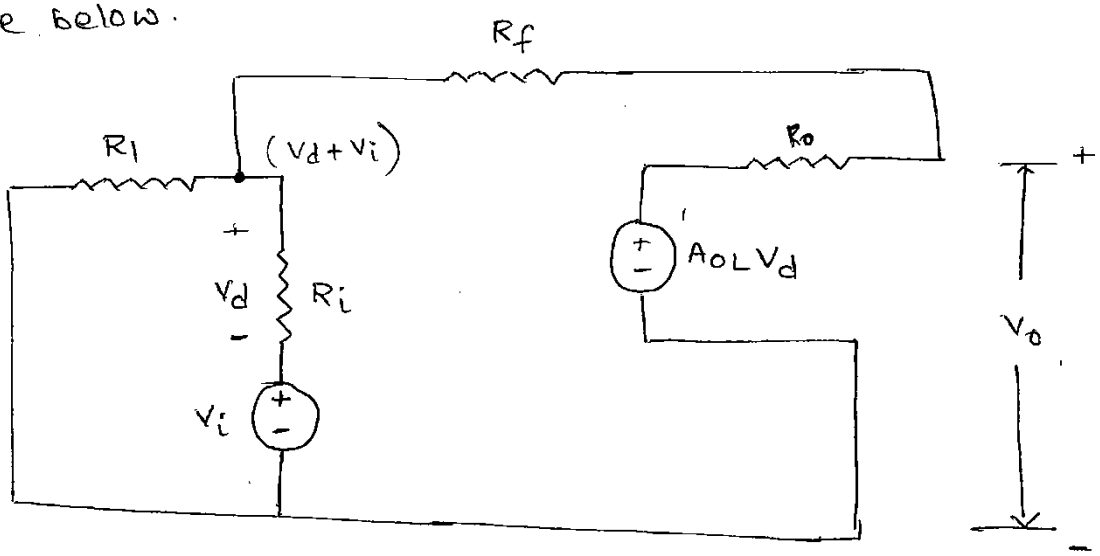


Fig: Equivalent circuit of Non inverting Amplifier using low frequency model.

writing KCL at the input node

$$\left(V_o - (V_d + V_i)\right) Y_f = (V_d + V_i) Y_1 + V_d Y_i$$

$$Y_f V_o = V_d \left(Y_1 + Y_i + Y_f\right) + V_i \left(Y_1 + Y_f\right) \longrightarrow (1)$$

writing KCL at the output node

$$\left(V_d + V_i - V_o\right) Y_f = \left(V_o - A_{OL} V_d\right) Y_o$$

$$V_o \left(Y_f + Y_o\right) = V_d \left(A_{OL} Y_o + Y_f\right) + Y_f V_i \longrightarrow (2)$$

From Eq (1) $$V_d = \frac{Y_f V_o - \left(Y_1 + Y_f\right) V_i}{Y_1 + Y_i + Y_f} \longrightarrow (3)$$

Substitute Eq (3) in Eq (2), After simplifying

$$A_{CL} = \frac{V_o}{V_i} = \frac{A_{OL}\, Y_0 (Y_1 + Y_f) - Y_f Y_i}{(A_{OL} - 1) Y_0 Y_f - (Y_1 + Y_i)(Y_0 + Y_f)} \longrightarrow (4)$$

This is the required closed loop gain of practical NON inverting Amplifier.

[For Ideal Amplifier, $A_{OL} \longrightarrow \infty$, so using in Eq (4), we get

$$A_{CL} = \frac{A_{OL}\, Y_0 (Y_1 + Y_f) - \frac{Y_f Y_i}{A_{OL}}}{(Y_0 \cdot Y_f) - \frac{Y_0 Y_f}{A_{OL}} - \frac{(Y_1 + Y_i)(Y_0 + Y_f)}{A_{OL}}} \Bigg|_{A_{OL} \to \infty}$$

$$A_{CL} = \frac{Y_0 (Y_1 + Y_f)}{Y_0 Y_f} = 1 + \frac{Y_1}{Y_f} \simeq 1 + \frac{R_f}{R_1}$$

$$=$$

Virtual Ground :

The differential input voltage V_d between the non inverting and inverting terminals is essentially zero.

This is obvious because even if output voltage is few volts, due to large open loop gain of op-Amp, the difference voltage V_d at the input terminals is almost zero.

Ex of output voltage is 10 V and the A_{OL} is 10^4 then

$$V_o = V_d \cdot A_{OL}$$

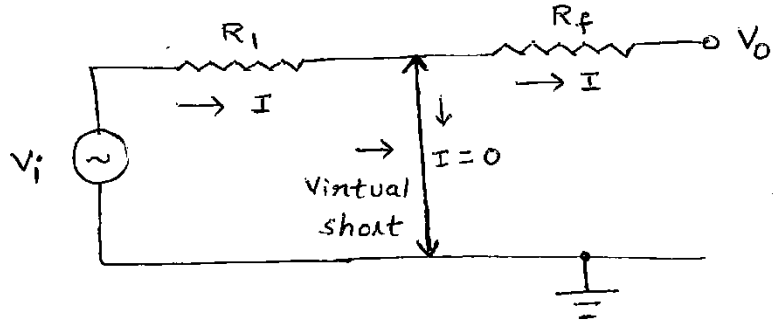
$$V_d = \frac{V_o}{A_{OL}} = \frac{10}{10^4} = 1\,mV$$

Hence V_d is very small.

As $A_{OL} \to \infty$, the differential voltage $V_d \to 0$, and assumed to be zero for analysing the circuits.

$$V_d = \frac{V_o}{A_{OL}} \Rightarrow V_1 - V_2 = \frac{V_o}{A_{OL}} = \frac{V_o}{\infty} = 0$$

$$V_1 = V_2$$



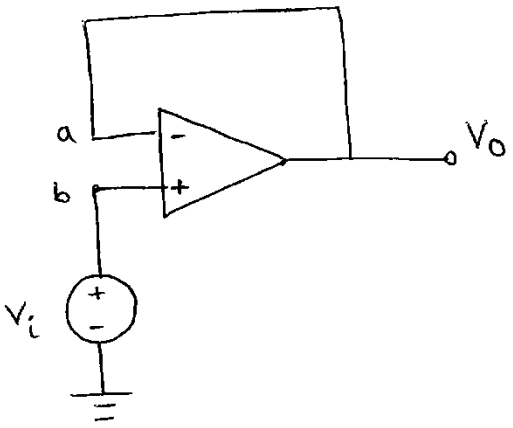
Thus we can say that under linear range of operation there is virtually short circuit between the two input terminals, in the sense that their voltages are same. No current flows from input terminals to the ground.

The above figure shows that the concept of virtual ground. The thick line indicates the virtual short between the input terminals.

Now if the non-inverting terminal is grounded by the concept of virtual short, the inverting terminal is also at ground potential, though there is no physical connection between the inverting terminal and the ground. this is the principle of virtual ground.

Voltage Follower:

In the Non-inverting amplifier if $R_f = 0$ and $R_1 = \infty$, we get the modified circuit shown in figure below



Here $V_b = V_i$ and $V_a = V_b$

$\therefore V_a = V_i$

Now $V_o = V_a$ and $\boxed{V_o = V_i}$

That is the output voltage is equal to input voltage both in magnitude and phase. In other words we can say that the output voltage follows the input voltage exactly. Hence the circuit is called a 'Voltage Follower'.

It is also called buffer Amplifier, unity gain amplifier and isolation Amplifier.

Advantages:

1- Input impedance is very high (ie MΩ), low output impedance. therefore it draws negligible current from the source. thus a voltage follower

may be used as buffer for impedance matching that is, to connect a high impedance source to a low impedance load.

2. It has large bandwidth

Differential Amplifier :

A circuit that Amplifies the difference between two signals is called a difference or differential amplifier. This type of the amplifier is very useful in instrumentation circuits.

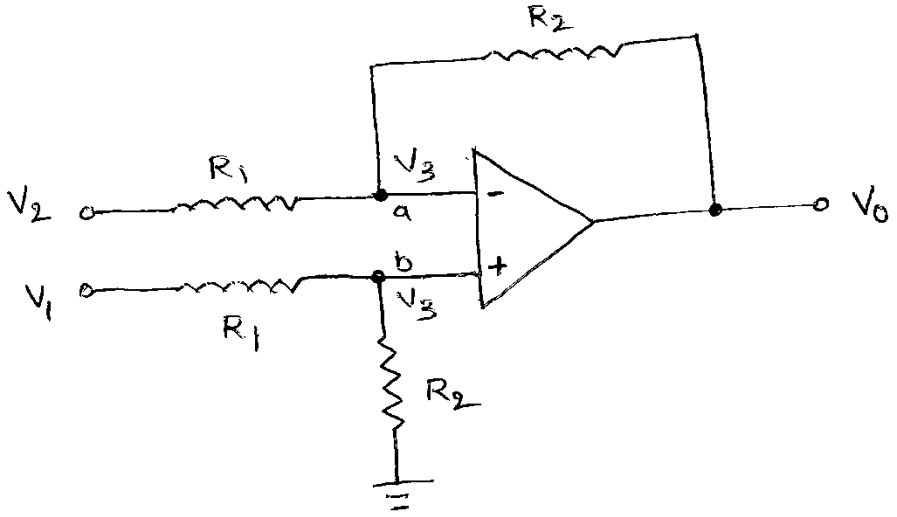


Fig : Differential Amplifier

$$\frac{V_2 - V_3}{R_1} = \frac{V_3 - V_0}{R_2}$$

and $$\frac{V_1 - V_3}{R_1} = \frac{V_3}{R_2}$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) V_3 = \frac{V_1}{R_1}$$

After simplifying

$$V_0 = \frac{R_2}{R_1}(V_1 - V_2)$$

Such a circuit is very useful in detecting very small differences in signals. since the gain $\frac{R_2}{R_1}$ can be chosen to be very large For example if $R_2 = 100 R_1$, then a small difference $V_1 - V_2$ is amplified 100 times.

Difference mode and common mode Gains.

output of a differential amplifier

$$V_0 = \frac{R_2}{R_1}(V_1 - V_2) \longrightarrow (1)$$

If $V_1 = V_2$ then $V_0 = 0$. That is, the signal common to both inputs gets cancelled and produces no output voltage. This is true for an ideal op-Amp, however a practical op-Amp exhibits some small response to the common mode component of the input voltages too.

For example, the output V_0 will have different value for cases

(i) with $V_1 = 100\mu V$ and $V_2 = 50\mu V$

(ii) with $V_1 = 1000\mu V$ and $V_2 = 950\mu V$

even though the difference signal $V_1 - V_2 = 50\,\mu V$ in both the cases.

the output voltage depends not only upon the difference signal V_d at the input, but is also affected by the average voltage of the input signals, called the common-mode signal V_{CM} defined as

$$V_{CM} = \frac{V_1 + V_2}{2}$$

For differential amplifier, though the circuit is symmetric, but because of the mismatch the gain at the output with respect to the positive terminal is slightly different in magnitude to that of the negative terminal. so even with the same voltage applied to both inputs, the output is not zero. The output therefore must be expressed as

$$V_o = A_1 V_1 + A_2 V_2 \longrightarrow (2)$$

where V_1 = voltage multiplication from input 1 to the output with input 2 grounded

V_2 = voltage multiplication from input 2 to the output with input 1 grounded.

since $V_{cm} = \frac{V_1 + V_2}{2}$ and $V_d = (V_1 - V_2)$

$$V_1 = V_{cm} + \frac{1}{2} V_d \longrightarrow (3)$$

$$V_2 = V_{CM} - \frac{1}{2} V_d \longrightarrow (4)$$

Substitute the value of V_1 and V_2 in eq ②, we get

$$V_o = A_{DM} V_d + A_{CM} V_{CM} \longrightarrow ④$$

where $A_{DM} = \frac{1}{2}(A_1 - A_2)$

$$A_{CM} = A_1 + A_2$$

The voltage gain for the difference signal is A_{DM} and that for the common mode signal is A_{CM}

Common mode Rejection Ratio :

The relative sensitivity of an op-Amp to a difference signal as compared to a common mode signal is called common mode Rejection Ratio (CMRR) and gives the figure of merit (ρ) for the differential amplifier. So, CMRR is given by

$$\rho = \left| \frac{A_{DM}}{A_{CM}} \right|$$

and is usually expressed in decibels (dB)

For example, the μA741 op-Amp has a minimum CMRR of 70 dB.

we should have A_{DM} large, A_{CM} should be zero ideally. So, higher the value of CMRR, better is the op-Amp.

Problem:

Determine the output of a differential amplifier for the input voltages of 300μv and 240μv. The differential gain of the amplifier is 5000 and the value of CMRR is (i) 100 (ii) 10^5.

Solution:

case 1: $CMRR = 100$, $V_1 = 300\mu V$, $V_2 = 240\mu V$

$$V_d = V_1 - V_2 = 300\mu V - 240\mu V = 60\mu V$$

$$V_{CM} = \frac{V_1 + V_2}{2} = \frac{300\mu V + 240\mu V}{2} = 270\mu V$$

$$A_{DM} = 5000$$

$$CMRR = \frac{A_{DM}}{A_{CM}} \Rightarrow A_{CM} = \frac{A_{DM}}{CMRR} = \frac{5000}{100}$$

$$\Rightarrow A_{CM} = 50$$

$$V_0 = A_{DM} V_d + A_{CM} V_{CM}$$

$$V_0 = (5000 \times 60\mu V) + (50 \times 270\mu V)$$

$$V_0 = 313.5 mV.$$

case 2: $CMRR = 10^5$, $V_1 = 300\mu V$, $V_2 = 240\mu V$

$$CMRR = \frac{A_{DM}}{A_{CM}} \Rightarrow A_{CM} = \frac{A_{DM}}{CMRR} = \frac{5000}{10^5} =$$

$$V_0 = 300.0135 mV.$$

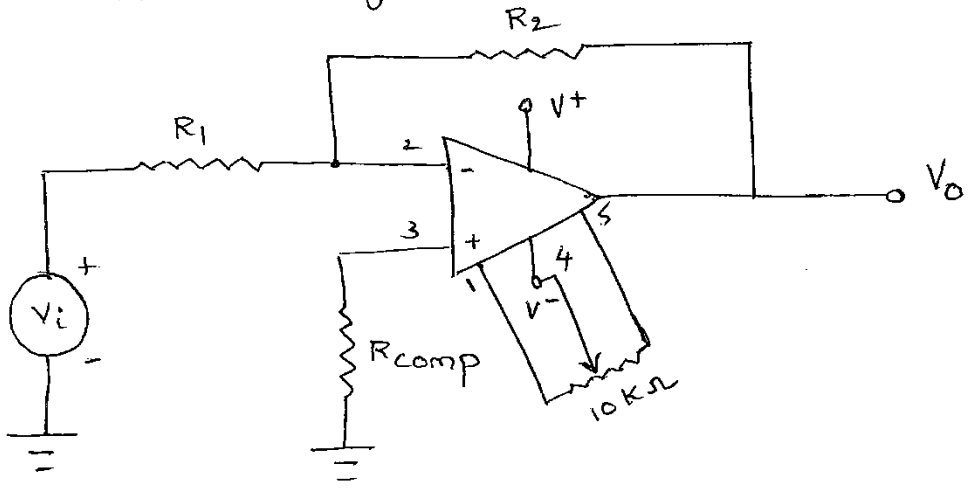
used, is given by

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_B$$

However with R_{comp} in the circuit then

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_{os}$$

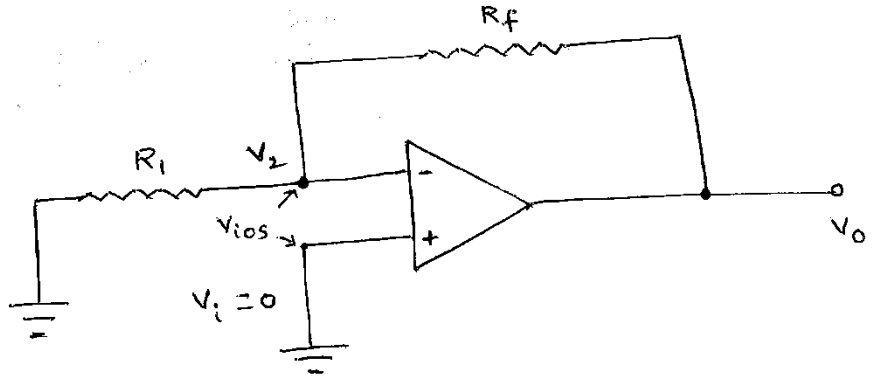
Many op-Amps provide offset Compensation pins to nullify the offset voltage. Figure below gives the connections for the 741 OP-Amp. The manufacturers recommend that a 10kΩ potentiometer potentiometer be placed across offset null pins 1 and 5 and the wiper be connected to the negative supply pin 4. The position of the wiper is adjusted to nullify the output offset voltage.



Thermal Drift:

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25°c may not remain so when the temperature rises to 35°c. This is called drift.

offset current drift is expressed in nA/°c and offset voltage drift in mv/°c. These indicate the change in offset for each degree celcius change in temperature.



the voltage V_2 at the inverting terminal is

$$V_2 = V_o \frac{R_1}{R_1 + R_f}$$

$$\Rightarrow V_o = V_2 \left(\frac{R_1 + R_f}{R_1} \right) = \left(1 + \frac{R_f}{R_1} \right) V_2$$

Since $V_{ios} = |V_i - V_2|$ and $V_i = 0$

$$V_{ios} = |0 - V_2| = V_2$$

$$V_o = \left(1 + \frac{R_f}{R_1} \right) V_{ios}$$

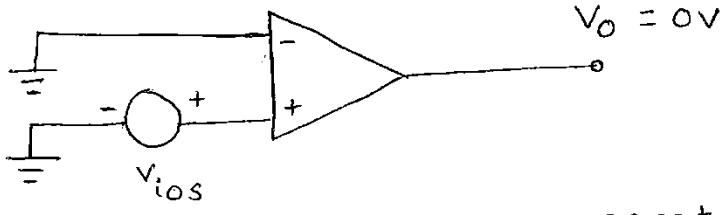
Thus the output offset voltage of an op-Amp in closed loop configuration is given by above eq.

Total output offset voltage:

The total output offset voltage V_{OT} could be either more or less than the offset voltage produced at the output due to input bias current or input offset voltage alone. this is because input offset voltage V_{ios} and the input bias current I_B could be either positive or negative with respect to ground. Therefore the max offset voltage at the output of an inverting and non inverting amplifier without any compensating technique

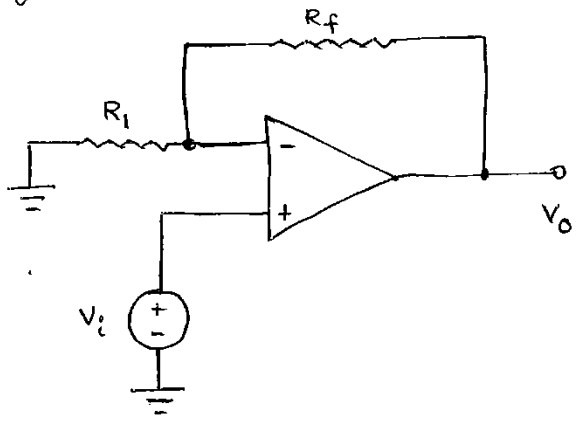
Input offset voltage :

Inspite of the use of the above Compensating techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-Amp and a small voltage is to be applied ~~at~~ btn the input terminals to make output voltage zero. This voltage is called Input offset voltage V_{ios}. This is the voltage required to be applied at the input for making output voltage to zero volts as shown in figure below.

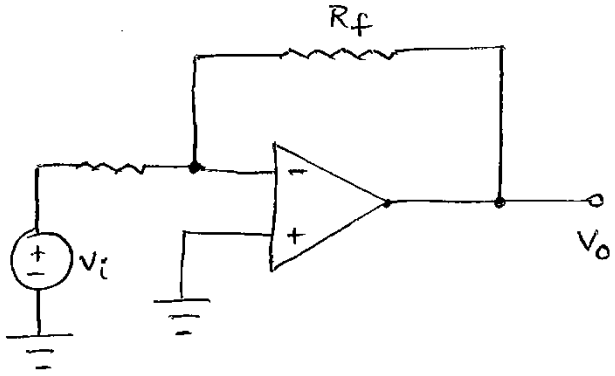


Fig(a): op-Amp showing input offset voltage.

Figure shows the Non-inverting and Inverting Amplifier CKts



Fig(b): Non Inverting Amplifier



Fig(c): Inverting Amplifier

If V_i is set to zero, the above circuits become the same as shown in figure below.

To obtain high input resistance R_1 must be kept large. with R_1 large, the feedback resistor R_f must also be high so as to obtain reasonable gain.

the T- feedback network is a good solution. This will allow large feedback resistance while keeping the resistance to ground (seen by the inverting i/p) low as shown in the dotted lines.

The T- network provides a feedback signal as if the network were a single feedback resistor

By T to π Conversion

$$R_f = \frac{R_t^2 + 2R_t R_s}{R_s}.$$

To design a T- network, first pick $R_t << \frac{R_f}{2}$ then calculate $R_s = \frac{R_t^2}{R_f - 2R_t}$.

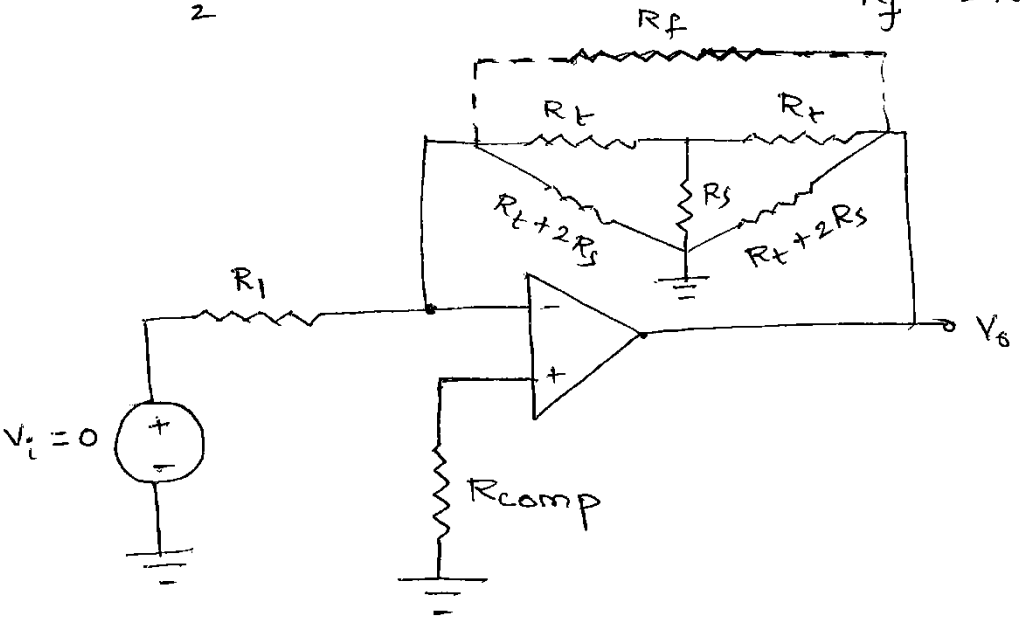


Fig: Inverting Amplifier with T- feedback Network

KCL at node 'a' gives

$$I_B^- = I_1 + I_2 \Rightarrow I_2 = I_B^- - I_1$$

$$I_2 = I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1} \right) \rightarrow (4)$$

Again $$I_2 = \frac{V_0 + V_\phi}{R_f} \Rightarrow V_0 = I_2 R_f - V_1$$

$$V_0 = I_2 R_f - I_B^+ (R_{comp})$$

$$\Rightarrow V_0 = \left(I_B^- - \frac{I_B^+ R_{comp}}{R_1} \right) R_f - I_B^+ R_{comp}$$

$$V_0 = \left(I_B^- R_f - \left(I_B^+ \left(R_{comp} \frac{R_f}{R_1} + R_{comp} \right) \right) \right)$$

$$V_0 = I_B^- R_f - I_B^+ R_{comp} \left(1 + \frac{R_f}{R_1} \right)$$

$$V_0 = I_B^- R_f - I_B^+ \frac{R_f R_1}{R_f + R_1} \left(\frac{R_f + R_1}{R_1} \right)$$

$$V_0 = R_f \left(I_B^- - I_B^+ \right)$$

$$V_0 = R_f I_{os} . \rightarrow (5)$$

So even with bias current compensation and with the feedback resistor of 1MΩ, a 741 BJT op-Amp has an output offset voltage

$V_0 = 1M\Omega \times 200nA = 200mV$. with a zero input voltage.

From it can be seen from Equation (5) that the effect of offset current can be minimized by keeping R_f small

Input offset Current :

Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal. Since the input transistors cannot be made identical, there will always be some small difference between I_B^+ and I_B^-. The difference is called the offset current I_{os} and can be written as

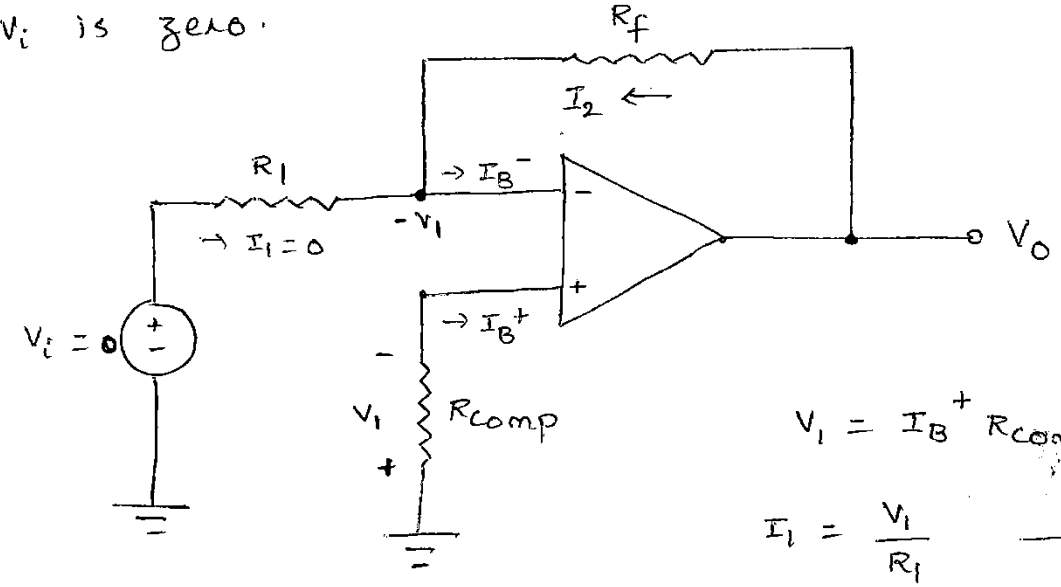
$$|I_{os}| = I_B^+ - I_B^-$$

The absolute value sign indicates that there is no way to predict which of the bias currents will be larger.

Offset current I_{os} for BJT Op-Amp is 200nA

FET Op-Amp is 10pA.

Even with bias current compensation, offset current will produce an output voltage when the input voltage V_i is zero.



$$V_1 = I_B^+ R_{comp} \longrightarrow (1)$$

$$I_1 = \frac{V_1}{R_1} \longrightarrow (2)$$

$$I_1 = I_B^+ \left(\frac{R_{comp}}{R_1}\right) \longrightarrow (3)$$

KCL at node a

For compensation V_o should be zero for $V_i = 0$, that is from Eq ① $V_2 = V_1$

so that $I_2 = \frac{V_1}{R_f}$

KCL at node 'a' gives $I_B^- = I_2 + I_1 = \frac{V_1}{R_f} + \frac{V_1}{R_1}$

Assuming $I_B^- = I_B^+$

$$V_1\left[\frac{1}{R_f} + \frac{1}{R_1}\right] = I_B^+$$

From Eq ②

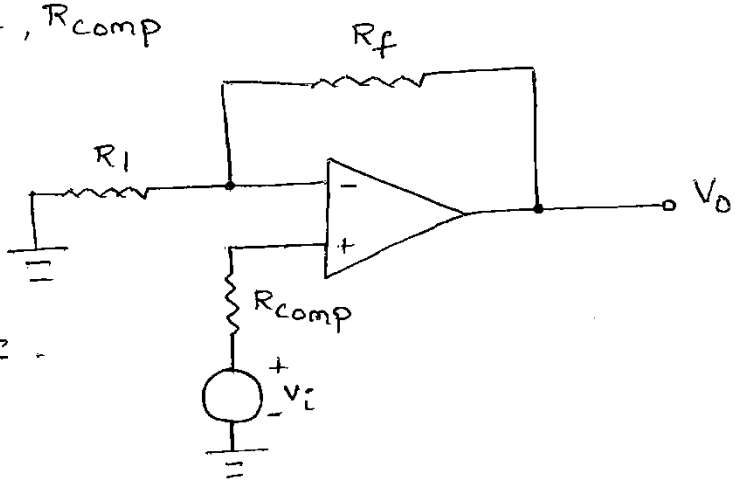
$$V_1\left[\frac{1}{R_f} + \frac{1}{R_1}\right] = \frac{V_1}{R_{comp}}$$

$$\Rightarrow \frac{1}{R_{comp}} = \frac{1}{R_f} + \frac{1}{R_1}$$

$$\Rightarrow R_{comp} = R_1 \| R_f$$

That is to compensate for bias currents, the corresponding resistor R_{comp} should be equal to the parallel combination of resistors tied to the inverting input terminal.

The effect of input bias current in a non-inverting amplifier can also be compensated by placing a compensating resistor, R_{comp} in series with the input signal V_i as shown in figure



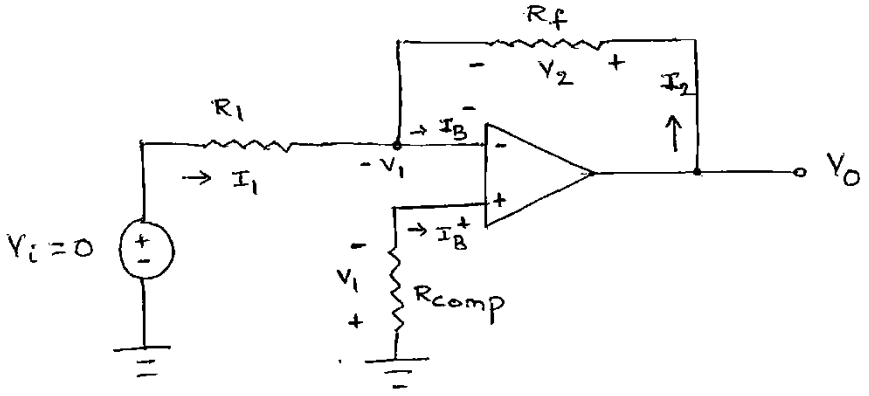
Here $R_{comp} = R_1 \| R_f$.

For example, For a 741 op-Amp, with a $R_f = 1M\Omega$

$$V_o = I_B^- R_f = 500\,nA \times 1M\Omega = 500\,mV$$

with zero input, because of bias currents, the output is driven to 500mV

This Effect can be compensated for as shown in fig(c) where a compensation resistor R_{comp} has been added between the non-inverting terminal and ground.



current I_B^+ flowing through the compensating resistor R_{comp} develops a voltage V_1 across it. Then by KVL we get

$$V_o = V_2 - V_1 \longrightarrow (1)$$

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the output V_o will be zero. the value of R_{comp} is derived as

$$V_1 = I_B^+ R_{comp}$$

$$I_B^+ = \frac{V_1}{R_{comp}} \longrightarrow (2)$$

Now $V_a = -V_1 \Rightarrow$ $I_1 = \frac{V_a - (-V_1)}{R_1} = \frac{0 + V_1}{R_1} = \frac{V_1}{R_1}$

Also $I_2 = \frac{V_2}{R_f}$

Even though both the transistors are identical, I_B^- and I_B^+ are not equal due to internal imbalances between the two inputs.

Manufacturers specify input bias current I_B as the average value of the base currents entering in to the terminals of an op-Amp.

$$\text{so} \quad I_B = \frac{I_B^+ + I_B^-}{2}$$

FOR $\overset{BJT}{741}$ x op Amp $\rightarrow I_B = 500\,nA \quad \left(I_B^+ = I_B^- = 500\,nA \right)$

FOR FET op-Amp $\rightarrow I_B = 50\,pA$.

Consider the basic inverting Amplifier

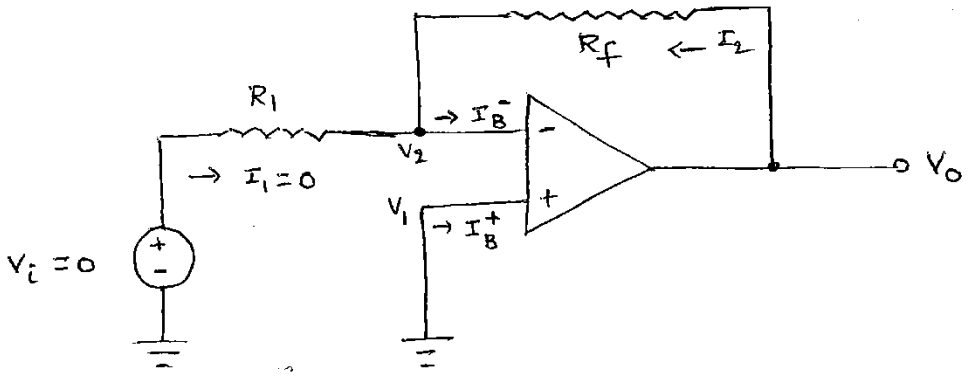


Fig (b): Inverting Amplifier with bias currents

If the input voltage $V_i = 0$, V_o should also be zero Instead the output voltage is offset by

From the ckt $\quad I_1 + I_2 = I_B^-$

$$I_1 = 0 \quad \Rightarrow \quad I_2 = I_B^-$$

$$I_2 = \frac{V_o - V_2}{R_f} = I_B^-$$

$$V_o - 0 = I_B^- R_f \quad \Rightarrow \quad V_o = I_B^- R_f$$

Operational Amplifier characteristics

DC Characteristics : An ideal op-Amp draws no current from the source and its response is also independent of temperature. However a real op-Amp doesn't work this way. Current is taken from the source in to the op-Amp inputs. Also the two inputs respond differently to current and voltage due to mismatch in transistors. A real op-Amp also shifts its operation with temperature. These non-ideal dc characteristics that add error components to the dc output voltage are

1) Input Bias Current
2) Input offset Current
3) Input offset Voltage
4) Thermal Drift.

1) Input Bias current :

Practically input terminals conduct a small value of dc current to bias the input transistors. The base currents entering in to the inverting and non inverting terminals are shown as I_B^- and I_B^+ respectively. (Fig (a))

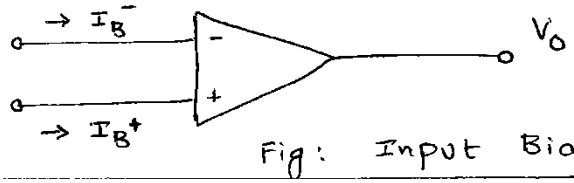


Fig: Input Bias Currents

there are very few circuit techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be used to keep op-Amps away from source of heat. Forced air cooling may be used to stabilize the ambient temperature.

problem:

a) For the non-inverting amplifier if $R_1 = 1k\Omega$ and $R_f = 10k\Omega$. Calculate the maximum output offset voltage due to V_{ios} and I_B. The op-Amp is LM307 with $V_{ios} = 10mV$ and $I_B = 300nA$, $I_{os} = 50nA$.

b) calculate the value of R_{comp} needed to reduce the effect of I_B

c) calculate the maximum output offset voltage if R_{comp} as calculated in (b) is connected in the circuit

solution:

a) $$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_B$$

$$V_{OT} = \left(1 + \frac{10k\Omega}{1k\Omega}\right)(10mV) + (10k\Omega)(300nA) = 113mV$$

b) The value of R_{comp} needed is

$$R_{comp} = 1k\Omega \,||\, 10k\Omega = 990\Omega$$

c) with R_{comp} in the circuit

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_{os} = 110mV + 0.5mV$$

$$V_{OT} = 110.5mV.$$

problem:

A non inverting Amplifier with a gain of 100 is nulled at 25°c. what will happen to the output voltage if the temperature rises to 50°c for an offset voltage drift of 0.15mv/°c ?

solution:

Input offset voltage due to temperature rise

$$V_{ios} = 0.15\,mV/^{\circ}C \times (50^{\circ}C - 25^{\circ}C) = 3.75\,mV.$$

since this is an input change, the output voltage will change by

$$V_o = V_{ios} \times A_{CL}$$

$$V_o = 3.75\,mV \times 100 = 375\,mV.$$

AC characteristics:

1. Frequency Response:

Ideally an op-Amp should have an infinite bandwidth. The practical op-Amp gain, however decreases at higher frequencies, because of the capacitive component in the equivalent circuit of the op-Amp.

Two major sources are responsible for capacitive effects

1. physical characteristics of semi conductor devices; opAmps are composed of BJT's and FET's which contain junction capacitors. As frequency increases, the reactance of these capacitors decrease
2. The Internal Construction of the op-Amp is a second source of capacitive effects. In op-Amps a number of transistors as well as resistors and some times a capacitor are integrated on the same material, called a substrate. Infact, the substrate acts as an insulator and helps to separate these components. The various components are connected by conducting paths, and the paths are separated by insulators. However, whenever two conducting paths are separated by an insulator, it acts as a capacitor. this means that because of its construction the op-Amp may contain a number of such stray capacitors.

The cumulative effect of these capacitors due to the characteristics of semi conductor devices and the internal construction of the op-Amp causes the gain to decrease as the frequency increases.

For an op-Amp with only one break frequency, we will represent all the capacitive effects by a single capacitor as shown in figure below.

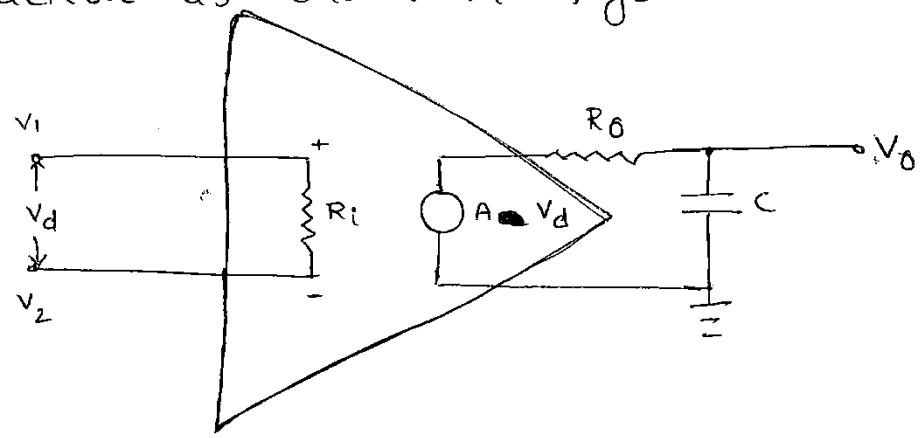


Fig: High frequency model of an op-Amp with single break frequency.

the gain as a function of frequency can be obtained as

$$V_0 = \frac{-jX_C}{R_0 - jX_C} A V_d$$

$$V_0 = \frac{\frac{1}{j2\pi f C}}{R_0 + \frac{1}{j2\pi f C}} A V_d$$

$$V_0 = \frac{A V_d}{1 + j2\pi f R_0 C}$$

Hence the open loop voltage gain is

$$A_{OL}(f) = \frac{V_o}{V_d}$$

$$A_{OL}(f) = \frac{A}{1 + j 2\pi f R_o C}$$

Let $f_o = \frac{1}{2\pi R_o C}$, then

$$A_{OL}(f) = \frac{A}{1 + j\left(\frac{f}{f_o}\right)}$$

where $A_{OL}(f)$ = open loop voltage gain as a function of frequency

A = Gain of the op-Amp at 0 Hz (dc)

f = operating frequency

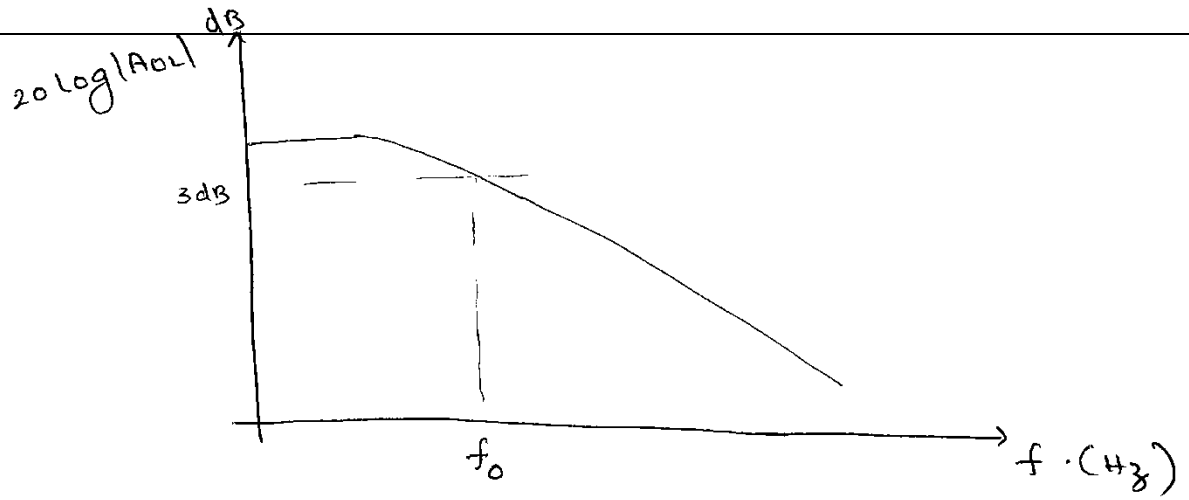
f_o = break frequency of the op-Amp.

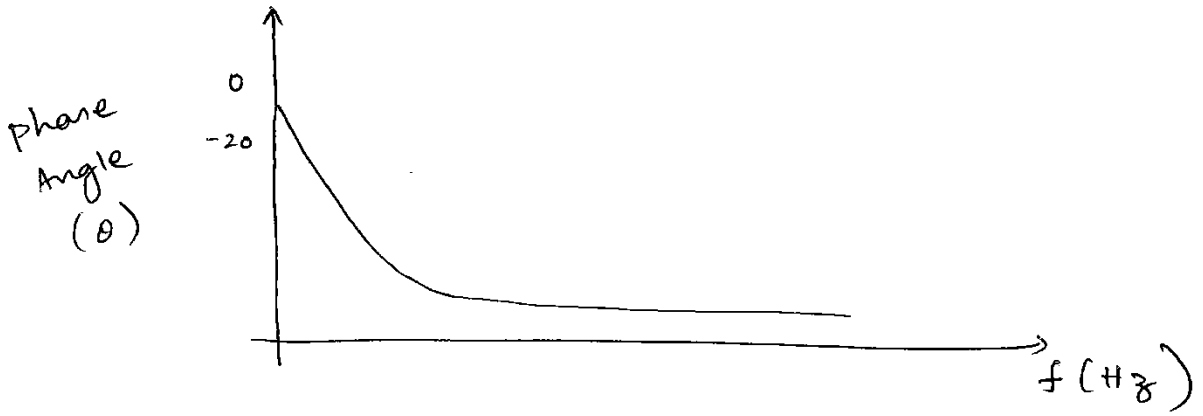
Now the break frequency f_o depends on the value of C and on output resistance R_o. Therefore f_o is fixed for a given op-Amp.

$$|A_{OL}(f)| = \frac{A}{\sqrt{1 + \left(\frac{f}{f_o}\right)^2}} \quad \text{and}$$

Phase Angle $\phi(f) = -\tan^{-1}\left(\frac{f}{f_o}\right)$

The open loop gain $A_{OL}(f)$ dB is approximately constant from 0 Hz to the break frequency f_o.



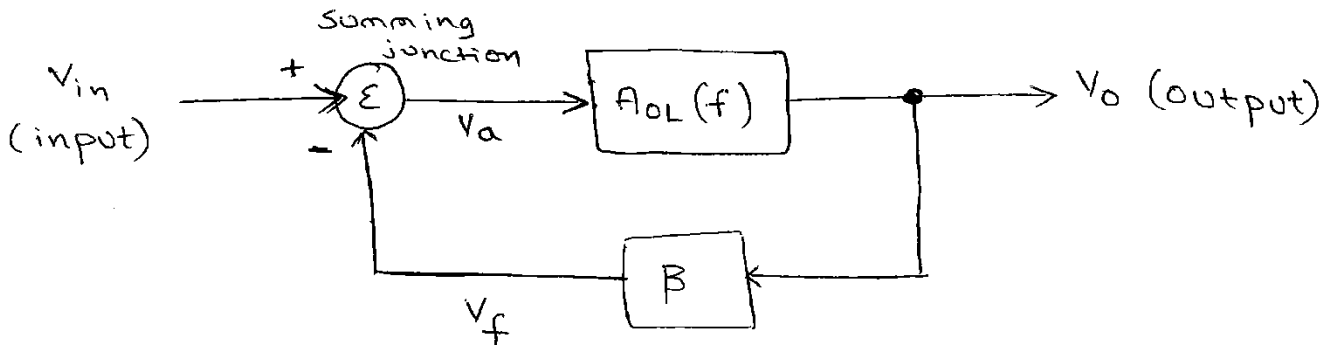


~~Open~~ closed loop frequency Response :

For an open loop op-Amp the band width is very small.

In order to increase the band width, a negative feed back must be used

A typical closed loop system (Non inverting Amplifier)



$$A_{OL}(f) = \frac{V_o}{V_a} \quad \text{and} \quad \beta = \frac{V_f}{V_o}$$

$$V_a = V_{in} - V_f \;. \quad \Rightarrow \quad V_{in} = V_a + V_f$$

$$A_{CL}(f) = \frac{V_o}{V_{in}} = \frac{V_o}{V_a + V_f}$$

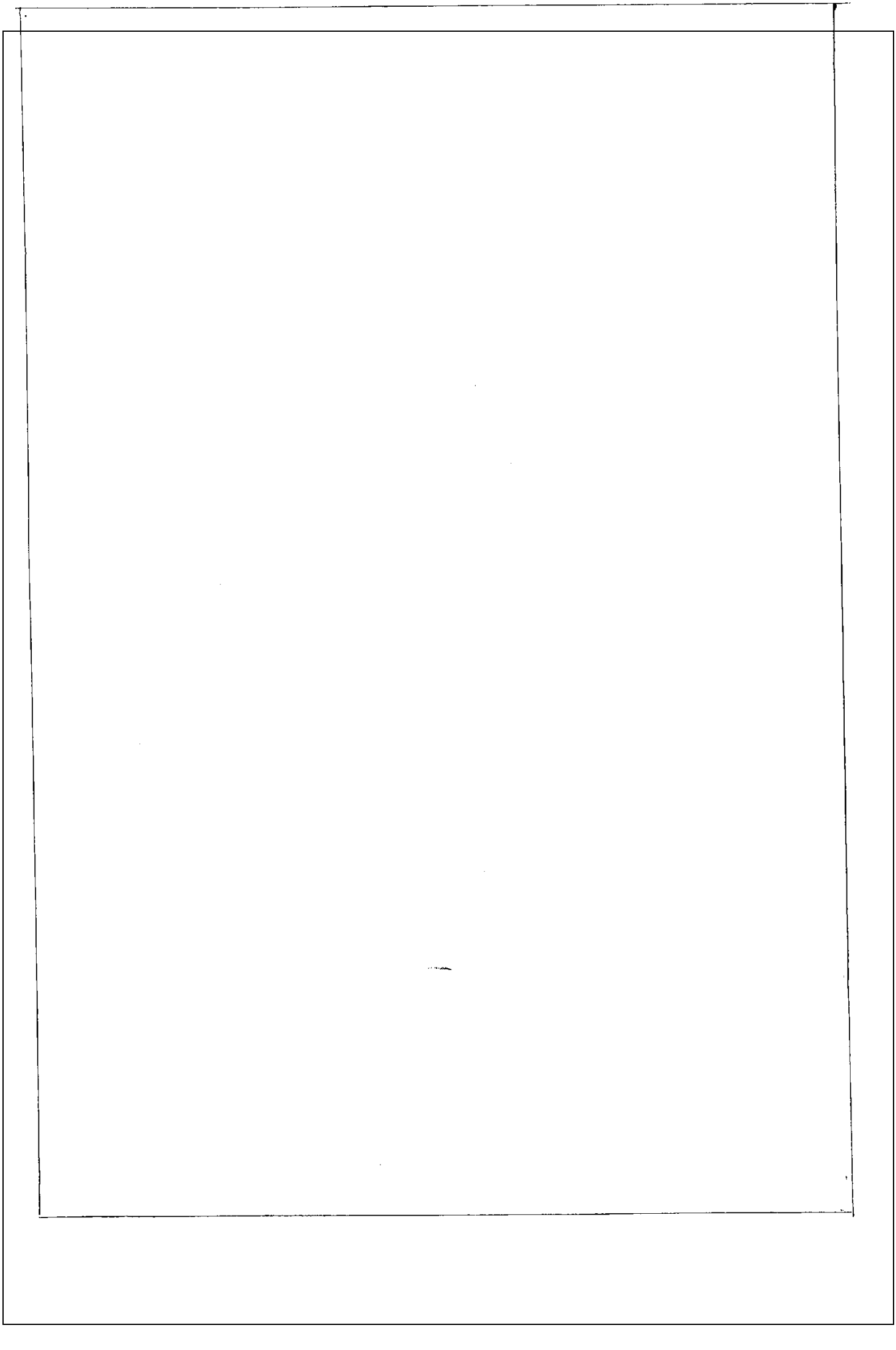
$$A_{CL}(f) = \frac{V_o/V_o}{\frac{V_a}{V_o} + \frac{V_f}{V_o}} \quad \Rightarrow \quad \frac{1}{\frac{1}{A_{OL}(f)} + \beta}$$

$$A_{CL}(f) = \frac{A_{OL}(f)}{1 + A_{OL}(f)\,\beta} \;.$$

System stability may be determined as follows.

<u>Method 1</u> : Determine the phase Angle when the Magnitude of $A_{OL}(f)\,\beta$ is 0 dB or 1. If the phase angle is $> 180^\circ$, the system is stable. However for some systems the Magnitude may never be 0dB. in that Case method 2 must be used to determine the system stability.

Method 2 : Determine the Magnitude of $A_{OL}(f)\,\beta$ when the phase angle is -180°. If the Magnitude is negative decibels, then the system is stable. However some times the phase angle of a system may never reach -180°, under such conditions, Method 1 must be used to determine the system stability.



Slew Rate :

Slew Rate is defined as the maximum rate of change of output voltage with respect to time. a slew Rate is specified in units of $V/\mu s$.

The general purpose op-Amps such as 741 have a maximum slew rate of $0.5 V/\mu s$, which means that the output voltage can change at a maximum of 0.5V in $1 \mu s$.

Causes for slew Rate :

The slew Rate is determined by a number of factors such as the amplifier gain, compensating capacitors and the change in polarity of output voltage It is also a function of temperature and the slew Rate generally reduces due to rise in temperature.

The capacitor within or outside the op-Amp is required to prevent oscillation and this capacitor restricts the response of op-Amp to a rapidly changing input signal. The rate at which the voltage across the capacitor V_c increases is given by

$$\frac{dV_c}{dt} = \frac{I}{C}$$

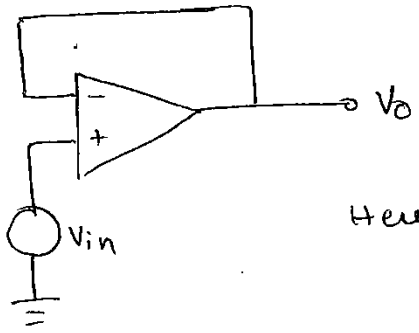
where I is the current furnished by the internal circuit. this means that the op-Amp must have either a higher current or a small Compensation capacitor.

For example IC 741 can provide 15 μA of maximum current to its internal 30PF capacitor. that is

$$\text{Slew Rate} = \left.\frac{dV_c}{dt}\right|_{max} = \frac{I_{max}}{C} = \frac{15\,\mu A}{30\,PF} = 0.5\,V/\mu s$$

Slew Rate Equation:

since the slew Rate is generally listed for a unity gain let us consider the voltage follower shown in figure below.



Here $V_o = V_{in}$

let us assume that the input is a large amplitude and high frequency sine wave. The Equation for the sine wave is

$$V_{in} = V_p \sin \omega t$$

$$V_o = V_p \sin \omega t$$

The rate of change of the output is

$$\frac{dV_o}{dt} = V_p \omega \cos \omega t$$

and the maximum rate of change of output occurs when $\cos \omega t = 1$ that is

$$\left.\frac{dV_o}{dt}\right|_{max} = V_p \omega$$

$$\text{Slew Rate} = 2\pi f V_p$$

$$\text{Slew Rate} = \frac{2\pi f V_p}{10^6} \text{ V/}\mu\text{s}$$

The maximum frequency f_{max} at which an undistorted output voltage with a peak value V_p can be obtained is determined by

$$f_{max} = \frac{\text{Slew Rate} \times 10^6}{2\pi V_p}$$

The maximum peak sinusoidal output voltage $(V_p)_{max}$ that can be obtained at a frequency of f is given by

$$(V_p)_{max} = \frac{\text{Slew Rate} \times 10^6}{2\pi f}$$

Problem: The op-Amp 741 Connected as a unity gain inverting amplifier is applied with a input change of 10V. Determine the time taken for the output to change by 10V.

Solution: For op-Amp Slew Rate = 0.5 V/μs

$$\text{Slew Rate} = \frac{\text{output voltage change}}{\text{Time}}$$

$$\text{Time} = \frac{10\text{V}}{0.5\text{ V/}\mu\text{s}} = 20\mu\text{s}.$$

problem: The slew Rate for 741 is 0.5 V/μs. What is the maximum undistorted sine wave that can be obtained for 12V peak.

$$f_{max} = \frac{\text{slew Rate} \times 10^6}{2\pi V_m} = \frac{0.5 \times 10^6}{2\pi \times 12} = 6.63\,kHz.$$

Problem: The 741 C is used as an inverting amplifier with a gain of 50. the sinusoidal input signal has a Variable frequency and maximum frequency of the input Aplitude of 20 mv peak. what is max at which the output will be undistorted? Assume that the amplifier is initially nulled.

Solution: $A = \frac{V_o}{V_{id}} \Rightarrow V_o = A V_{id} = 50 \times 20mV$

$$V_o = 1000 \times 10^{-3} V = 1 V (peak) = V_p$$

$$f_{max} = \frac{SR \times 10^6}{2\pi V_p} = \frac{0.5 \times 10^6}{2\pi \times 1} = 79.6\,kHz.$$

problem: An inverting amplifier using the 741 c must have a flat response upto 40 kHz. The gain of the amplifier is 10. what maximum peak to peak input signal can be applied with out distorting the output?

solution: slew Rate of 741 op-Amp = $0.5\,V/\mu s$

$$SR = \frac{2\pi f V_p}{10^6}$$

$$(V_p)_{max} = \frac{SR \times 10^6}{2\pi f} = \frac{0.5 \times 10^6}{2\pi \times 40 \times 10^3} = 1.99\,V$$

$$V_p = 1.99\,V = V_o$$

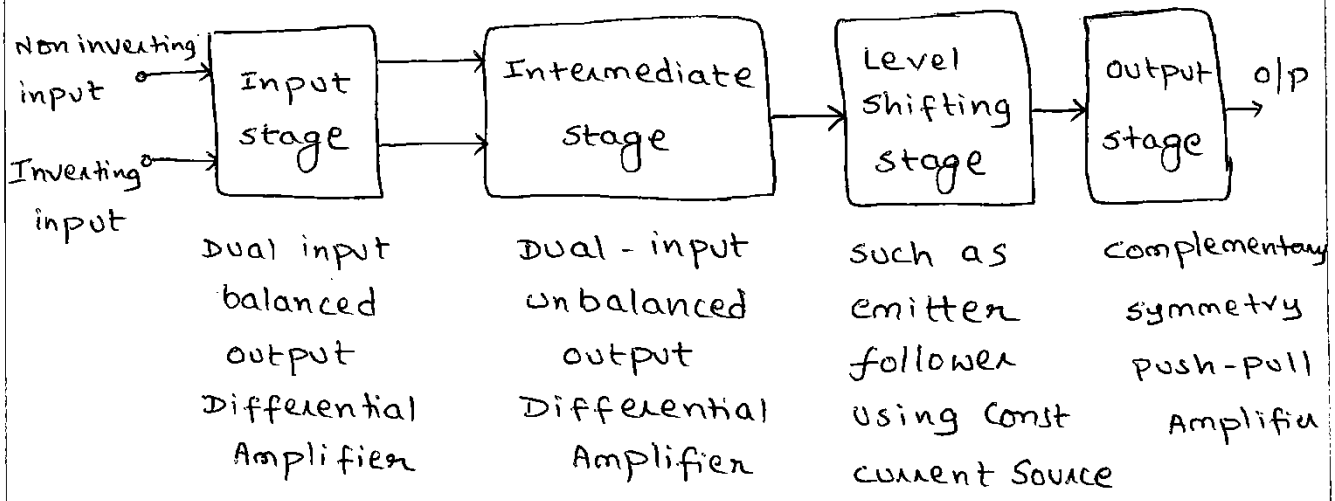
$$(V_o)_{peak} = 1.99V \Rightarrow (V_o)_{peak\ to\ peak} = 3.98V$$

$$A = \frac{(V_o)_{peak\ to\ peak}}{(V_{in})_{peak\ to\ peak}} \Rightarrow A = \frac{3.98}{(V_{in})_{peak\ to\ peak}}$$

$$(V_{in})_{peak\ to\ peak} = \frac{3.98}{10} = 0.398V.$$

Op-Amp Internal circuit

Op-Amps usually consists of four cascaded blocks. The block diagram of IC Op-Amp is shown in figure below.



Input stage:

The input stage requires high input impedance to avoid loading on the sources. It requires two input terminals. It also requires low output impedance. All such requirements are achieved by using the dual input, balanced output differential amplifier as the input stage. The function of a differential amplifier is to amplify the difference between the two input signals. The differential amplifier has high input impedance. This stage provides most of the voltage gain of the amplifier

Intermediate stage :

The output of the input stage drives the next stage which is a intermediate stage. This is another differential amplifier with Dual input unbalanced output ie. single ended output. The overall gain requirement of the op-Amp is very high. The input stage alone cannot provide such a high gain. The main function of the Intermediate stage is to provide an additional voltage gain required. practically the intermediate stage is not a single amplifier but the chain of cascaded amplifiers called as multistage Amplifiers.

3) Level shifting stage :

All the stages are directly coupled to each other. As the op-Amp amplifies d.c signals also, the coupling capacitors are not used to cascade the stages. Hence the dc quiescent voltage level of previous stage gets applied as the input to the next stage. Hence stage by stage dc level increases well above ground ~~level~~ potential. Such a high d.c level may drive the transistors into saturation. This further may cause distortion in the output due to clipping. this may limit the

maximum a.c output voltage swing with out any distortion. Hence before the output stage, it is necessary to bring such a high dc voltage level to zero volts with respect to ground.

The level shifter stage brings the dc level down to ground potential, when no signal is applied at the input terminals. Then the signal is given to the last stage which is the output stage.

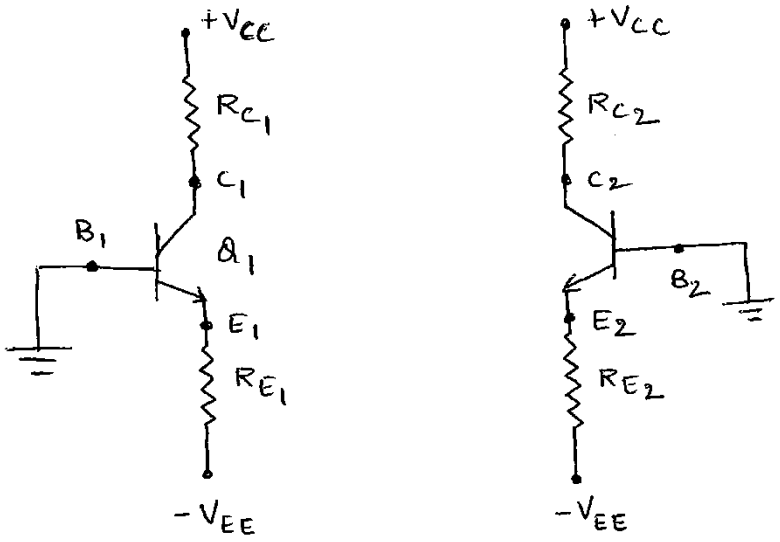
Output stage :

The basic requirements of an output stage are low output impedance, large ac output voltage swing and high current source and sinking capability.

The push pull complementary amplifier meets all these requirements and hence used as an output stage. This stage increases the output voltage swing and keeps the voltage swing symmetrical with respect to ground. This stage raises the current supplying capability of the op-Amp.

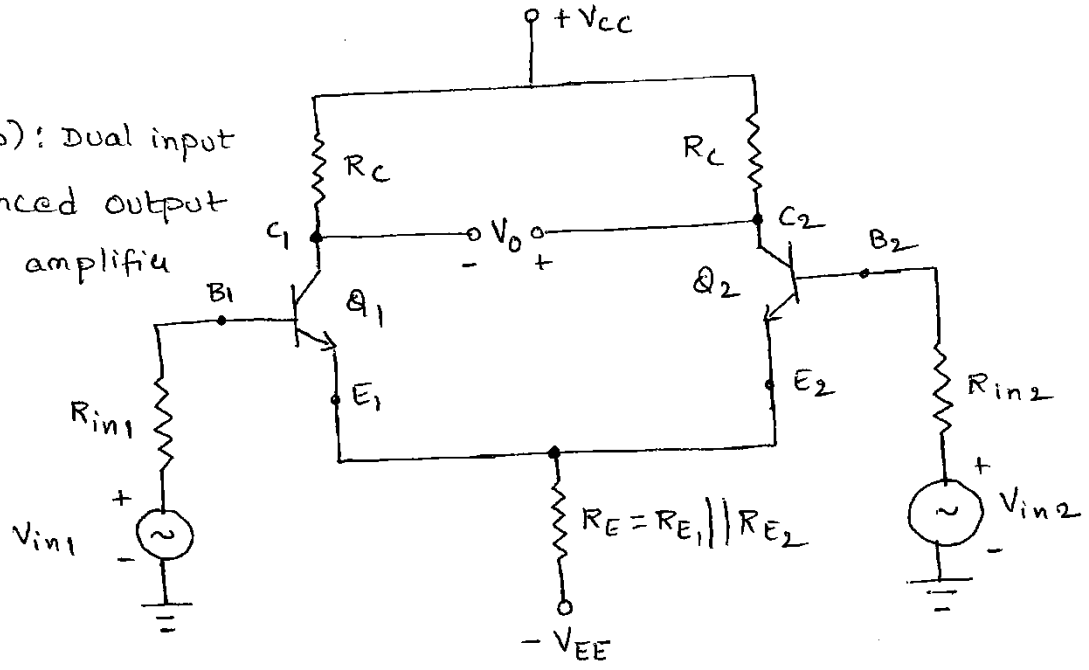
Differential Amplifier:

Let us consider the emitter biased circuit. Figure below shows two emitter identical emitter-biased circuits in that transistor Q_1 has the same characteristics as transistor Q_2. $R_{E_1} = R_{E_2}$, $R_{C_1} = R_{C_2}$ and the magnitude of $+V_{CC}$ is equal to the magnitude of $-V_{EE}$ Here the supply voltages $+V_{CC}$ and $-V_{EE}$ are mear measured with respect to ground.



Fig(a): Two identical emitter-biased circuits

Fig(b): Dual input balanced output diff amplifier



the two circuits of fig(a) are reconnected to obtain a single circuit as shown in fig(b).

the differential amplifier of fig(b) amplifies the difference between two input signals V_{in1} and V_{in2}. the differential amplifier is also referred to as difference amplifier.

Differential Amplifier Circuit configurations :

the four differential amplifier configurations are

1. Dual input, balanced output differential amplifier
2. Dual input, unbalanced output differential amplifier
3. Single input, balanced output differential amplifier
4. Single input, unbalanced output differential amplifier.

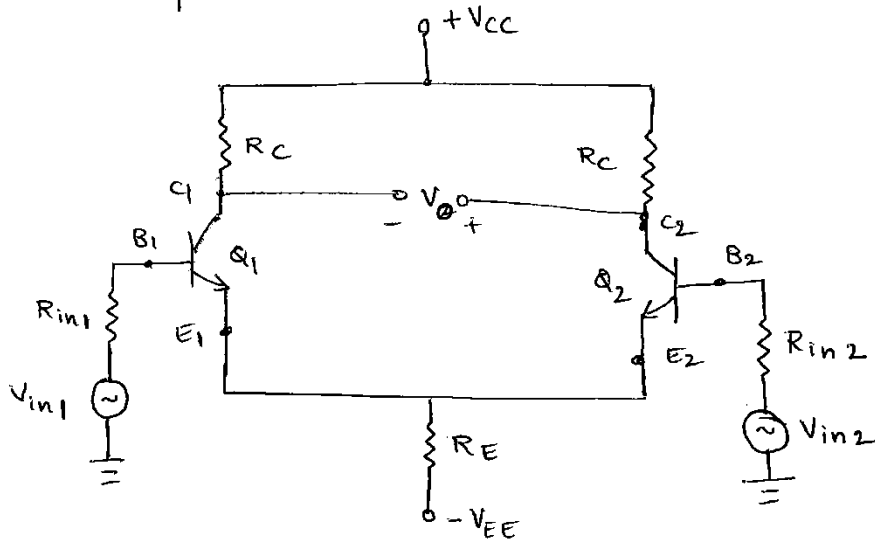
If we use two input signals, the configuration is said to be dual input, otherwise it is a single input configuration.

If the output is measured between two collectors it is referred to as a balanced output, because both collectors are at the same dc potential with respect to ground.

If the output is measured at one of the collectors with respect to ground, the configuration is called an unbalanced output.

i) Dual input, Balanced output Differential Amplifier

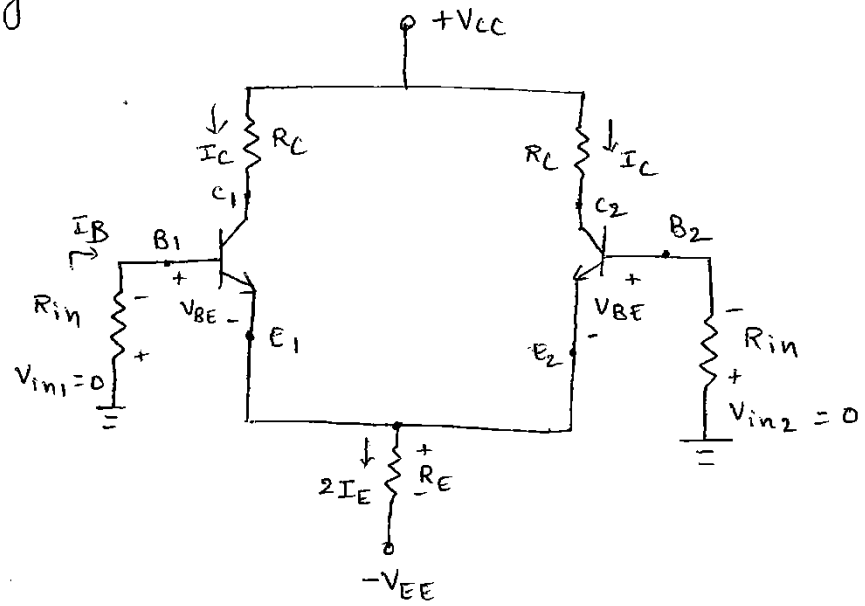
Figure below shows the dual input balanced output differential amplifier.



Fig(a): Dual input, balanced output differential Amplifier

Here the output V_o is measured between the two collectors C_1 and C_2 which are at the same dc potential. Because of the equal dc potential at the two collectors with respect to ground, the output is referred to as a balanced output.

Dc Analysis:



Fig(b): Dc Equivalent circuit of the dual input, balanced output differential amplifier.

To determine the operating values (I_{CQ} and V_{CEQ}) for the differential amplifier of fig(a), it is needed to obtain a dc Equivalent circuit. The dc equivalent circuit can be obtained simply by reducing the input signals V_{in1} and V_{in2} to zero. The dc Equivalent circuit is shown in figure (b).

Since both emitter-biased junctions of the differential amplifier are symmetrical, the operating point (V_{CEQ}, I_{CQ}), for only one section (Q_1) can be determined. these V_{CEQ} and I_{CQ} can then be used for transistor Q_2 also.

Applying KVL to the base emitter loop of the transistors Q_1

$$0 = R_{in} I_B + V_{BE} + 2 I_E R_E - V_{EE} \longrightarrow (1)$$

But $I_C = \beta I_B$ since $I_C \simeq I_E$

$$I_E = \beta_{dc} I_B \Rightarrow I_B = \frac{I_E}{\beta_{dc}} \longrightarrow (2)$$

From Eq (1) & (2) $I_E = \dfrac{V_{EE} - V_{BE}}{2R_E + \dfrac{R_{in}}{\beta_{dc}}}$

From Eq (1) & (2), $V_{EE} = V_{BE} + 2R_E \dfrac{I_E}{\beta_{dc}} + R_{in} \dfrac{I_E}{\beta_{dc}}$

$$V_{EE} = V_{BE} + I_E \left[2R_E + \frac{R_{in}}{\beta_{dc}} \right]$$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E + \dfrac{R_{in}}{\beta_{dc}}} \longrightarrow (3)$$

Generally $\frac{R_{in}}{\beta_{dc}} << 2R_E$, therefore Eq ③ can be written as

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \longrightarrow ④$$

By selecting the proper value of R_E, the desired value of emitter current for a known value of $-V_{EE}$.

The voltage at the emitter of transistor Q_1 is approximately equal to $-V_{BE}$, if we assume that voltage drop across R_{in} to be negligibly small.

$$V_C = V_{CC} - I_C R_C$$

But $V_{CE} = V_C - V_E$

$$V_{CE} = (V_{CC} - I_C R_C) - (-V_{BE})$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C \longrightarrow ⑤$$

Hence for both transistors, the I_{CQ} and V_{CEQ} by Equations ④ and ⑤ can be determined because the operating point $I_E = I_{CQ}$ and $V_{CE} = V_{CEQ}$.

AC analysis :

To perform ac analysis to derive the expression for the voltage gain A_d and the input resistance R_i of the differential amplifier shown in figure (a)

1. set the dc voltages $+V_{CC}$ and $-V_{EE}$ at zero
2. Substitute the small-signal T-equivalent models for the transistors.

Figure (c) shows the resulting ac equivalent circuit of the dual input, balanced output differential amplifier

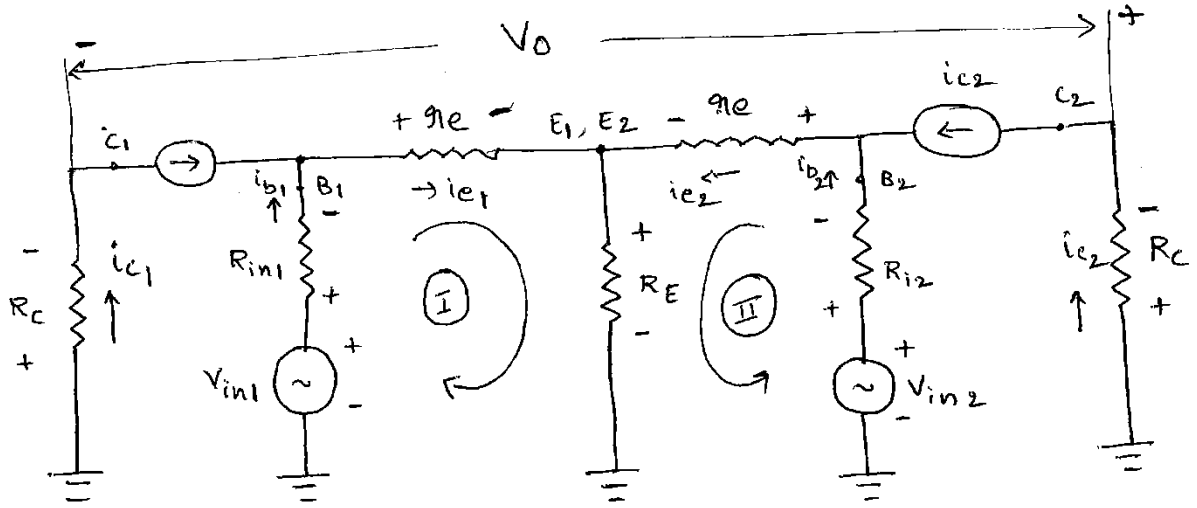


Fig C: AC Equivalent ckt

writing KVL for loops I and II in figure (c)

$$V_{in1} = R_{in1} i_{b1} + i_{e1} r_e + R_E (i_{e1} + i_{e2}) \longrightarrow (1)$$

$$V_{in2} = i_{b2} R_{in2} + i_{e2} r_e + R_E (i_{e1} + i_{e2}) \longrightarrow (2)$$

$$i_{b1} = \frac{i_{e1}}{\beta_{ac}} \qquad i_{b2} = \frac{i_{e2}}{\beta_{ac}}$$

Generally $\frac{R_{in1}}{\beta_{ac}}$ and $\frac{R_{in2}}{\beta_{ac}}$ values are very small. therefore we shall neglect them

$$V_{in1} = \frac{R_{in1}}{\beta_{ac}} i_{e1} + i_{e1} r_e + R_E (i_{e1} + i_{e2}) \longrightarrow (3)$$

$$V_{in2} = \frac{R_{in2}}{\beta_{ac}} i_{e2} + i_{e2} r_e + R_E (i_{e1} + i_{e2}) \longrightarrow (4)$$

$$\therefore V_{in1} = (r_e + R_E) i_{e1} + R_E i_{e2} \longrightarrow (5)$$

$$V_{in2} = R_E i_{e1} + (r_e + R_e) i_{e2} \longrightarrow (6)$$

Equations (5) and (6) can be solved simutaneously for ie_1 and ie_2 by using Cramer's rule.

$$ie_1 = \frac{\Delta_1}{\Delta} = \frac{\begin{vmatrix} V_{in1} & R_E \\ V_{in2} & r_e + R_E \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$ie_1 = \frac{(r_e + R_E) V_{in1} - R_E V_{in2}}{(r_e + R_E)^2 - (R_E)^2} \longrightarrow (7)$$

$$ie_2 = \frac{\Delta_2}{\Delta} = \frac{\begin{vmatrix} r_e + R_E & V_{in1} \\ R_E & V_{in2} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$ie_2 = \frac{(r_e + R_E) V_{in2} - R_E V_{in1}}{(r_e + R_E)^2 - (R_E)^2} \longrightarrow (8)$$

The output voltage $V_o = V_{c_2} - V_{c_1}$

$$V_o = -ic_2 R_C - (-ic_1 R_C)$$

$$V_o = R_C (ic_1 - ic_2)$$

$$V_o = R_C (ie_1 - ie_2) \longrightarrow (9)$$

Substituting the current relations ie_1 and ie_2 in Eq (9) we get

$$V_o = R_C \left[\frac{(r_e + R_E) V_{in1} - R_E V_{in2}}{(r_e + R_E)^2 - R_E^2} - \frac{(r_e + R_E) V_{in2} - R_E V_{in1}}{(r_e + R_E)^2 - R_E^2} \right]$$

$$V_o = \frac{R_C}{r_e}(V_{in1} - V_{in2})$$

Let $V_d = V_{in1} - V_{in2}$, then

$$V_o = \frac{R_C}{r_e} V_d \quad \Rightarrow \quad A_d = \frac{V_o}{V_d} = \frac{R_C}{r_e} \longrightarrow (10)$$

The voltage gain equation of the differential amplifier is independent of R_E.

2. Differential input Resistance :

Differential input resistance is defined as the equivalent resistance that would be measured at either input terminals with the other terminal grounded.

$$R_{i1} = \left| \frac{V_{in1}}{i_{b1}} \right|_{V_{in2}=0}$$

$$R_{i1} = \left| \frac{V_{in1}}{I_{e1}/\beta_{ac}} \right| = \frac{\beta_{ac} V_{in1}}{(r_e + R_E) V_{in1} - R_E (0)}$$

$$\frac{}{(r_e + R_E)^2 - R_E^2}$$

$$R_{i1} = \frac{\beta_{ac} (r_e^2 + 2 r_e R_E)}{(r_e + R_E)}$$

$$R_{i1} = \frac{\beta_{ac} \; r_e (r_e + 2R_E)}{(r_e + R_E)}$$

$R_E \gg r_e$ which implies that $r_e + 2R_E \simeq 2R_E$

$r_e + R_E \simeq R_E$

$$R_{i1} = \frac{\beta_{ac} \; r_e \; 2R_E}{R_E}$$

$$R_{i1} = 2\beta_{ac} r_e$$

Similarly $R_{i2} = 2\beta_{ac} r_e$.

Output Resistance :

Output resistance is defined as the equivalent resistance that would be measured at either output terminal with respect to ground.

$$R_{O1} = R_{O2} = R_C .$$

Inverting and Non inverting Inputs :

In the differential amplifier circuit the input voltage V_{in1} is called the non inverting input because a positive voltage V_{in1} acting alone produces a positive output voltage.

$$V_O = \frac{R_C}{r_e}(V_{in1} - 0) = \frac{R_C}{r_e} V_{in1}$$

Similarly the positive voltage V_{in2} acting alone produces a negative output voltage, hence V_{in2} is called inverting input.

$$V_O = \frac{R_C}{r_e}(0 - V_{in2}) = -\frac{R_C}{r_e} V_{in2} .$$

Common mode Rejection Ratio :

An important characteristic of the dual input balanced output differential amplifier is its ability to supress undesired disturbances that might be amplified along with the desired signal.

when the matched pair of transistors is used in the differential amplifier, the unwanted signals would appear as common to both input bases, and the net output would be theoretically zero.

The practical effectiveness of rejecting the common signal depends on the degree of matching between the two common-emitter stages forming the differential amplifier.

In other words, the more closely equal are the currents in the input transistors Q_1 and Q_2 the better is the common mode signal rejection.

When the same voltage is applied to both input terminals of a differential amplifier, the differential amplifier is said to operate in the common mode configuration.

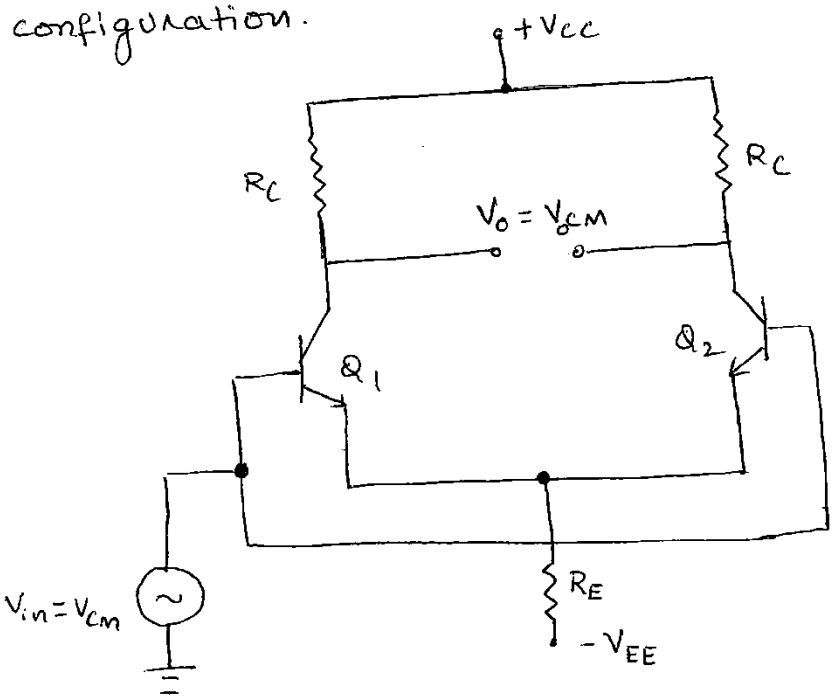


Figure: Differential amplifier in common mode configuration.

The ability of a differential amplifier to reject a common mode signal is expressed by its "common mode

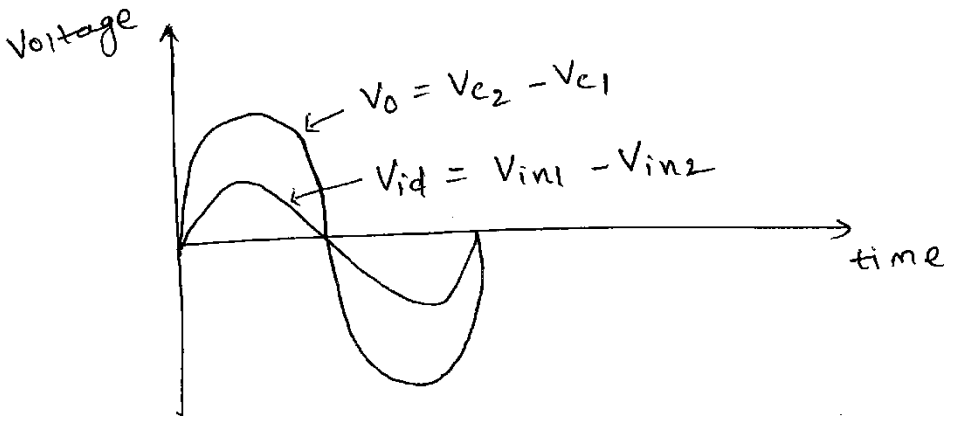
Rejection Ratio" (CMRR). It is the ratio of differential gain A_{DM} to the common mode gain A_{CM}

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

The common mode voltage gain A_{CM} can be as follows. The known voltage A_{CM} to both input terminals of the differential amplifier is applied as shown in figure above. Here $A_{CM} = \frac{V_{OCM}}{V_{CM}}$

Ideally A_{CM} to be zero that is $V_{OCM} = 0$ V. In other words CMRR is ideally infinity. Thus it is advantageous to use a differential amplifier with higher CMRR since this amplifier is better able to reject common mode signals.

Input output wave forms



Dual input unbalanced output Differential Amplifier :

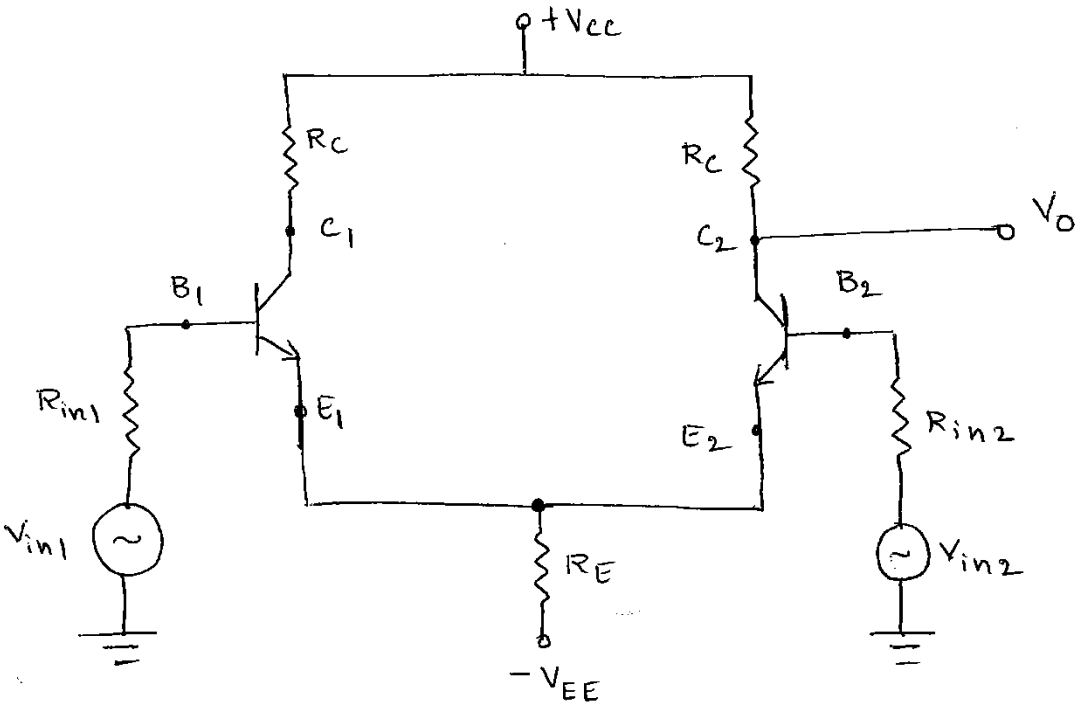
In this configuration two input signals are used. however the output is measured at only one of the two collectors with respect to ground. the output is refered to as an unbalanced output.

Let us assume that the output is measured at the collector of transistor Q_2 with respect to ground.

Dc Analysis :

$$I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_{in}}{\beta_{dc}}}$$

$$V_{CE} = V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C$$



Fig(a): Dual input unbalanced output Differential Amplifier

Ac Analysis : Fig below shows the ac equivalent circuit of the dual input, unbalanced output differential

amplifier with small signal T-equivalent models substituted for the transistors.

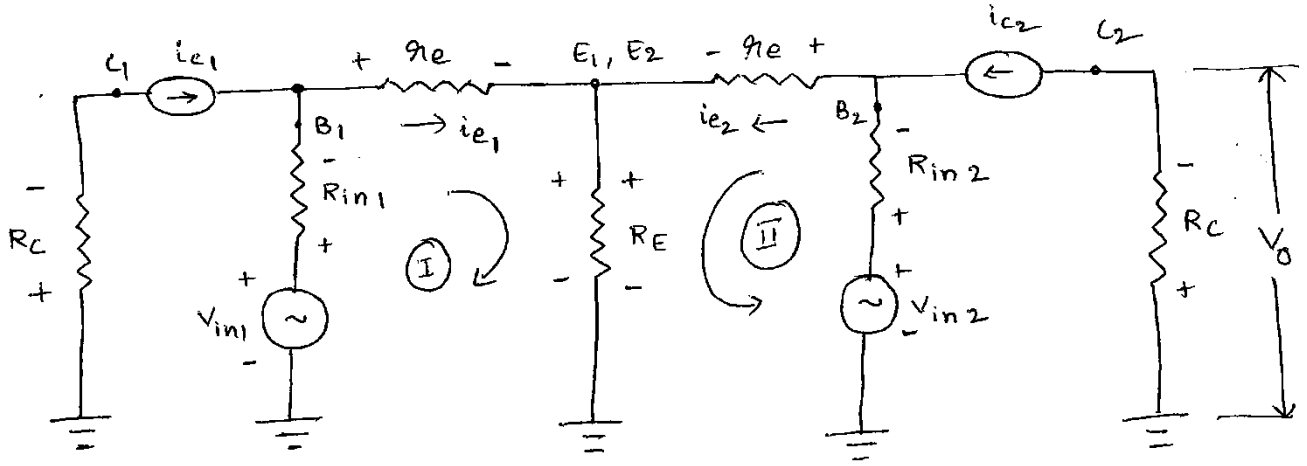


Fig (b) ; AC Equivalent circuit.

Voltage gain : writing KVL for loops (I) and II

$$V_{in1} = R_{in1} i_{b1} + r_e i_{e1} + R_E (i_{e1} + i_{e2})$$

$$V_{in2} = R_{in2} i_{b2} + r_e i_{e2} + R_E (i_{e1} + i_{e2})$$

$$i_{e1} = \frac{(r_e + R_E) V_{in1} - R_E V_{in2}}{(r_e + R_E)^2 - R_E^2}$$

$$i_{e2} = \frac{(r_e + R_E) V_{in2} - R_E V_{in1}}{(r_e + R_E)^2 - R_E^2}$$

$$V_o = V_{c2} = V_{cc} - i_{c2} R_C = -R_C i_{c2} = -R_C i_{e2}$$

$$V_o = -R_C \frac{(r_e + R_E) V_{in2} - R_E V_{in1}}{(r_e + R_E)^2 - R_E^2}$$

$$V_o = R_C \cdot \frac{R_E V_{in1} - (r_e + R_E) V_{in2}}{r_e (r_e + 2R_E)}$$

Generally $R_E >> r_e$, hence $r_e + R_E \simeq R_E$, $r_e + 2R_E \simeq 2R_E$

$$\therefore \quad V_o = R_c \frac{R_E V_{in1} - R_E V_{in2}}{2 r_e R_E}$$

$$V_o = \frac{R_c}{2 r_e} (V_{in1} - V_{in2})$$

$$A_d = \frac{V_o}{V_d} = \frac{R_c}{2 r_e}$$

Thus the voltage gain of the dual input unbalanced output differential amplifier is half the gain of the dual input balanced output differential amplifier.

Differential input resistance :

$$R_{i1} = R_{i2} = 2 \beta_{ac} r_e$$

Differential output resistance

$$R_{o1} = R_{o2} = R_c$$

Level Translator (Level shifting stage) :

Because of the direct coupling, the dc level at the emitters rises from stage to stage. This increase in dc level tends to shift the operating point of the succeeding stages and therefore limits the output voltage swing and may even distort the output signal.

The voltage at the output terminal of the second stage is well above ground (0v). This dc level is undesirable because it tends to limit the peak to peak output voltage swing without distortion and

also contributes to the error in the dc output signal.

Therefore a final stage should be included to shift the output dc level at the second stage down to about zero volts to ground. such a stage is referred to as a level translator or shifter. Thus in the cascaded differential amplifier, to shift the output dc level down to zero volts, the final stage must be followed by a level translator circuit.

A simplest level translator circuit is an emitter follower with a voltage divider circuit. is shown in figure below.

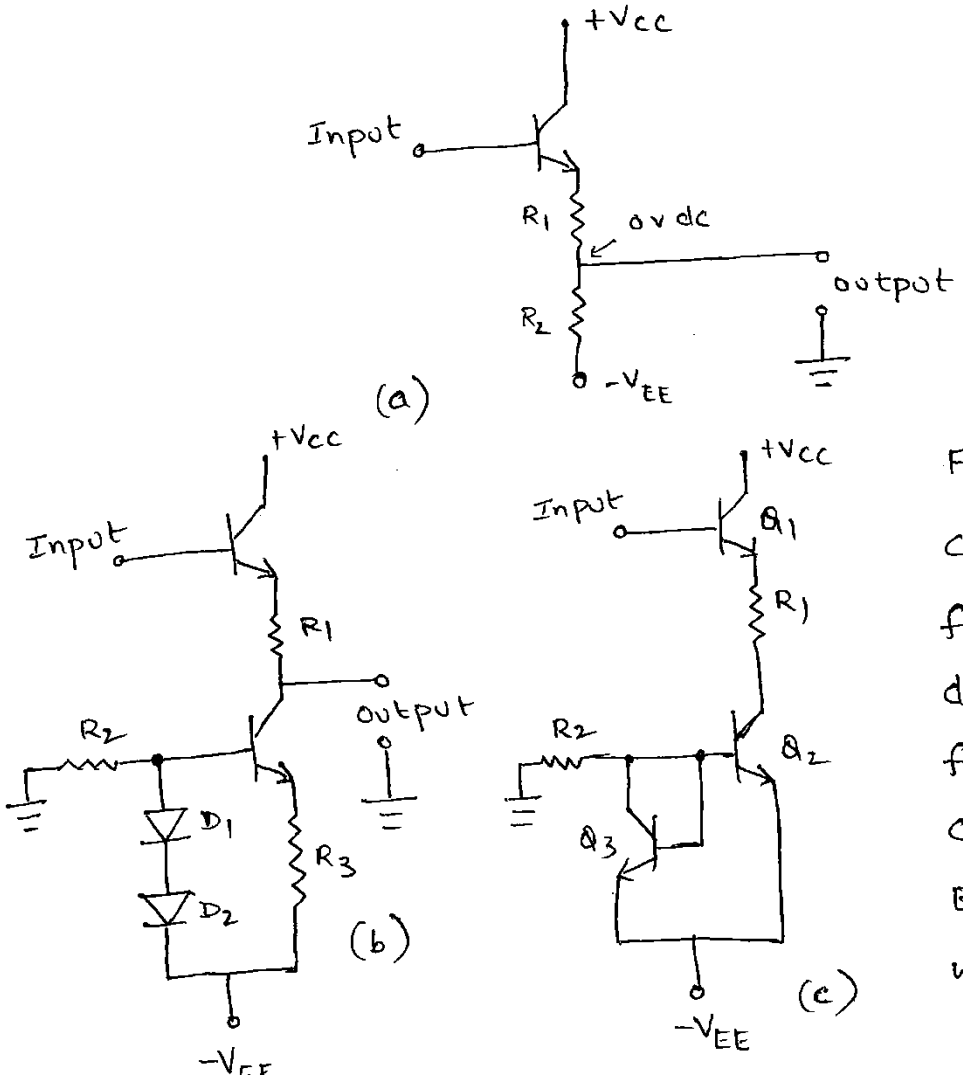
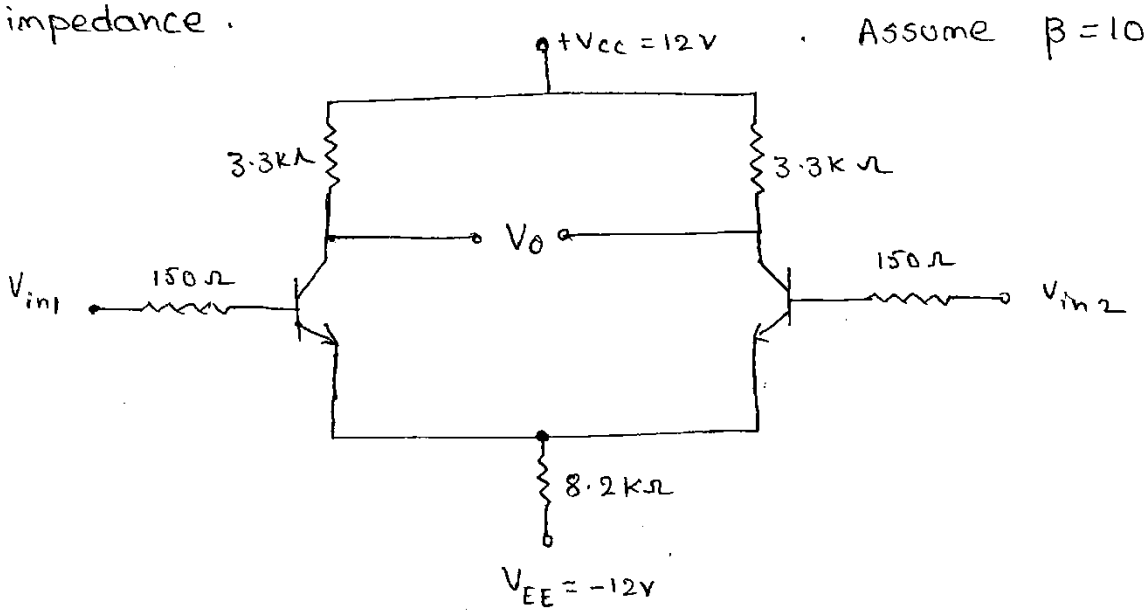


Fig: Level translator circuits (a) Emitter follower with voltage divider (b) Emitter follower with constant current bias (c) Emitter follower with current mirror.

Problem: For the differential amplifier shown in figure below. calculate

i) operating point 2) voltage gain 3) Input and output impedance. Assume $\beta = 100$



Solution: $R_C = 3.3k\Omega$, $R_{in} = 150\Omega$, $R_E = 8.2k\Omega$

$V_{cc} = 12V = -V_{EE}$, $\beta = 100$

i) $$I_E = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_{in}}{\beta}} = \frac{12 - 0.7}{\frac{150}{100} + 2 * 8.2 \times 10^3} = 0.688\,mA.$$

$$I_{CQ} = I_E = 0.688\,mA$$

$$V_{CEQ} = V_{cc} + V_{BE} - I_{CQ} R_C = 12 + 0.7 - \left(0.688 \times 10^{-3} \times 3.3 \times 10^3\right)$$

$$V_{CEQ} = 10.42V$$

(ii) $$r_e = \frac{25\,mV}{I_E} =$$

$$\therefore A_d = \frac{R_C}{r_e}$$

As the configuration is dual input balanced output

iii) $R_i = 2 h_{ie} \beta = 2 \times$

(iv) $R_O = R_C = 3.3 K\Omega$.

Problem: If the base currents for the emitter coupled transistors of a differential amplifier are 18μA and 22μA. Determine

i) Input bias current (ii) Input offset current for an op-Amp.

Solution: $I_{b_1}^{+} = 18\mu A$, $I_{b_2}^{-} = 22\mu A$

(i) Input bias current $I_b = \frac{I_{b_1}^{+} + I_{b_2}^{-}}{2} = \frac{18+22}{2} = 20\mu A$

(ii) Input offset current

$$I_{ios} = |I_{b_1}^{+} - I_{b_2}^{-}| = |18 - 22| = 4\mu A.$$

problem:

An op-Amp operates as a unity gain buffer with 3V (peak to peak) square wave input. If op-Amp is ideal with slew rate 0.5 V/μs. Find the maximum frequency of operation.

solution: $V_{p-p} = 3V \Rightarrow V_p = \frac{V_{p-p}}{2} = \frac{3}{2} = 1.5V$

$$f_{max} = \frac{\text{slew rate} \times 10^6}{2\pi V_p} = \frac{0.5 \times 10^6}{2\pi \times 1.5} = 53.05 KHz$$

Problem: A square wave of peak to peak amplitude of 750 mV has to be amplified to a peak to peak amplitude of 3.8V, with a rise time of 4.5 μsec or less. Can IC 741 op-Amp be used?

Solution: $SR = \frac{\Delta V}{\Delta t}$, IC 741 has $SR = 0.5\ V/\mu sec$

Now Rise time is the time required by the output to rise from 10% to 90% of its final value

$$\Delta V = (0.9 - 0.1)\ 3.8\ V = 3.04\ V.$$

$$\Delta t = 4.5\ \mu sec$$

$$SR = \frac{\Delta V}{\Delta t} = \frac{3.04V}{4.5\ \mu} = 0.675\ V/\mu sec.$$

The slew Rate of IC 741 is $0.5\ V/\mu sec$ which is too low compared to what is required. Hence IC 741 op-Amp Cannot be used.

Problem: In response to a square wave input, the output of an op-Amp changed from -3V to +3V over a time interval of $0.25\ V/\mu s$. Determine the slew Rate of the op-Amp.

Solution: change in output voltage = -3V to +3V

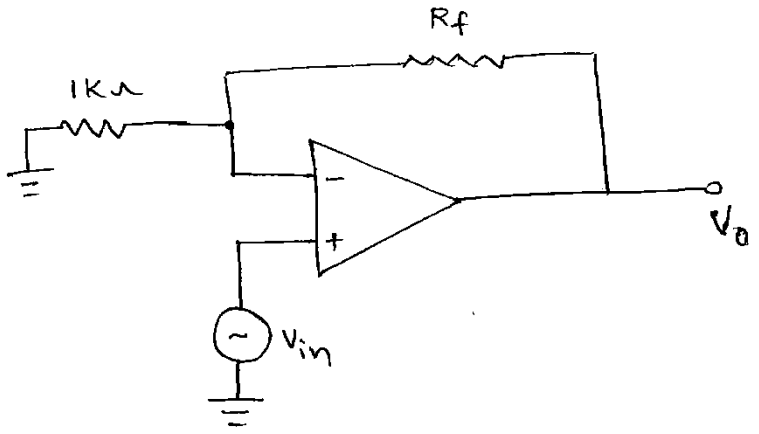
$$dV_0 = 3 - (-3) = 6V$$

$$dt = 0.25\ V/\mu s.$$

$$\text{slew Rate} = \frac{dV_0}{dt} = \frac{6}{0.25\ \mu s} = 24\ V/\mu s.$$

Problem: For the op-Amp configuration shown in figure below. the gain required is 61. Determine the appro-priate value of feedback resistor R_f.

solution:



solution: $\text{Gain} = 1 + \frac{R_f}{R_1} \Rightarrow 61 - 1 = \frac{R_f}{R_1}$

$R_f = 60\, R_1 = 60 \times 1K\Omega = 60K\Omega.$

Problem: For an op-Amp having a slew rate of $3\ V/\mu s$. what is the maximum closed loop voltage gain that can be used when the input signal varies by 0.4 V in 12 μsec ?

Solution: $V_o = A\, V_i$

$$\frac{dV_o}{dt} = A\,\frac{dV_i}{dt}$$

$$\text{Slew rate} = A\,\frac{dV_i}{dt} \Rightarrow A = \frac{SR}{\frac{dV_i}{dt}}$$

$$\Rightarrow A = \frac{\frac{3}{10^{-6}}}{\frac{0.4}{12 \times 10^{-6}}} = 90.$$

Problem: The common mode input to a certain differential amplifier, having differential gain of 125 is $4 \sin 200\pi t$ V. Determine the common mode output if CMRR is 60 dB.

Solution: The CMRR in dB is

$$60 = 20 \log \left| \frac{A_d}{A_c} \right|$$

$$\frac{A_d}{A_c} = 1000 \quad \Rightarrow \quad A_c = \frac{A_d}{1000} = \frac{125}{1000} = 0.125$$

Hence the common mode output is $= A_c V_c$

$$= 0.125 \left(4 \sin 200\pi t \right) = 0.5 \sin(200\pi t) \text{ V}$$

Problem: How fast can the output of an op-Amp change by 10V if its slew Rate is $1 \text{V}/\mu\text{s}$.

Solution:

$$SR = 1 \text{V}/\mu\text{s}$$

$$SR = \frac{\Delta V_o}{\Delta t} \quad \Rightarrow \quad \Delta t = \frac{\Delta V_o}{SR}$$

$$\Delta t = \frac{10 \text{V}}{1 \text{V}/\mu\text{s}} = 10 \, \mu\text{s}$$

Thus 10 μsec will be required by an op-Amp to change output by 10V.

UNIT - II

a) Linear Applications of OP-AMP

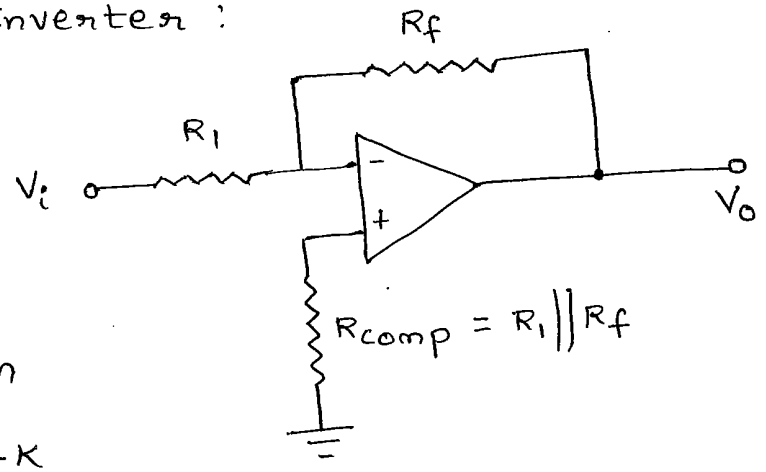
Inverting Amplifier : [Discussed in Unit - 1]

Non Inverting Amplifier : [Discussed in Unit - 1]

→ the inverting, Non inverting and differential configurations are useful in such applications as Summing, scaling and averaging amplifiers

1) Inverting Configuration :

a) scale changer / Inverter :



In the basic inverting amplifier if the ratio $\frac{R_f}{R_1} = K$

the closed loop gain

$$A_{CL} = \frac{-R_f}{R_1} = -K$$

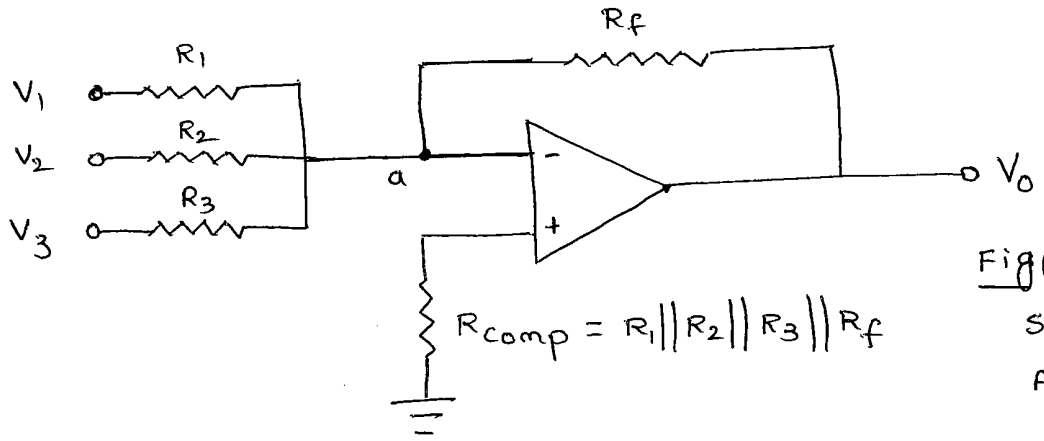
The circuit could be used to multiply by a Constant factor if R_f and R_1 are selected as precision resistors.

For $R_f = R_1$, $A_{CL} = -1$, and the circuit is called an inverter. ie. the output is 180° out of phase with respect to input though the magnitudes are same.

b) Summing Amplifier (Inverting) [Adder]

A typical summing amplifier with three input voltages V_1, V_2 and V_3, three input resistors

R_1, R_2, R_3 and a feedback resistor R_f as shown in figure below.



Fig(a): Inverting summing Amplifier

The following analysis is carried out assuming that the op-Amp is an ideal one ie $A_{OL} = \infty$ and $R_i = \infty$. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non inverting input terminal is at ground potential.

The voltage at node 'a' is zero as the non inverting input terminal is grounded. The nodal equation by KCL at node 'a' is

$$\frac{V_1 - 0}{R_1} + \frac{V_2 - 0}{R_2} + \frac{V_3 - 0}{R_3} = \frac{0 - V_0}{R_f}$$

$$\Rightarrow \quad V_0 = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right)$$

Hence the output is inverted and the weighted sum of the inputs.

If $R_1 = R_2 = R_3 = R_f \Rightarrow V_0 = -(V_1 + V_2 + V_3)$

Hence the output is inverted and sum of 3 inputs.

c) Average circuit :

In fig(a), if $R_1 = R_2 = R_3 = R$

$$\frac{R_f}{R} = \frac{1}{n} \Rightarrow n = \text{number of inputs}$$

If $n = 3 \Rightarrow \frac{R_f}{R} = \frac{1}{3}$

From fig(a) the output $V_0 = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$

$$\Rightarrow V_0 = -\left(\frac{R_f}{R} V_1 + \frac{R_f}{R} V_2 + \frac{R_f}{R} V_3\right)$$

$$V_0 = -\left(\frac{1}{3} V_1 + \frac{1}{3} V_2 + \frac{1}{3} V_2\right)$$

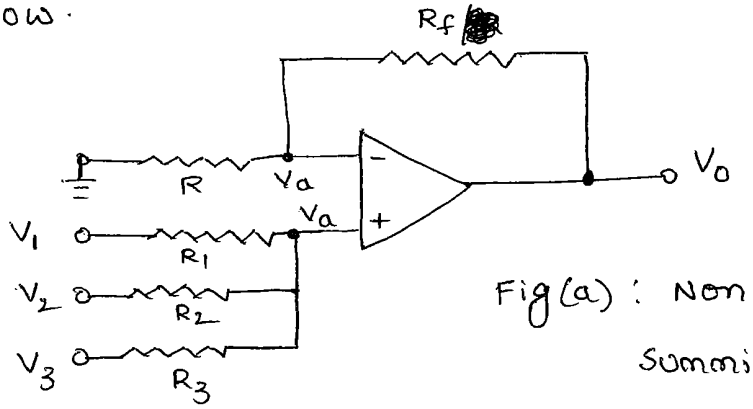
$$V_0 = -\left(\frac{V_1 + V_2 + V_3}{3}\right)$$

output is inverted, and average of three inputs.

② Non inverting configuration :

a) Summing Amplifier (Non inverting) [Adder] :

A summer that gives a non inverted sum is the non inverting summing amplifier. It is shown in figure below.



Fig(a) : Non inverting Summing Amplifier

Here $V_0 = \left(1 + \frac{R_f}{R}\right) V_a$

writing KCL at non inverting input

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

$$\Rightarrow V_a = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

Now Eq ① $\Rightarrow$ $V_0 = \left(1 + \frac{R_f}{R}\right) \left(\frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \right) \rightarrow ②$

V_0 is non inverted and weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R$, $R_f = 2R$

$$V_0 = (V_1 + V_2 + V_3)$$

output is Non inverted, sum of inputs

b) Averaging Amplifier:

From Eq ② Let $R_1 = R_2 = R_3 = R$

$$V_0 = \left(1 + \frac{R_f}{R}\right) \left(\frac{\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R}}{\frac{1}{R} + \frac{1}{R} + \frac{1}{R}} \right)$$

$$V_0 = \left(1 + \frac{R_f}{R}\right) \left(\frac{V_1 + V_2 + V_3}{3} \right)$$

V_0 is $\left(1 + \frac{R_f}{R}\right)$ times average of all three inputs.

problem: Design an adder circuit using an op-Amp to get the output expression as

$V_0 = -(0.1 V_1 + V_2 + 10 V_3)$ where V_1, V_2, V_3 are inputs

Solution: Given $V_o = -(0.1V_1 + V_2 + 10V_3)$

The output V_o of inverting summing amplifier

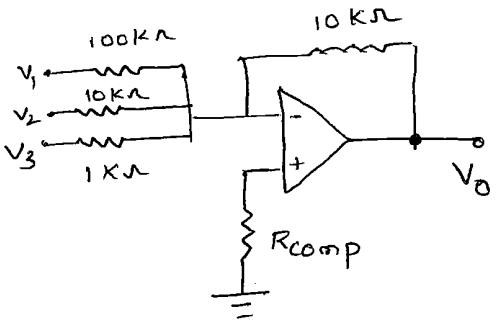
$$V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

Assume $R_f = 10\,K\Omega$

$\Rightarrow \frac{R_f}{R_1} = 0.1 \Rightarrow R_1 = 100\,K\Omega$

$\frac{R_f}{R_2} = 1 \Rightarrow R_2 = 10\,K\Omega$

$\frac{R_f}{R_3} = 10 \Rightarrow R_3 = 1\,K\Omega$



(3) Differential Configuration:

(a) subtractor:

A basic differential amplifier can be used as a subtractor as shown in figure below.

If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

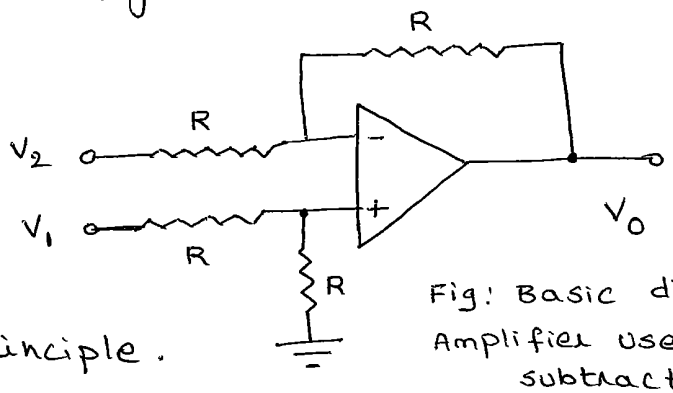
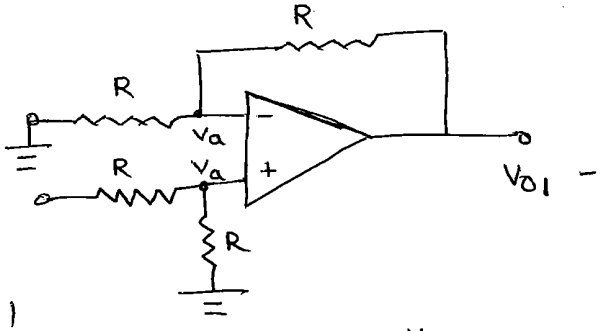


Fig: Basic differential Amplifier used as subtractor.

To find the V_{o1} due to V_1 alone make $V_2 = 0$



$V_{o1} = \left(1 + \frac{R}{R}\right)V_a = 2V_a$

$\frac{V_1 - V_a}{R} = \frac{V_a}{R} \Rightarrow V_a = \frac{V_1}{2}$

$\therefore V_{o1} = 2V_a = 2 \times \frac{V_1}{2} = V_1$

$\Rightarrow V_{o1} = V_1$

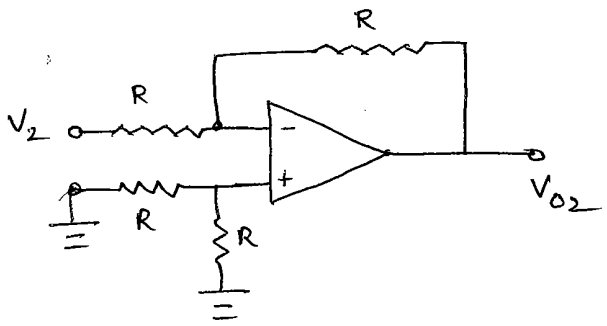
To find V_{02} due to V_2 alone make $V_1 = 0$

$$V_{02} = -\frac{R}{R} V_2$$

$$V_{02} = -V_2$$

$$\therefore \quad V_0 = V_{01} + V_{02}$$

$$V_0 = V_1 - V_2$$



Adder - Subtractor [summing Amplifier using differential configuration] :

the output voltage V_0 can be obtained by using superposition theorem.

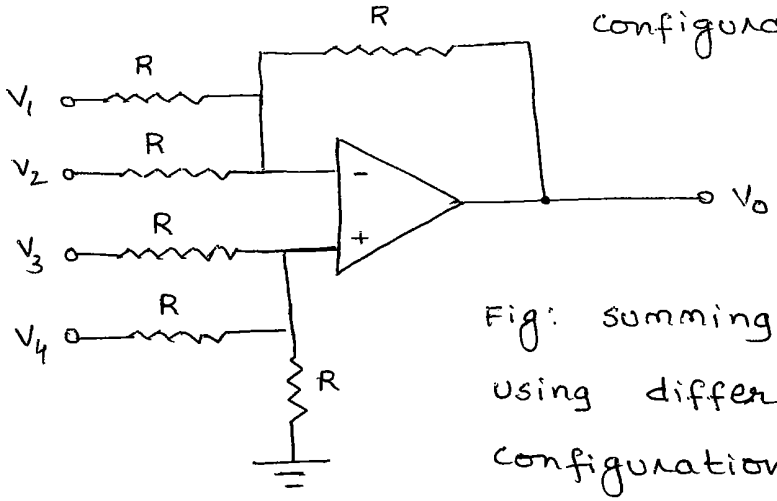


Fig: summing Amplifier using differential configuration.

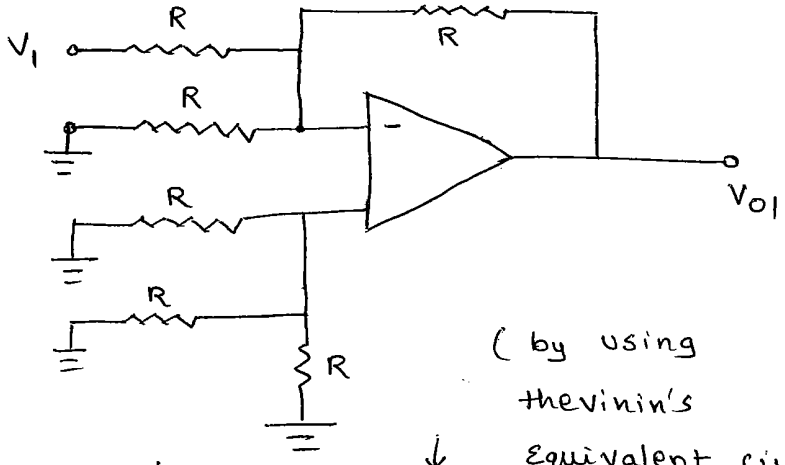
To find V_{01} due to V_1 alone make $V_2 = V_3 = V_4 = 0$

$$V_{01} = -\frac{R}{R/2} \times \frac{V_1}{2}$$

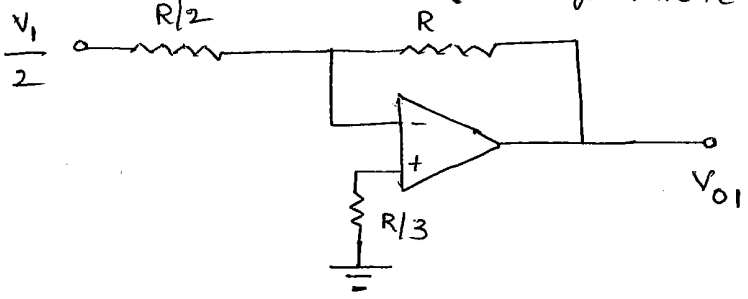
$$V_{01} = -V_1$$

Similarly, the output voltage V_{02} due to V_2 alone is

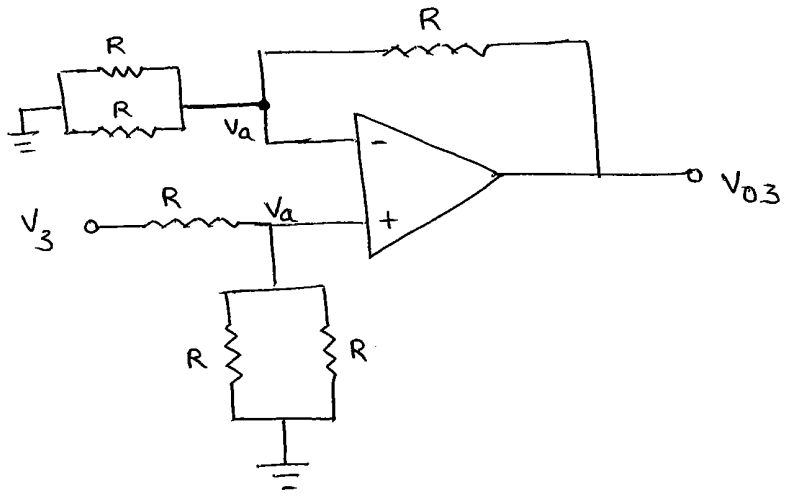
$$V_{02} = -V_2$$



(by using thevinin's Equivalent circuit)



To find V_{03} due to V_3 alone, make $V_1 = V_2 = V_4 = 0$



$$V_{03} = \left(1 + \frac{R}{R/2}\right) V_a$$

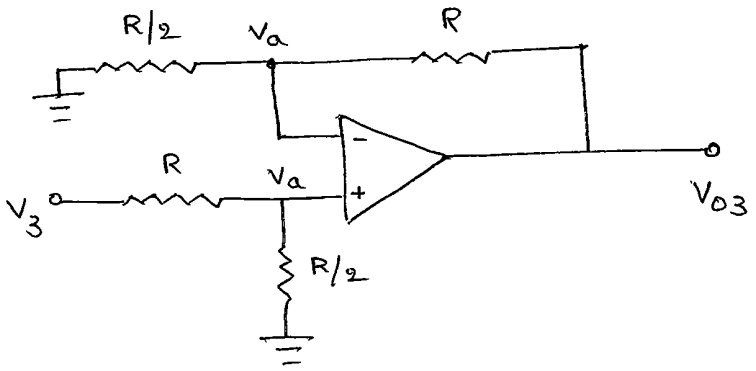
$$V_{03} = 3V_a \longrightarrow (1)$$

$$\frac{V_3 - V_a}{R} = \frac{V_a}{R/2}$$

$$V_3 = 3V_a \longrightarrow (2)$$

From (1) & (2)

$$V_{03} = V_3$$



Similarly to find V_{04} due to V_4 alone,

$$V_{04} = V_4$$

$$\therefore \quad V_0 = V_{01} + V_{02} + V_{03} + V_{04}$$

$$V_0 = -V_1 - V_2 + V_3 + V_4$$

$$V_0 = (V_3 + V_4) - (V_1 + V_2)$$

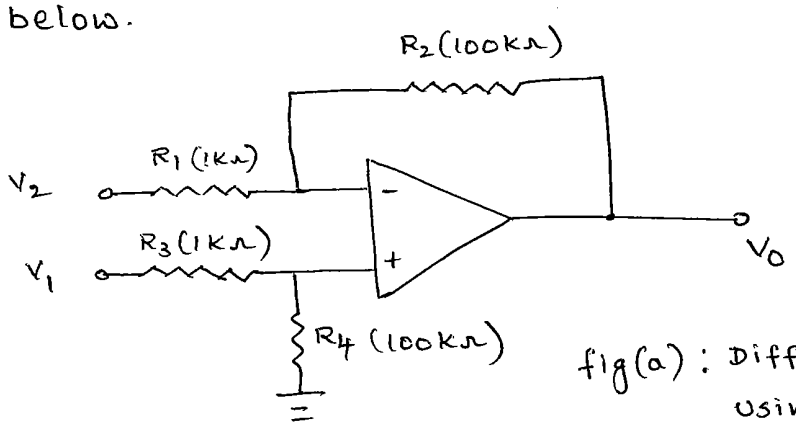
Instrumentation Amplifier

In a number of Industrial and Consumer applications, it is required to measure and control physical quantities. Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. These physical quantities are usually measured with the help of transducers. the output of

transducer has to be amplified, so that it can drive the indicator or display system. this function is performed by an instrumentation amplifier. The important features of an instrumentation amplifier are

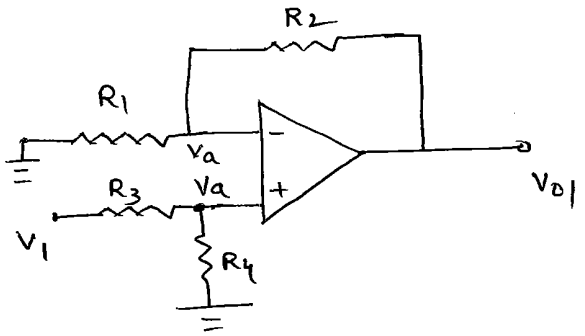
1) High gain accuracy
2) High CMRR
3) High gain stability with low temp co-efficient
4) Low dc offset
5) Low output impedance.

consider the basic differential amplifier shown in figure below.



fig(a): Differential Amplifier using single op-Amp

V_{o1} due to V_1 alone, make $V_2 = 0$



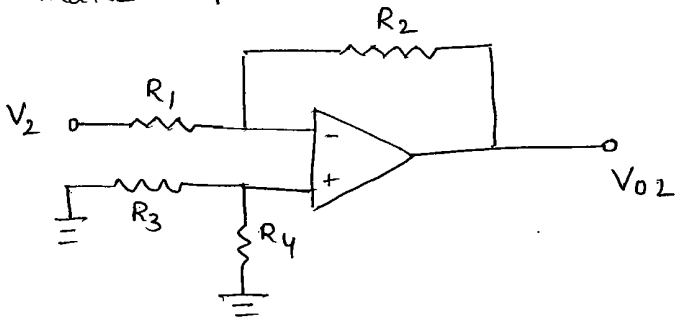
$$V_{o1} = \left(1 + \frac{R_2}{R_1}\right) V_a \longrightarrow (1)$$

$$\frac{V_1 - V_a}{R_3} = \frac{V_a}{R_4}$$

$$\frac{V_1}{R_3} = V_a\left[\frac{1}{R_3} + \frac{1}{R_4}\right] \Rightarrow V_a = \frac{V_1}{R_3\left[\frac{1}{R_3} + \frac{1}{R_4}\right]} = \frac{V_1}{1 + \frac{R_3}{R_4}} \longrightarrow (2)$$

from (1) $V_{o1} = \left(1 + \frac{R_2}{R_1}\right) V_1 \left(\frac{1}{1 + \frac{R_3}{R_4}}\right)$

V_{o2} due to V_2 alone, make $V_1 = 0$



$$V_{o2} = -\frac{R_2}{R_1} V_2$$

$$V_o = V_{o1} + V_{o2}$$

$$V_o = -\frac{R_2}{R_1} V_2 + V_1 \left(1 + \frac{R_2}{R_1}\right)\left(\frac{1}{1 + \frac{R_3}{R_4}}\right)$$

$$V_o = \frac{R_2}{R_1}\left[-V_2 + V_1 \frac{R_1}{R_2}\left(1 + \frac{R_2}{R_1}\right)\left(\frac{1}{1 + \frac{R_3}{R_4}}\right)\right]$$

$$V_o = \frac{R_2}{R_1}\left[V_1\left(1 + \frac{R_1}{R_2}\right)\frac{1}{\left(1 + \frac{R_3}{R_4}\right)} - V_2\right] \longrightarrow (1)$$

If $\frac{R_1}{R_2} = \frac{R_3}{R_4} \Rightarrow V_o = \frac{R_2}{R_1}(V_1 - V_2) \longrightarrow (2)$

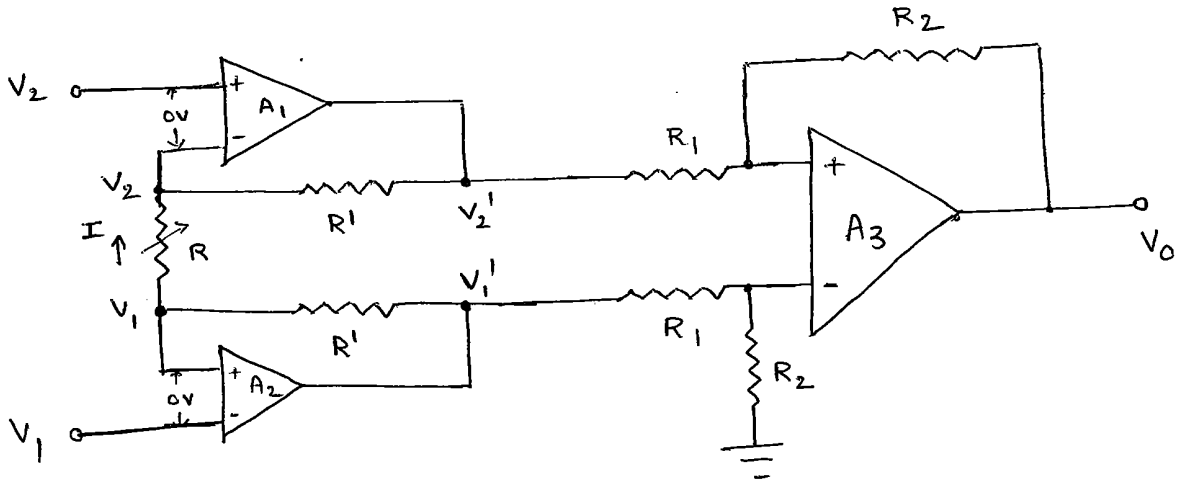
In fig(a) source V_1 sees an input impedance $= R_3 + R_4$ (101kΩ) and the impedance seen by source V_2 is only R_1 (1kΩ). this low impedance may load the signal source heavily. Therefore, high resistance buffer is used proceeding each input to avoid this loading effect as shown in fig(b) below.

The op-Amps A_1 and A_2 have differential input voltage as zero. For $V_1 = V_2$, that is, under common mode condition, the voltage across R will be zero. As no current flows through R and R' the non inverting amplifier A_1 acts as voltage follower, so its output $V_2' = V_2$

Similary $V_1' = V_1$.

However if $V_1 \neq V_2$, current flows in R and R' and

$(V_2' - V_1') > (V_2 - V_1)$. Therefore this circuit has differential gain and CMRR more compared to the single op-Amp circuit (fig(a)). The output voltage V_0 can be calculated as follows.



Fig(b): An improved instrumentation Amplifier

Compare op-Amp-3 with op-Amp in fig(a), then output V_0 can be written as [by comparing eq(1)]

$$V_0 = \frac{R_2}{R_1}\left[V_1' \left(1 + \frac{R_1}{R_2}\right) \frac{1}{\left(1 + \frac{R_1}{R_2}\right)} - V_2' \right]$$

$$V_0 = \frac{R_2}{R_1}\left(V_1' - V_2'\right) \longrightarrow (3)$$

Since no current flows into op-Amp, the current I flowing (upwards) in R is $I = \frac{V_1 - V_2}{R}$ and passes through the resistor R'.

$$V_2 = I R' + V_2' \Rightarrow V_2' = V_2 - I R' = V_2 - \left(\frac{V_1 - V_2}{R}\right) R'$$

$$\therefore V_2' = -\frac{R'}{R}(V_1 - V_2) + V_2 \longrightarrow (4)$$

Illy $V_1 = -I R' + V_1' \Rightarrow V_1' = V_1 + I R' = V_1 + \left(\frac{V_1 - V_2}{R}\right) R'$

$$\therefore V_1' = \frac{R'}{R}(V_1 - V_2) + V_1 \longrightarrow (5)$$

From Eq's (4) and (5), Eq (3) becomes

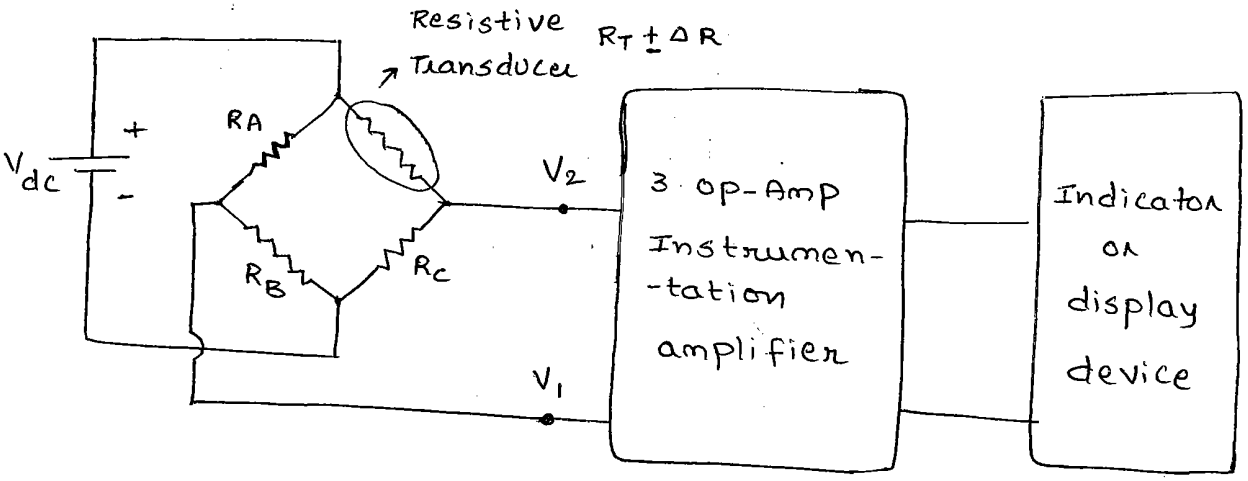
$$V_0 = \frac{R_2}{R_1}\left[\frac{R'}{R}(V_1 - V_2) + V_1 + \frac{R'}{R}(V_1 - V_2) - V_2\right]$$

$$V_0 = \frac{R_2}{R_1}\left[\frac{2R'}{R}(V_1 - V_2) + (V_1 - V_2)\right]$$

$$V_0 = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)(V_1 - V_2) \longrightarrow (6)$$

In Eq (6), if we choose $R_2 = R_1 = 25\,k\Omega$, $R' = 25\,k\Omega$, $R = 50\Omega$ then a gain of 1001 can be achieved. the difference gain of this instrumentation amplifier can be varied by replacing the resistance R by a potentiometer in fig(b). the resistance R, however should never be made zero, as this will make the gain infinity. To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R.

Figure (c) below shows a differential instrumentation amplifier using transducer bridge.



Fig(c): Instrumentation amplifier using transducer bridge

The circuit uses a resistive transducer whose resistance changes ch as a function of the physical quantity to be measured. the bridge is initially balanced

by a dc supply voltage V_{dc} so that $V_1 = V_2$. As the physical quantity changes, the resistance R_T of the transducer also changes, causing an unbalance in the bridge ($V_1 \neq V_2$). This differential voltage now gets amplified by the three op-Amp differential instrumentation Amplifier.

There are a number of practical applications of instrumentation amplifier with the transducer bridge, such as temperature indicator, temperature controller, light intensity meter etc.

Instrumentation Amplifier using Transducer Bridge (ex: Temperature measurement):

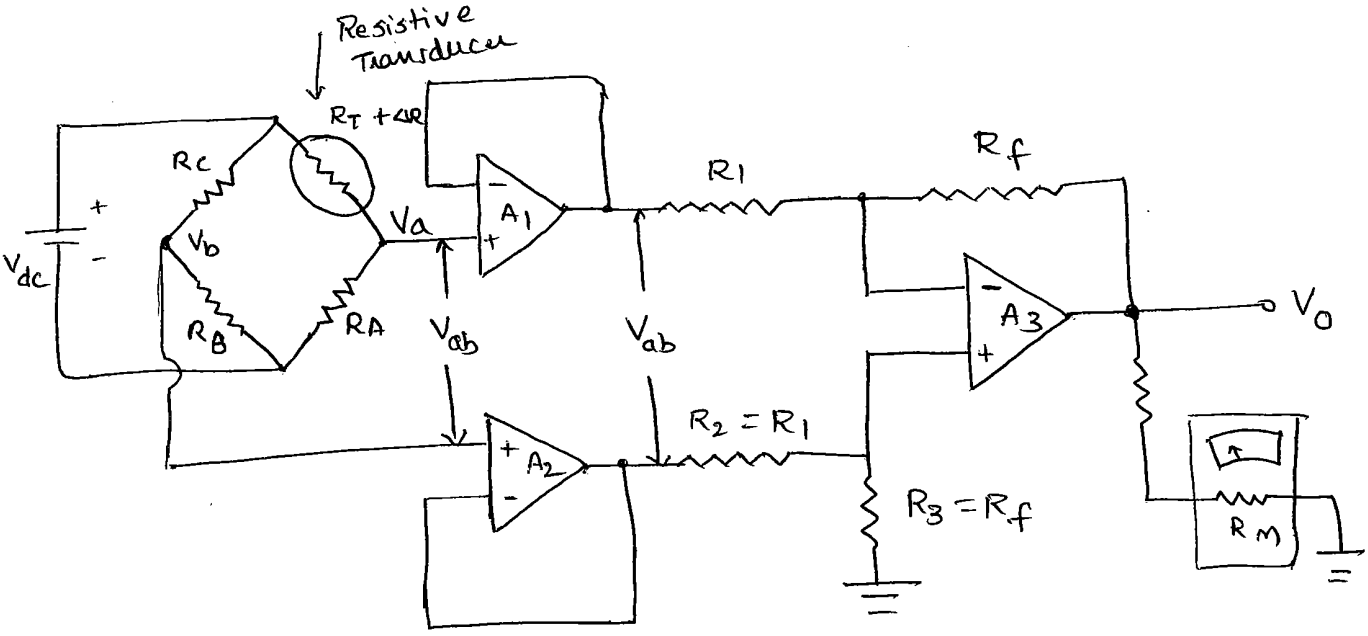


Fig: Differential instrumentation amplifier using a transducer bridge.

Figure shows a simplified differential instrumentation amplifier using a transducer bridge. A resistive transducer whose resistance changes as a

function of some physical energy is connected in one arm of the bridge with a small circle around it and is denoted by $(R_T \pm \Delta R)$ where R_T is the resistance of the transducer and ΔR the change in resistance R_T

The bridge in the circuit is dc excited but could be ac excited as well. For the balanced bridge at some reference condition

$$V_b = V_a$$

$$\frac{R_b V_{dc}}{R_B + R_C} = \frac{R_A V_{dc}}{R_A + R_T} \Rightarrow \frac{R_C}{R_B} = \frac{R_T}{R_A}.$$

Generally resistors R_A, R_B and R_C are selected so that they are equal in value to the transducer resistance at some reference condition.

The bridge is balanced initially at a desired reference condition. However as the physical quantity to be measured changes, the resistance of the transducer also changes, which causes the bridge to unbalance. $(V_a \neq V_b)$

Let the change in resistance of transducer be ΔR. then

$$V_a = \frac{R_A V_{dc}}{R_A + (R_T + \Delta R)}$$

$$V_b = \frac{R_B V_{dc}}{R_B + R_C}$$

$$V_{ab} = V_a - V_b$$

$$= \frac{R_A V_{dc}}{R_A + R_T + \Delta R} - \frac{R_B V_{dc}}{R_B + R_C}$$

However if $R_A = R_B = R_C = R_T = R$, then

$$V_{ab} = -\frac{\Delta R V_{dc}}{2(2R + \Delta R)}$$

The negative sign indicates that $V_a < V_b$ because of the increase in the value of R_T.

Temperature indicator: the above circuit can be used as a temperature indicator if the transducer in the bridge circuit is a thermistor and the output meter is calibrated in degrees celcius or Fahrenheit. the bridge can be balanced at a desired reference condition (ex 25°c). As the temperature varies from its reference value, the resistance of the thermistor changes and the bridge becomes unbalanced. This unbalanced bridge inturn produces the meter movement. the meter can be calibrated to read a desired temp range by selecting an appropriate gain for the differential instrumentation Amplifier. [meter movement α ΔV_o, ΔV_o α ΔR]

Here ΔR = temp co-efficient of resistance (final temp - ref temp)

Ac Amplifier:

The inverting and non-inverting op-Amp Amplifier respond to both ac and dc signals. But to get the ac frequency response of an op-Amp or if the ac input signal is superimposed with dc level, it becomes essential to block the dc component. this is achieved by using an AC amplifier with a coupling capacitor.

Ac amplifiers are of two types

1. Inverting ac Amplifier.
2. Non inverting ac Amplifier.

1. Inverting Ac amplifier:

The circuit of inverting ac Amplifier is shown in figure below.

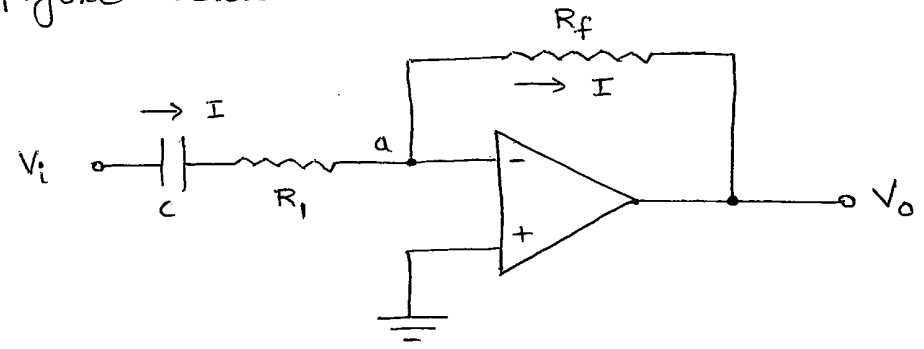


Fig : Inverting Ac Amplifier

$$I = \frac{V_i - V_a}{R_1 + \frac{1}{sC}} = \frac{V_i}{R_1 + \frac{1}{sC}} \longrightarrow (1)$$

$$\text{Again} \quad I = \frac{V_a - V_o}{R_f} \Rightarrow \frac{-V_o}{R_f} \longrightarrow (2)$$

From (1) and (2)

$$\frac{-V_o}{R_f} = \frac{+V_i}{R_1 + \frac{1}{sC}}$$

$$\frac{V_0}{V_i} = \frac{-R_f}{R_1 + \frac{1}{sC}} = -\frac{R_f}{R_1}\left(\frac{1}{1+\frac{1}{sR_1C}}\right)$$

$$A_{CL} = \frac{-R_f}{R_1}\left(\frac{s}{s\left(1+\frac{1}{sR_1C}\right)}\right)$$

$$A_{CL} = \frac{-R_f}{R_1}\left(\frac{s}{s+\frac{1}{R_1C}}\right)$$

$$\left[\frac{-R_f}{R_1}\left(\frac{1}{1+\frac{1}{j2\pi f R_1 C}}\right)\right]$$

$$\left[\frac{-R_f}{R_1}\left(\frac{1}{1-j\left(\frac{f_L}{f}\right)}\right)\right]$$

Here the lower 3dB frequency $f_L = \frac{1}{2\pi R_1 C}$

In the mid-band range of frequencies, capacitor C behaves as a short circuit and

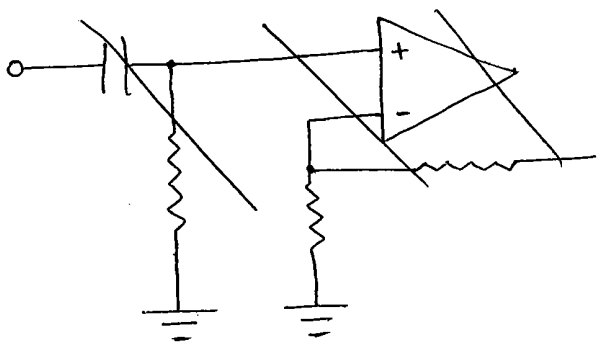
$$A_{CL} = \frac{-R_f}{R_1}$$

Here the coupling capacitor 'C' not only blocks the dc voltage, but also sets the low frequency cut-off limit which is given by

$$f_L = \frac{1}{2\pi R_1 C}$$

Non-inverting AC Amplifier:

The circuit of Non-inverting AC amplifier is shown in figure below



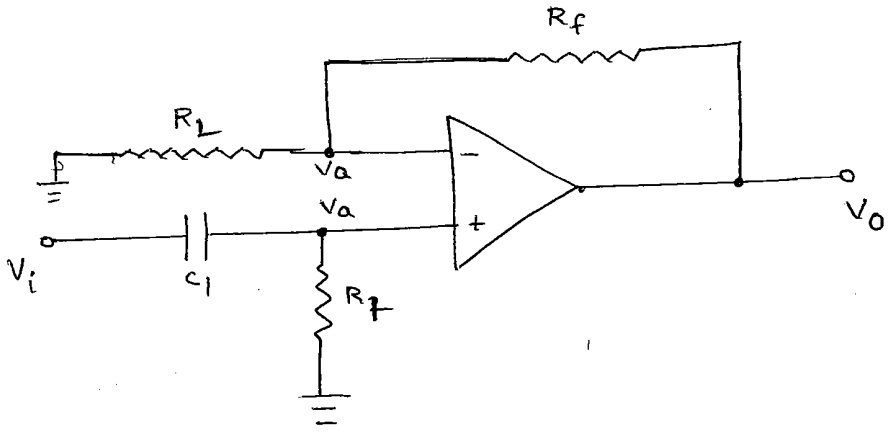


Fig : Non-Inverting Ac Amplifier

Here a resistor R_2 is ~~provided~~ added to provide a dc return to ground. However this reduces overall input impedance of the amplifier, which now approximately R_2.

$$\text{Here} \quad V_o = \left(1 + \frac{R_f}{R_1}\right) V_a \longrightarrow (1)$$

$$\text{and} \quad \frac{V_i - V_a}{\frac{1}{j\omega C_1}} = \frac{V_a}{R_2} \Rightarrow V_i - V_a = \frac{V_a}{j\omega C_1 R_2}$$

$$V_i = V_a\left(1 + \frac{1}{j\omega C_1 R_2}\right)$$

$$V_a = \frac{j\omega C_1 R_2}{1 + j\omega C_1 R_2} V_i \longrightarrow (2)$$

from (1) and (2)

$$V_o = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{j\omega C_1 R_2}{1 + j\omega R_1 C_1}\right) V_i$$

$$V_o = \left(1 + \frac{R_f}{R_2}\right)\left(\frac{j\omega C_1 R_1}{1 + j\,2\pi f R_1 C_1}\right) V_i$$

$$V_o = \left(1 + \frac{R_f}{R_2}\right)\left(\frac{j\,2\pi f R_1 C_1}{1 + j\left(\frac{f}{f_L}\right)}\right) V_i$$

$$A_{OF} = \left(1 + \frac{R_f}{R_2}\right) \quad \text{where} \quad f_L = \frac{1}{2\pi R_1 C_1}$$

The problem of low input impedance is eliminated by connecting a capacitor C_3 as shown in figure below. capacitor C_2 is large enough to act as short circuit to ac signals. the non inverting terminal and the node 'n' will be almost at the same potential so that R_1 carries almost no current. Hence the circuit will have an extremely high input impedance.

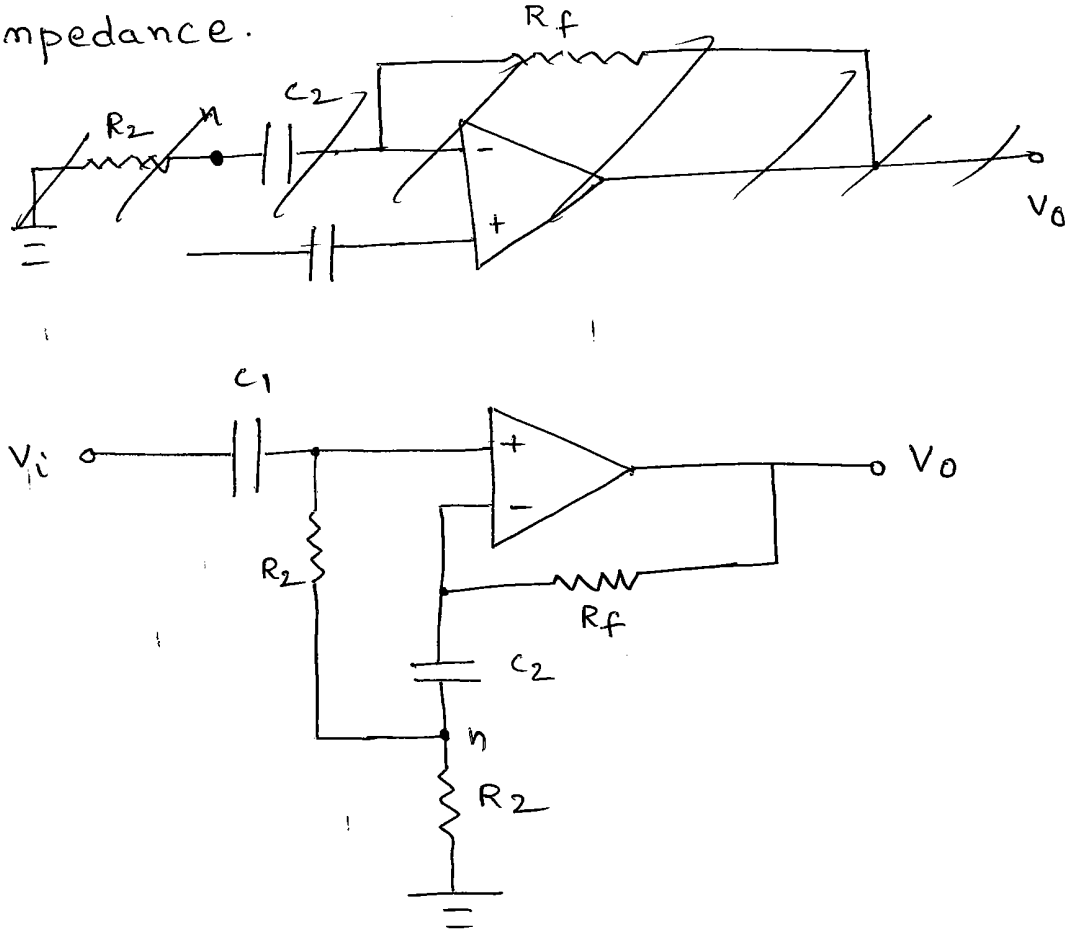


Fig: High input impedance non-inverting ac Amplifier.

Voltage to Current Converter (V to I Converter) :

1) Voltage to Current converter with floating load :

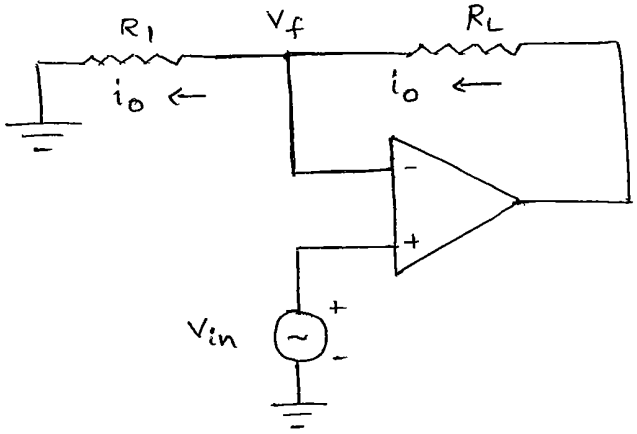


Fig: V to I Converter with floating load

Figure shows a voltage to current converter in which load resistor R_L is floating (not connected to ground). The input voltage is applied to the non-inverting input terminal, and the feedback voltage across R_1 drives the inverting input terminal. This circuit is also called a current series negative feedback amplifier because the feedback voltage across R_1 depends on the output current i_o.

Here $V_{in} = V_f$

$$V_{in} = R_1 i_o \quad (or) \quad i_o = \frac{V_{in}}{R_1}$$

so an input voltage V_{in} is converted in to an output current of $\frac{V_{in}}{R_1}$. In other words, input voltage V_{in} appears across R_1.

If R_1 is a precision resistor, the output current ($i_o = \frac{V_{in}}{R_1}$) will be precisely fixed.

Applications of V to I Converter with floating load

1. Low voltage dc and ac voltmeters
2. LED's 3. Zener diode testers.

Low voltage DC voltmeter

the V to I Converter with floating load can be modified as a low voltage dc voltmeter circuit. the resistance R_L is to be replaced by D'Arsonal meter movement. this is shown in figure below.

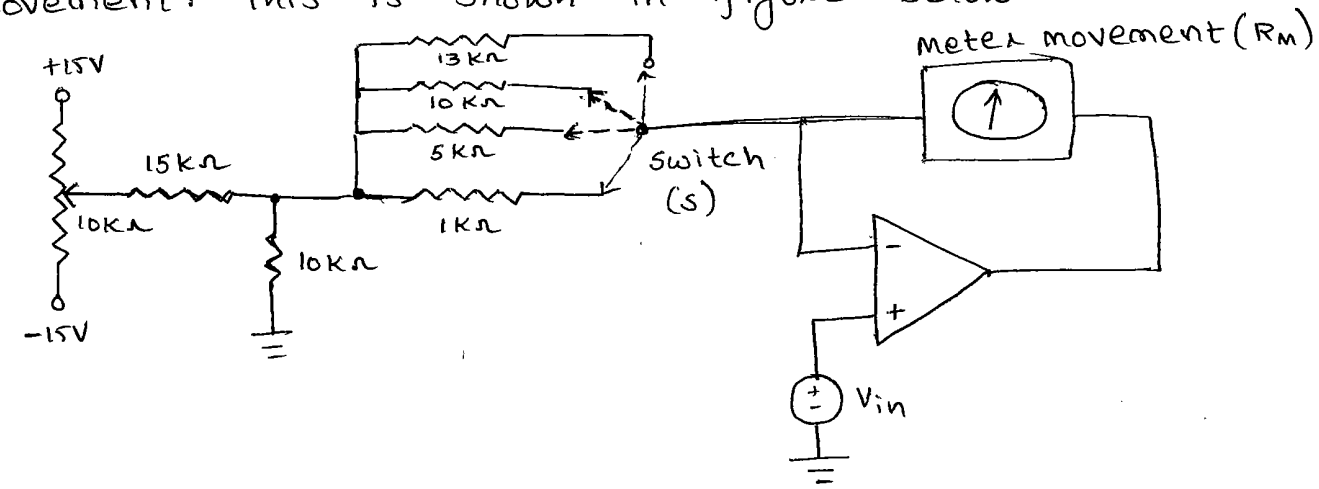


Fig: DC voltmeter

For accurate reading it is necessary to make the nulling of op-Amp. this is done by offset voltage compensating network. let R_m be the meter resistance. the effective thevinin's equivalent of compensating network is 10Ω.

when switch S is in position 1, the effective R_1 is $1K\Omega + 10\Omega \simeq 1K\Omega$

Let $V_{in} = 1V$ then, $I_0 = \frac{V_{in}}{R_1} = \frac{1V}{1K\Omega} = 1mA$.

Input of 1V result full scale deflection, if meter has full scale deflection current of 1mA.

when switch is in position 2 then $R_1 = 5K\Omega$.

Thus for full scale deflection

$$1 \times 10^{-3} = \frac{V_{in}}{5 \times 10^3} \Rightarrow V_{in} = 5V$$

Thus 5V are required to cause full scale deflection. Thus range of voltmeter increases by 5. Similarly at positions 3 and 4, rangers of X10 and X13 are also obtained.

For ±15 V supply, Maximum input voltage swing is ±14 V, hence with ±15 V supply, maximum range possible is X13.

Here meter Resistance R_m doesn't affect the value of I_0. Thus meter can be calibrated properly to measure dc voltages.

Current to Voltage converter:

In this converter the output voltage is proportional to the input current. It accepts an Input current I_s and yields an output voltage V_o such that $V_o = A I_s$. where A is the gain of the circuit.

Figure below shows the current to voltage converter Here $V_A = 0$

Since the inverting input terminal is at Virtual ground, no current flows through R_s and current

I_s flows the feedback resistor R_f. Thus the output voltage is

$$I_s = \frac{0 - V_o}{R_f} = \frac{-V_o}{R_f}$$

$$V_o = -I_s R_f \qquad [V_o \propto I_s]$$

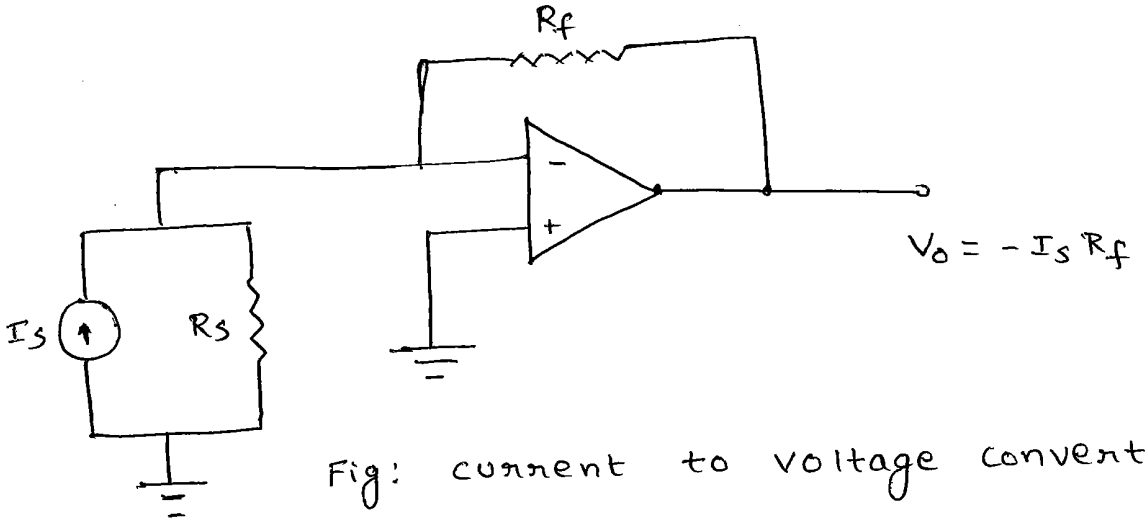


Fig: current to voltage converter

Thus output voltage is proportional to the input current and circuit works as a current to voltage converter. this circuit is also referred as current controlled voltage source.

Here the proportionality factor is R_f (Resistance)

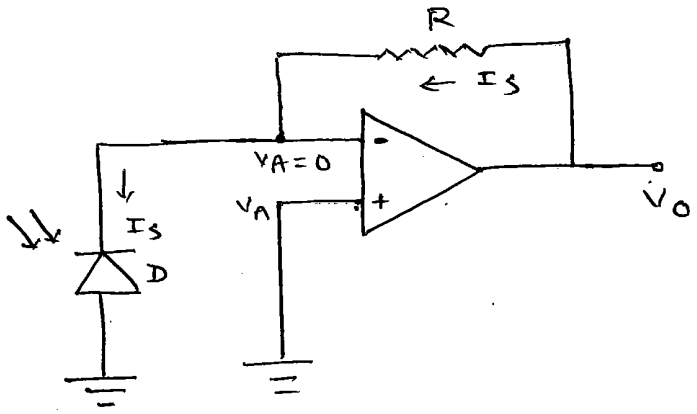
Because of this, I-V converters are also called Transresistance Amplifiers.

Applications:

photo cell, photo diode and photo voltaic cell give an output current that is proportional to an incident radiant energy or light. The current through these devices can be converted to voltage

by using a current to voltage converter and there by the amount of light or radiant energy incident on the photo device can be measured.

Photo diode Detector:



The photo diode produces electrical current in response to incident light. This current flows through R.

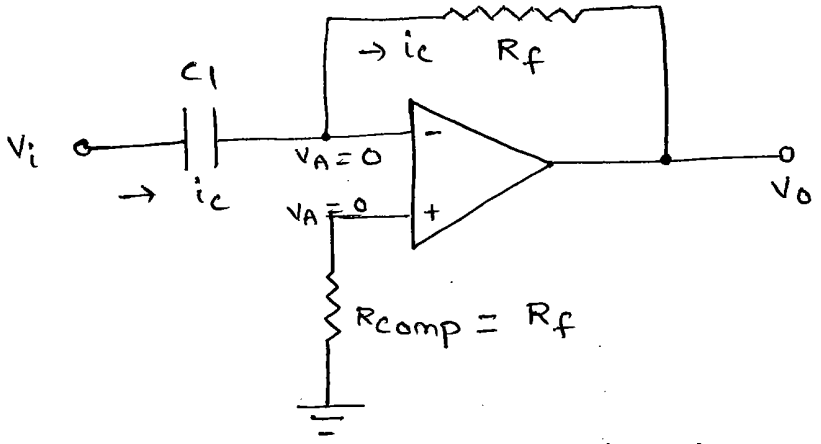
$$I_S = \frac{V_O - V_A}{R} = \frac{V_O}{R}$$

$$V_O = I_S R .$$

The output voltage is proportional to the diode current.

Differentiator:

One of the simplest of the op-Amp circuits that contain capacitor is the differential amplifier. As the name suggests, the circuit performs the mathematical operation of differentiation, that is the output waveform is the derivative of the input waveform. A differentiator circuit is shown in figure below.



the current $i_c = C_1 \frac{d}{dt}(V_i - V_A) = +C_1 \frac{dV_i}{dt} \rightarrow (1)$

$$i_c = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f} \longrightarrow (2)$$

from (1) and (2)

$$\frac{-V_o}{R_f} = C_1 \frac{dV_i}{dt}$$

$$\boxed{V_o = -R_f C_1 \frac{dV_i}{dt}}$$

thus the output voltage V_o is a constant $(-R_f C_1)$ times the derivative of the input voltage V_i and the circuit is a differentiator.

Illy $V_o(s) = -R_f C_1 \, s \, V_i(s)$

$$\frac{V_o(s)}{V_i(s)} = -R_f C_1 \, s$$

$$A = \frac{V_o(j\omega)}{V_i(j\omega)} = -R_f C_1 \, j\omega = -j 2\pi f R_f C_1$$

$$A = -j \frac{f}{fa} \quad \text{where} \quad fa = \frac{1}{2\pi R_f C_1}$$

the $|A| = \frac{f}{fa}$

The gain in dB $= 20 \log|A| = 20 \log\left|\frac{f}{fa}\right|$

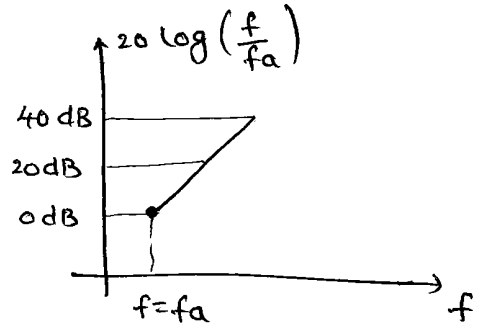
Let $fa = 10$

$fa = 10$, $f = 10$ then $20 \log\left|\frac{f}{fa}\right| = 20 \log 1 = 0$ dB

$fa = 10$, $f = 100$, then $20 \log\left|\frac{100}{10}\right| = 20$ dB

$fa = 10$, $f = 1000$, then $20 \log\left|\frac{1000}{10}\right| = 40$ dB.

So for every decade the gain increases at a rate of +20 dB/decade. Thus at high frequency, a differen-tiator may become unstable and break in to oscillation.



there is one more problem in the ideal differentia-tor circuit is if frequency increases, the reactance of the capacitor decreases, there by making the circuit sensitive to high frequency noise. these problems can be corrected using some additional parameters in the basic differentiator circuit. such a circuit is called practical differentiator circuit.

practical Differentiator:

The noise and stability at high frequency can be corrected, in the practical differentiator circuit using the resistance R_1 in series with C_1

and the capacitor C_f in parallel with resistance R_f. the circuit is shown in figure below.

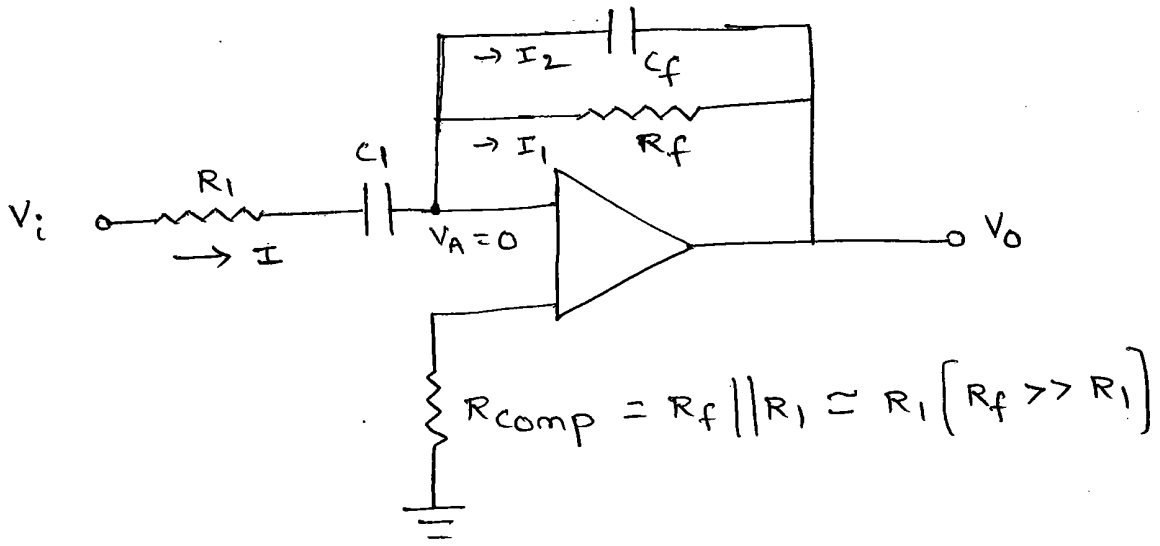


Fig: practical Differentiator circuit.

Here $I = \frac{V_i - V_A}{Z} = \frac{V_i}{Z}$

$$Z = R_1 + \frac{1}{sC_1} = \frac{1 + sR_1C_1}{sC_1}$$

$$I = \frac{V_i(s)\, sC_1}{1 + sR_1C_1} \longrightarrow (1)$$

$$I_1 = \frac{V_A - V_o(s)}{R_f} = \frac{-V_o(s)}{R_f} \longrightarrow (2)$$

$$I_2 = C_f \frac{d}{dx}\left(-V_o(s)\right) \Rightarrow -sC_f$$

$$I_2 = C_f\, s\, -V_o(s) = -s\, C_f\, V_o(s) \longrightarrow (3)$$

But from the circuit $I = I_1 + I_2$

$$V_i(s)\, \frac{sC_1}{1 + sR_1C_1} = -\frac{V_o(s)}{R_f} - s\, C_f\, V_o(s)$$

$$\Rightarrow \frac{V_o(s)}{V_i(s)} = \frac{-sR_f C_1}{(1 + sR_1C_1)(1 + sR_f C_f)}$$

As $R_f C_f = R_1 C_1$

$$\frac{V_o(s)}{V_i(s)} = \frac{-sR_f C_1}{(1+sR_1C_1)^2}$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j\omega R_f C_1}{(1+j\omega R_1 C_1)^2}$$

$$A = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j\,2\pi f R_f C_1}{(1+j\,2\pi f R_1 C_1)^2}$$

Let $f_a = \frac{1}{2\pi R_f C_1}$, $f_b = \frac{1}{2\pi R_1 C_1}$

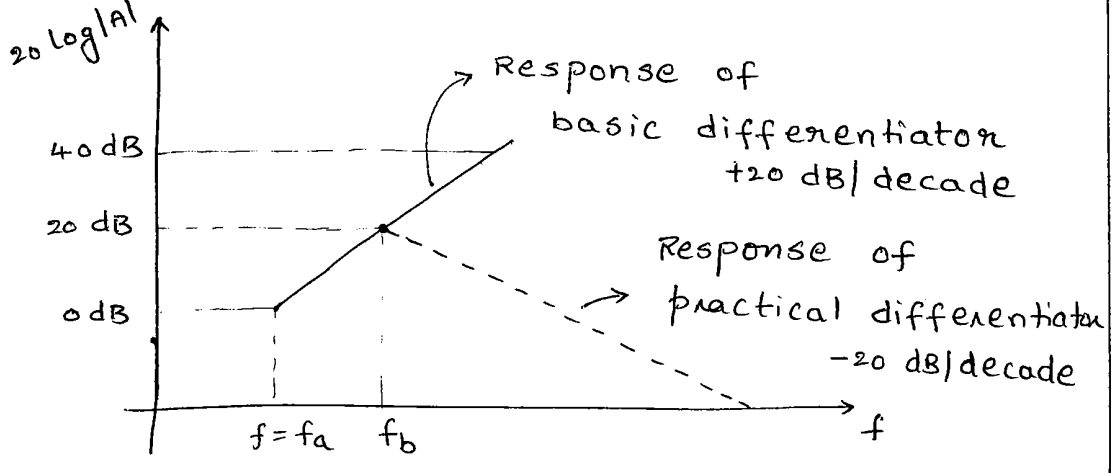
$$A = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j\left(\frac{f}{f_a}\right)}{\left(1+j\frac{f}{f_b}\right)^2}$$

$$|A| = \frac{\frac{f}{f_a}}{1+\left(\frac{f}{f_b}\right)^2}$$

As $R_f C_1 >> R_1 C_1$

$f_a < f_b$.

From the above equation it is evident that the gain increases at +20 dB/decade for frequency $f < f_b$ and decreases at -20 dB/decade for $f > f_b$



combination of R_1C_1 and $R_f C_f$ help to reduce effectively the impact of high frequency noise and offsets

A good differentiator may be designed as per the following steps

1. choose f_a equal to the highest frequency of the input signal. Assume a practical value of C_1 ($< 1\mu F$) and then calculate R_f.

2. choose $f_b = 10 f_a$. Now calculate the values of R_1 and C_f so that $R_1C_1 = R_f C_f$

problem:

a) Design an op-Amp Differentiator that will differen-tiate an input signal with $f_{max} = 100\,Hz$

b) Draw the output waveform for a sine wave of 1V peak at 100Hz applied to the differentiator.

solution:

a) select $f_a = f_{max} = 100\,Hz = \frac{1}{2\pi R_f C_1}$

Let $C_1 = 0.1\mu F$

then $R_f = 15.9\,K\Omega$

Now choose $f_b = 10 f_a = 1KHz$

$$\frac{1}{2\pi R_1 C_1} = 10\,KHz \Rightarrow R_1 = 1.59\,K\Omega$$

Since $R_f C_f = R_1 C_1 \Rightarrow C_f = \frac{R_f}{R_1 C_1} = 0.01\mu F$

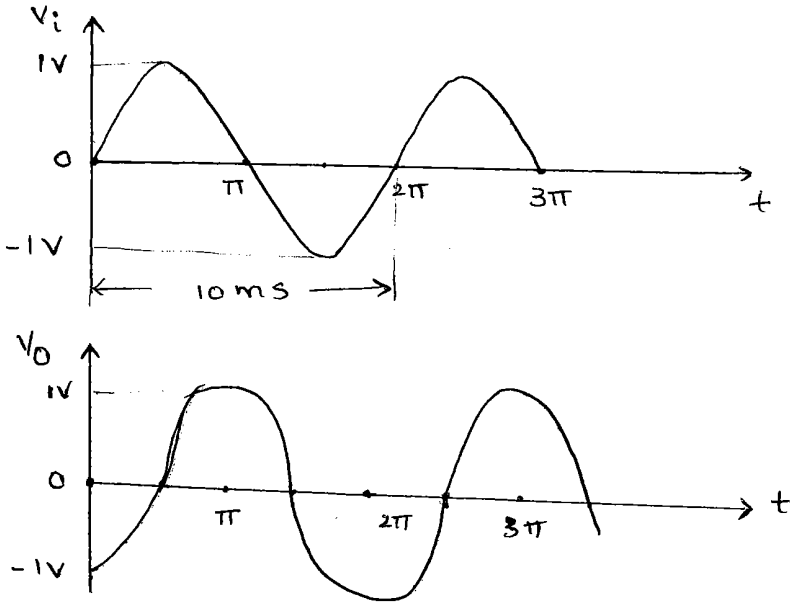
b) $V_i = 1 \sin \omega t$

$V_i = 1 \sin 2\pi f t = 1 \sin (2\pi \times 10^2) t$

$$V_o = -R_f C_1 \frac{dV_i}{dt} = -(15.9\,k\Omega)(0.1\,\mu F)\frac{d}{dt}(1V \sin 2\pi 10^2 t)$$

$$V_o = -1 \cos\left[2\pi(10^2)t\right]$$

The input and output waveforms are shown in figure below



Integrator:

If we interchange the resistor and capacitor of the differentiator, the circuit becomes an integrator

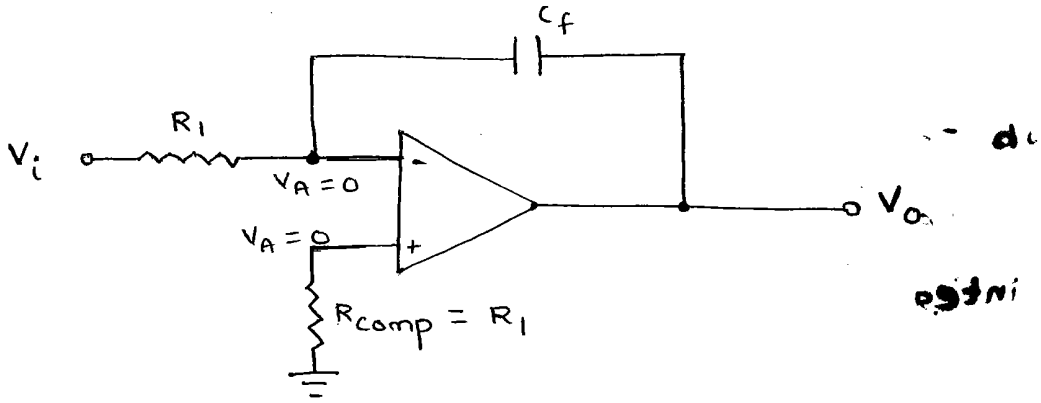


Fig: op-Amp Integrator

$$\frac{V_i - V_A}{R_1} = C_f \frac{d}{dt}(V_A - V_o)$$

$$\frac{V_i}{R_1} = -C_f \frac{dV_o}{dt} \Rightarrow \frac{dV_o}{dt} = -\frac{1}{R_1 C_f} V_i$$

$$\int_0^t dV_o = -\frac{1}{R_1 C_f} \int_0^t V_i \, dt$$

$$V_o(t) - V_o(0) = -\frac{1}{R_1 C_f} \int_0^t V_i(t) \, dt$$

$$V_o(t) = -\frac{1}{R_1 C_f} \int_0^t V_i(t) \, dt + V_o(0)$$

$V_o(0)$ = Initial output voltage

$$V_o(s) = -\frac{1}{sR_1 C_f} V_i(s)$$

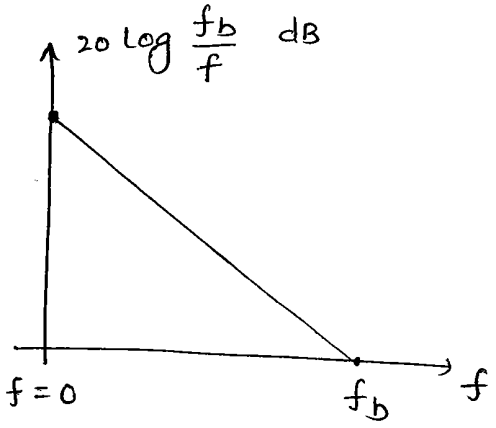
$$\Rightarrow \frac{V_o(s)}{V_i(s)} = \frac{-1}{sR_1 C_f} \Rightarrow A = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-1}{j\omega R_1 C_f}$$

$$A = \frac{j}{2\pi f R_1 C_f} = j\frac{f_b}{f} \quad \text{where } f_b = \frac{1}{2\pi R_1 C_f}$$

At $f \neq 0 \Rightarrow 20 \log |A| = \frac{f_b}{f}$

At $f = 0 \Rightarrow 20 \log \frac{f_b}{f} = \infty$

At $f = f_b \Rightarrow 20 \log \frac{f_b}{f} = 0$



At $f = 0$, the magnitude of the integrator transfer function is infinite.

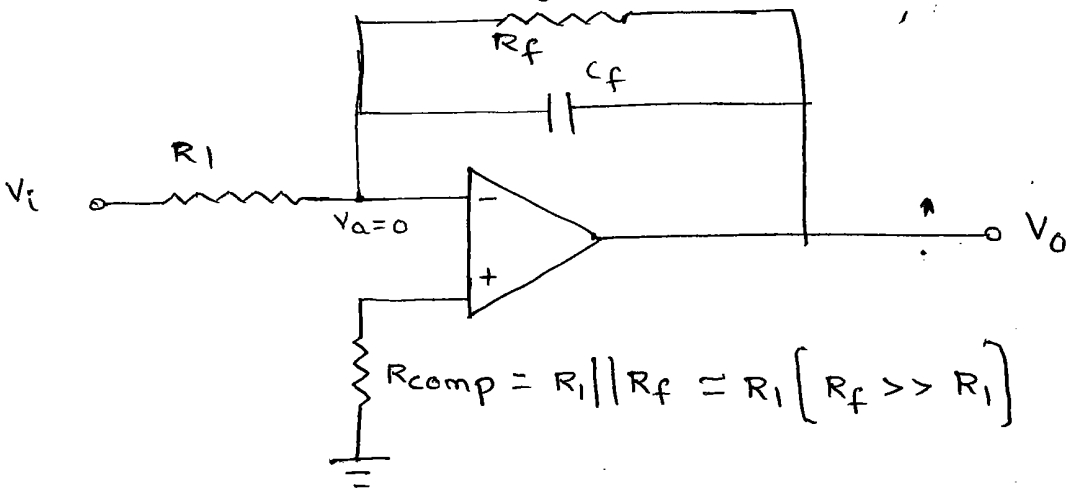
At dc ($f = 0$) the capacitor C_f behaves as an open circuit and there is no negative feedback. The op-Amp thus operates in open loop, resulting in an infinite gain. In practice, output never becomes infinite, rather the output of the amplifier saturates at a voltage close to $+V_{CC}$ or $-V_{EE}$.

As the gain of the integrator decreases with increasing frequency, the integrator circuit doesn't have any frequency problem as faced in a differentiator. However, at low frequencies such as at dc ($\omega = 0$) the gain becomes infinite (or saturates). The solution to this problem is solved by practical integrator ckt.

practical Integrator circuit [Lossy Integrator]:

The gain of an integrator at low frequency can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance R_f as shown in figure below.

the parallel combination of R_f and C_f behaves like a parallel capacitor which dissipates power unlike an ideal capacitor. For this reason, this circuit is also called a lossy integrator.



Here $$\frac{V_i - V_a}{R_1} = C_f \frac{d}{dt}(V_a - V_o) + \frac{V_a - V_o}{R_f}$$

$$\frac{V_i}{R_1} = -C_f \frac{dV_o}{dt} - \frac{V_o}{R_f}$$

Taking laplace transform on both sides

$$\frac{V_i(s)}{R_1} + s C_f V_o(s) + \frac{V_o(s)}{R_f} = 0$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-\frac{R_f}{R_1}}{1 + s R_f C_f}$$

$$A = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-R_f/R_1}{1 + j\omega R_f C_f}$$

$$A = \frac{-R_f/R_1}{1 + j\, 2\pi f R_f C_f} = \frac{-R_f/R_1}{1 + j\frac{f}{f_a}} \quad \text{where} \quad f_a = \frac{1}{2\pi R_f C_f}$$

$$|A| = \frac{R_f/R_1}{\sqrt{1 + \left(\frac{f}{f_a}\right)^2}}$$

At $f = 0 \Rightarrow 20 \log|A| = \frac{R_f}{R_1}$

At $f = f_a \Rightarrow 20 \log|A| = \frac{R_f/R_1}{\sqrt{2}} = 0.707 \frac{R_f}{R_1}$

$$= \frac{R_f}{R_1} - 3\,dB.$$

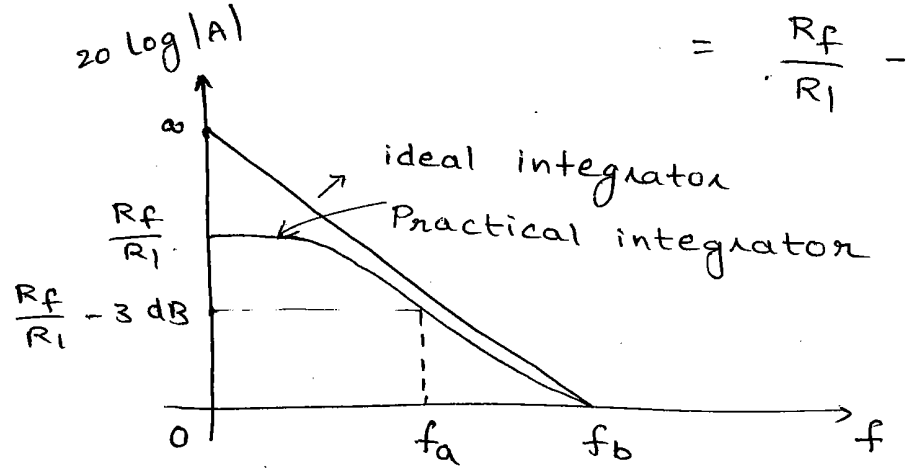


fig: Frequency Response

Applications of practical Integrator:

a) In Analog computers b) In solving differential eq's

c) In ADc's d) Ramp Generators

Problem: Find R_1 and R_f in the lossy integrator so that the peak gain is 20 dB and the gain is 3dB down from its peak when $\omega = 10000$ rad/s. use a capacitance of $0.01\mu F$.

solution: the gain of lossy integrator is

$$A(dB) = 20 \log_{10} \frac{R_f / R_1}{\sqrt{1 + (\omega R_f C_f)^2}}$$

the gain is max, when $\omega = 0$

$$A(dB) = 20 \log \frac{R_f}{R_1} = 20 \text{ dB}$$

$$\Rightarrow \frac{R_f}{R_1} = 10 \Rightarrow R_1 = \frac{R_f}{10}.$$

At $\omega = 10{,}000$ rad/s, gain is 3dB down from its peak of 20 dB, so gain becomes 17 dB. so

$$20 \log \frac{10}{\sqrt{1 + (10^4 \times R_f \times 0.01)^2}} = 17 \text{ dB}.$$

$$\Rightarrow R_f = 10 K\Omega \quad \text{then} \quad R_1 = 1 K\Omega.$$

Non Linear Applications Of OP-AMP

Sample and Hold circuit :

A sample and circuit samples an input signal and holds on to its last sampled value until the input is sampled again.

This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation systems.

One of the simplest practical sample and hold circuit configuration is shown in figure below.

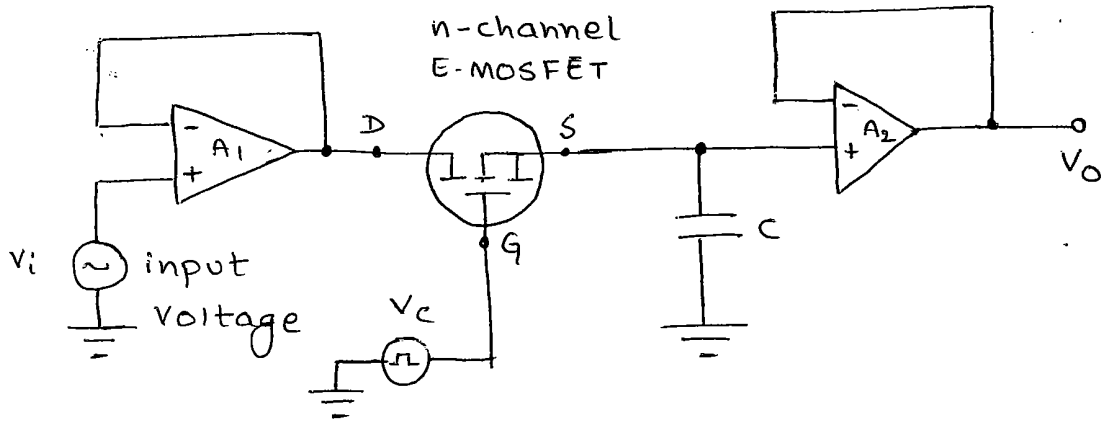


Fig (a) : Sample and Hold Circuit.

The n-channel E-MOSFET works as a switch and is controlled by the control voltage V_c and the capacitor 'C' stores the charge. The analog signal V_i to be sampled is applied to the drain of E-MOSFET and the control voltage V_c is applied to its gate.

when V_c is positive, the E-MOSFET turns on and the capacitor c charges to the instantaneous value of input V_i with a time constant $[R_o + r_{ds(on)}]$

Here R_o is the output resistance of the voltage follower A_1 and $r_{ds(on)}$ is the resistance of the MOSFET when on. Thus the input voltage V_i appears across the capacitor 'C' and then at the output thro-ugh the voltage follower A_2. The waveforms are as shown in figure below.

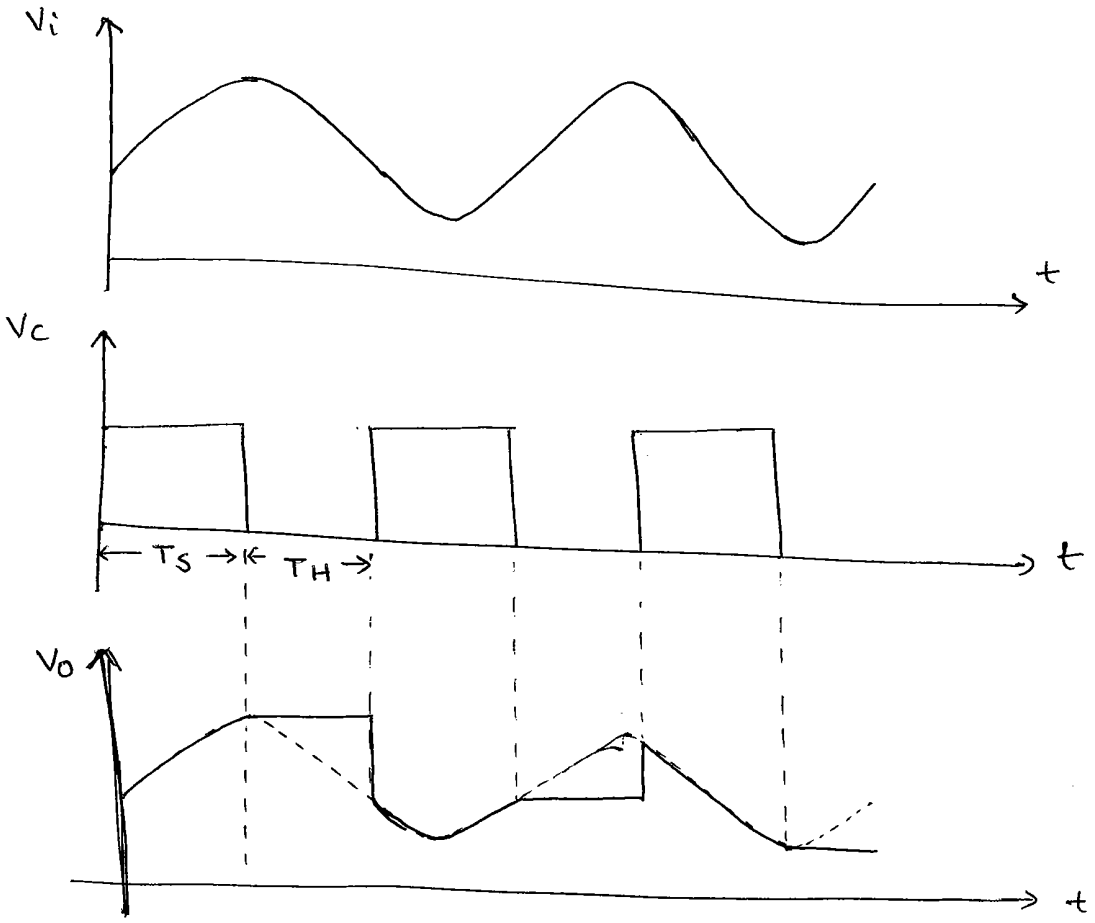
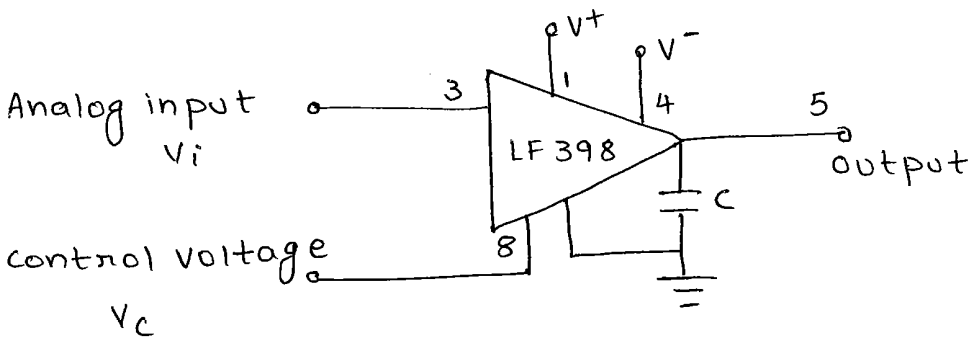


Fig b : Input and output waveforms

During the time when control voltage V_c is zero, the E-MOSFET is off. The capacitor C is now facing the high input impedance of the voltage follower A_2 and hence cannot discharge. The capacitor holds the voltage across it

The time period T_s, the time during which the voltage across the capacitor is equal to input voltage

is called sample period. The time period T_H of V_C during which the voltage across the capacitor is held constant is called hold period. The frequency of the control voltage should be kept higher than (atleast twice) the input so as to retrieve the input from output waveform. A typical connection diagram of the LF398 is shown below.



Log Amplifier:

Anti log computation may require functions such as $\ln x$, $\log x$ or $\sinh x$. These can be performed continu-ously with log Amps. log-Amp can also be used to compress the dynamic range of a signal.

The fundamental log-Amp circuit is shown in figure below where a grounded base transistor is placed in the feedback path.

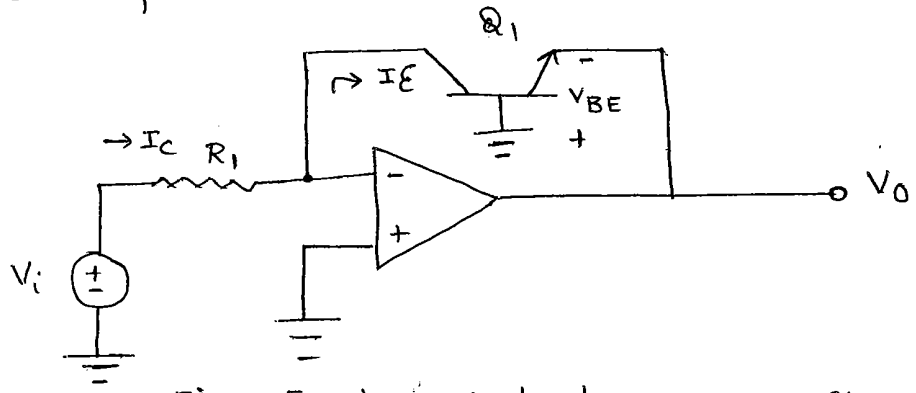


Fig: Fundamental Log-amp Circuit.

Here $I_E = I_S \left[e^{V_{BE}/\eta V_T} - 1 \right]$

where I_S = Reverse saturation current = 10^{-13} A

$\eta = 1$, & $V_T = \frac{KT}{q}$

K = Boltzman constant

T = absolute temp in ^0K

$$I_E = I_S \left[e^{qV_{BE}/KT} - 1 \right]$$

Here $I_E = I_C$

$$\frac{I_C}{I_S} + 1 = e^{qV_{BE}/KT}$$

$$\frac{I_C}{I_S} = e^{qV_{BE}/KT} \qquad \left[\frac{I_C}{I_S} >> 1 \right]$$

$$\ln \frac{I_C}{I_S} = \frac{qV_{BE}}{KT}$$

$$V_{BE} = \frac{KT}{q} \ln \frac{I_C}{I_S}$$

From the circuit $V_O = -V_{BE}$

$$V_O = -\frac{KT}{q} \ln \frac{I_C}{I_S}$$

$$\boxed{V_O = -\frac{KT}{q} \ln \frac{V_i}{R_1 I_S}} \qquad \left[\because I_C = \frac{V_i}{R_1} \right]$$

The output voltage is thus proportional to the logarithm of input voltage. Then by proper scaling

$$\log_{10} X = 0.4343 \ln X$$

The above log Amplifier circuit has one problem. the emitter saturation current I_s varies from transistor to transistor and with temperature. This is eliminated by the circuit shown in figure below.

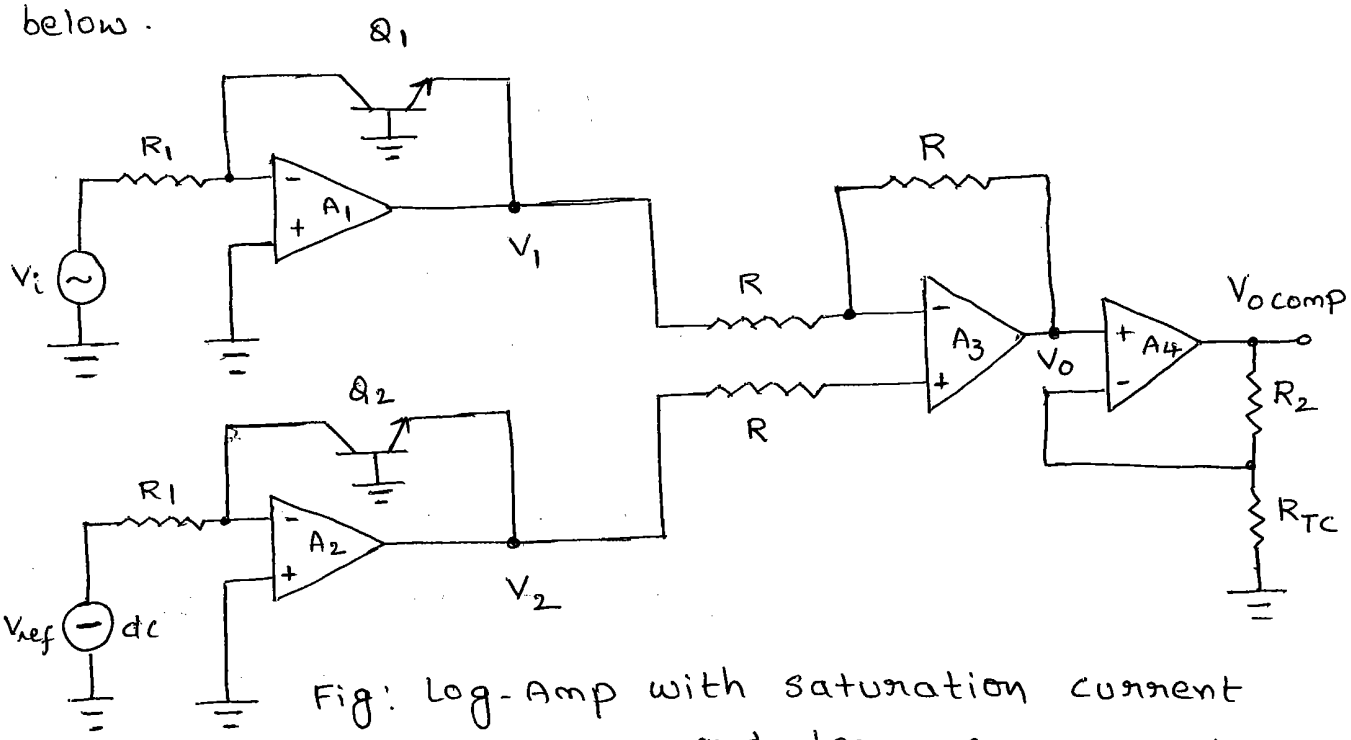


Fig: Log-Amp with saturation current and temp compensation

Let $I_{S_1} = I_{S_2} = I_S$

Here $$V_1 = \frac{-KT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$$

$$V_2 = \frac{-KT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

$$V_o = V_2 - V_1 = \frac{KT}{q} \ln \frac{V_i}{V_{ref}}$$

Thus reference level is now set with a single external voltage source. It dependence on device and temperature has been removed. The voltage V_o is still dependent upon temperature

and is directly proportional to T. This is compensated by the last op-Amp stage A_4 which provides a non inverting gain $\left(1 + \frac{R_2}{R_{TC}}\right)$. Now the output voltage is

$$V_{ocomp} = \left(1 + \frac{R_2}{R_{TC}}\right)\left(\frac{KT}{q}\right) \ln\left(\frac{V_i}{V_{ref}}\right)$$

where R_{TC} is a temp sensitive resistance with a positive co-efficient of temperature so that the slope of the equation becomes constant as the temperature changes.

the circuit of above figure requires four op-Amps. the same output (with an inversion) can be obtained by the circuit shown below which uses two op-Amps only.

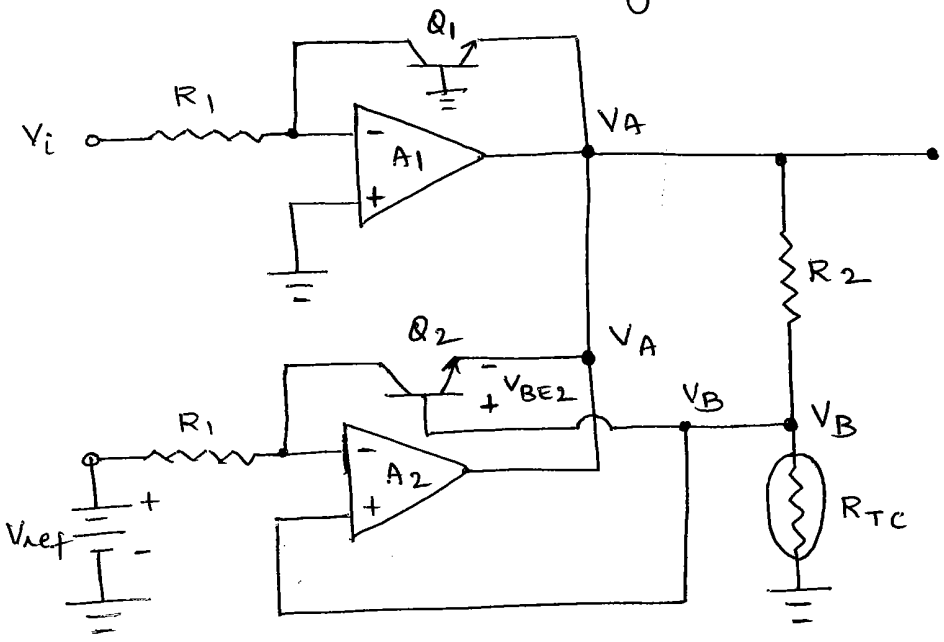


Fig: Log Amplifier using two op-Amps

Here $V_A = \frac{-KT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$

$$V_{BE2} = \frac{KT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

and $V_A = -V_{BE2} + V_B$

$$V_B = V_A + V_{BE2}$$

$$V_B = \frac{-KT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right) + \frac{KT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

$$V_B = -\frac{KT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

and $$V_B = V_o \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

$$\Rightarrow V_o = \left(\frac{R_2 + R_{TC}}{R_{TC}}\right) V_B$$

$$V_o = \left(1 + \frac{R_2}{R_{TC}}\right) \frac{-KT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

$$V_o = -\left(1 + \frac{R_2}{R_{TC}}\right) \frac{KT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

Anti log Amplifier:

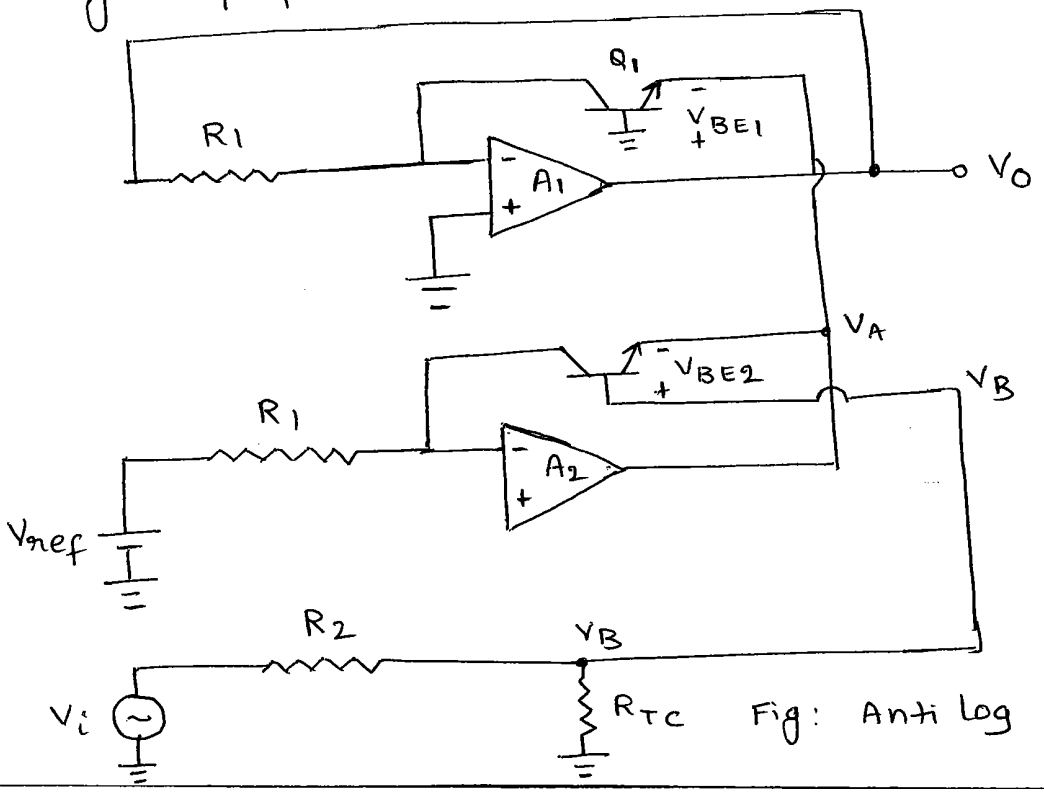


Fig: Anti log Amplifier

Here $V_A = \frac{-KT}{q} \ln\left[\frac{V_o}{R_1 I_S}\right]$ $\longrightarrow$ (1)

$$V_{BE2} = \frac{KT}{q} \ln\left[\frac{V_{ref}}{R_1 I_S}\right] \longrightarrow (2)$$

$$V_B = V_i \frac{R_{TC}}{R_2 + R_{TC}} \longrightarrow (3)$$

and $V_A = -V_{BE2} + V_B$

$$V_B = V_A + V_{BE2} = \frac{-KT}{q} \ln\left[\frac{V_o}{V_{ref}}\right]$$

From Eq (3) $V_i \frac{R_{TC}}{R_2 + R_{TC}} = \frac{-KT}{q} \ln\left[\frac{V_o}{V_{ref}}\right]$

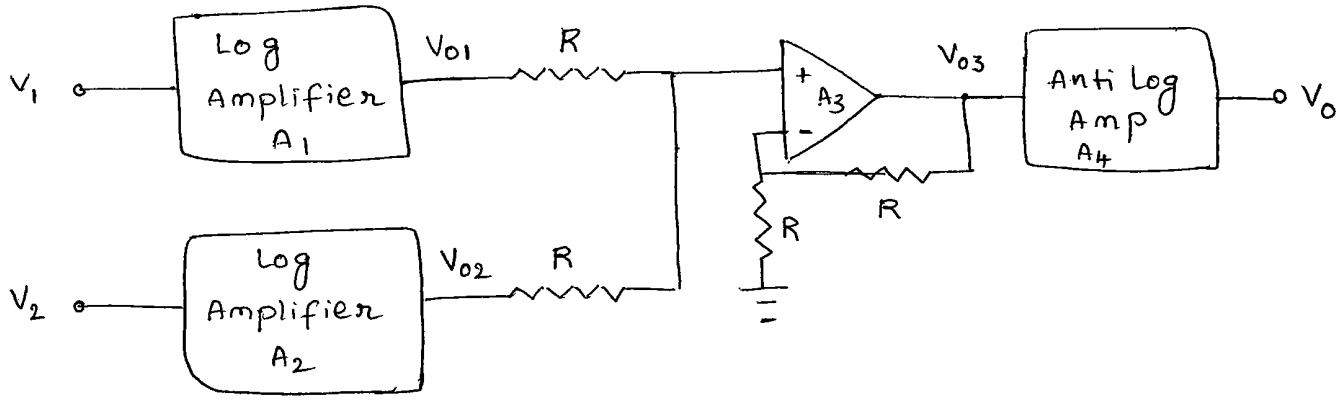
$$\ln\left(\frac{V_o}{V_{ref}}\right) = \frac{-q}{KT} \frac{R_{TC}}{R_2 + R_{TC}} V_i$$

$$\frac{V_o}{V_{ref}} = e^{\frac{-q}{KT}\left(\frac{1}{1 + \frac{R_2}{R_{TC}}}\right) V_i}$$

$$V_o = V_{ref}\, e^{-q/KT \left(\frac{1}{1 + \frac{R_2}{R_{TC}}}\right) V_i}$$

Multiplier and Divider Circuit :

Analog voltage multiplier Circuit :



The output of Log Amplifier

$$V_{o1} = -\frac{KT}{q}\left(1 + \frac{R_2}{R_{TC}}\right) \ln\left(\frac{V_1}{V_{ref}}\right)$$

$$V_{o2} = -\frac{KT}{q}\left(1 + \frac{R_2}{R_{TC}}\right) \ln\left[\frac{V_2}{V_{ref}}\right]$$

Since A_3 is a Non inverting Summing Amplifier

$$V_{o3} = V_{o1} + V_{o2}$$

$$V_{o3} = -\frac{KT}{q}\left(1 + \frac{R_2}{R_{TC}}\right) \ln \frac{V_1 V_2}{V_{ref}^2}$$

V_o is output of Antilog Amplifier

$$V_o = V_{ref}\ e^{-\frac{q}{KT}\frac{1}{\left(1 + \frac{R_2}{R_{TC}}\right)} V_{o3}}$$

$$V_o = V_{ref}\ e^{-\frac{q}{KT}\frac{1}{\left(1 + \frac{R_2}{R_{TC}}\right)} -\frac{KT}{q}\left(1 + \frac{R_2}{R_{TC}}\right) \ln \frac{V_1 V_2}{V_{ref}^2}}$$

$$V_o = V_{ref}\ \frac{V_1 V_2}{V_{ref}^2} \Rightarrow \boxed{V_o = \frac{V_1 V_2}{V_{ref}}}$$

$\therefore V_o \propto V_1 V_2$

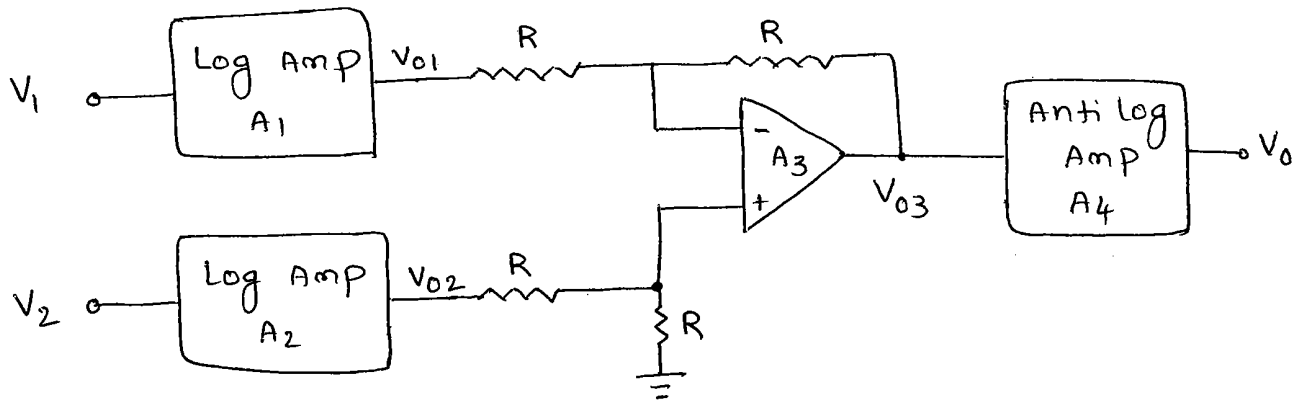


Fig: Analog Voltage Divider circuit

$$V_{o1} = \frac{-KT}{q}\left(1 + \frac{R_2}{R_{TC}}\right) \ln \frac{V_1}{V_{ref}}$$

$$V_{o2} = \frac{-KT}{q}\left(1 + \frac{R_2}{R_{TC}}\right) \ln \frac{V_2}{V_{ref}}$$

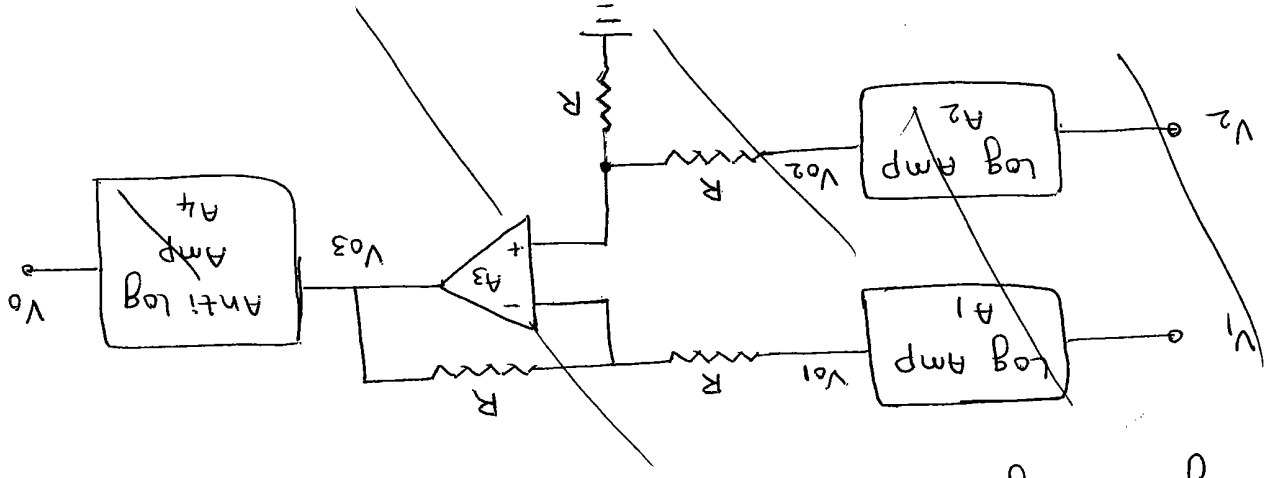
Since A_3 is Differential Amplifier

$$V_{o3} = V_{o2} - V_{o1}$$

$$V_{o3} = \frac{-KT}{q}\left(1 + \frac{R_2}{R_{TC}}\right) \ln \frac{V_2}{V_{ref}} + \frac{KT}{q}\left(1 + \frac{R_2}{R_{TC}}\right) \ln \frac{V_1}{V_{ref}}$$

$$V_{o3} = -\frac{KT}{q}\left(1 + \frac{R_2}{R_{TC}}\right) \ln \left(\frac{V_2}{V_1}\right)$$

Fig: Analog Voltage divider circuit



Analog Voltage Divider circuit :

V_o is output of Antilog Amplifier

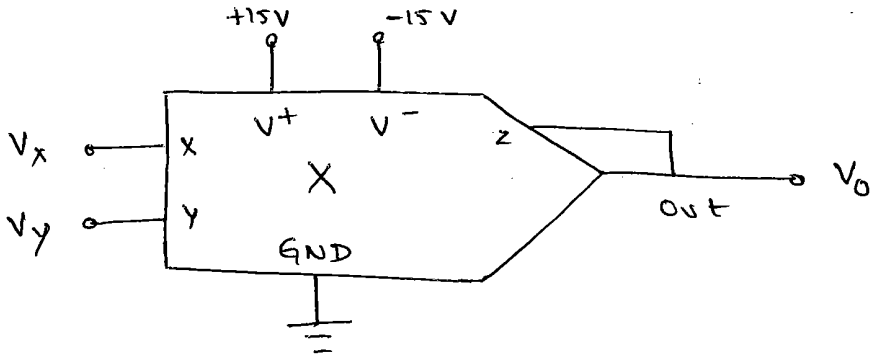
$$V_o = V_{ref} \cdot e^{\frac{-q}{KT} \frac{1}{\left(1+\frac{R_2}{R_{TC}}\right)} \frac{-KT}{q} \left(1+\frac{R_2}{R_{TC}}\right) \frac{V_2}{V_1}}$$

$$V_o = V_{ref} \left(\frac{V_2}{V_1}\right)$$

$$V_o \propto \frac{V_2}{V_1}.$$

Multiplier IC :

A basic multiplier schematic symbol is shown in figure below. Two signals (V_x and V_y) are provided. The output is the product of the two inputs divided by a reference voltage V_{ref}.



Here the output voltage is given by

$$V_o = \frac{V_x V_y}{V_{ref}}$$

As long as $V_x < V_{ref}$ and $V_y < V_{ref}$, the output of the multiplier will not saturate.

If both inputs are positive, the IC is said to be one quadrant multiplier.

A two quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative.

If both inputs may be either positive or negative, the IC is called a four quadrant multiplier.

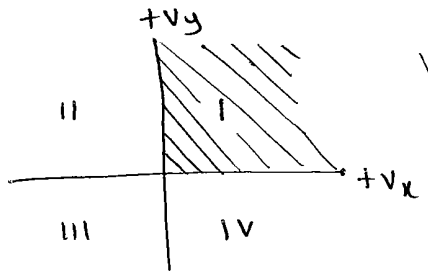
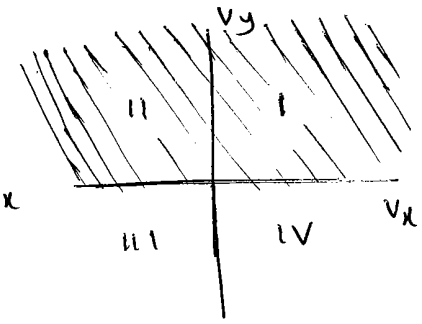
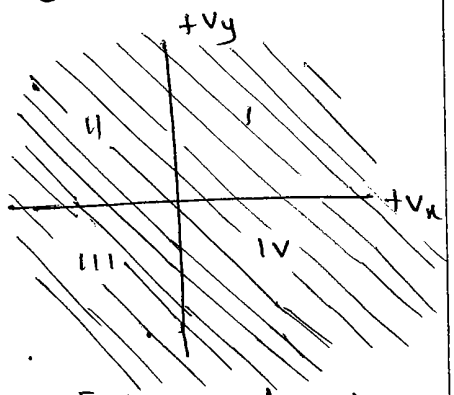


Fig: one quadrant Multiplier



Two quadrant Multiplier



Four quadrant Multiplier

Applications of Multipliers:

1) Frequency Doubling:

The multiplication of two sine waves of the same frequency, but of possibly different amplitudes and phase allows to double a frequency and to directly measure real power. Let

$$V_x = V_x \sin \omega t$$

$$V_y = V_y \sin(\omega t + \theta)$$

where θ is the phase difference between the two signals.

$$V_o = \frac{V_x V_y}{V_{ref}} = \frac{V_x \sin \omega t \; V_y \sin(\omega t + \theta)}{V_{ref}}$$

$$V_o = \frac{V_x V_y}{2 V_{ref}} \left[2 \sin \omega t \sin(\omega t + \theta) \right]$$

$$V_o = \frac{V_x V_y}{2 V_{ref}} \left[\cos \theta - \cos(2\omega t + \theta) \right]$$

$$V_o = \frac{V_x V_y}{2 V_{ref}} \cos\theta - \frac{V_x V_y}{2 V_{ref}} \cos(2\omega t + \theta)$$

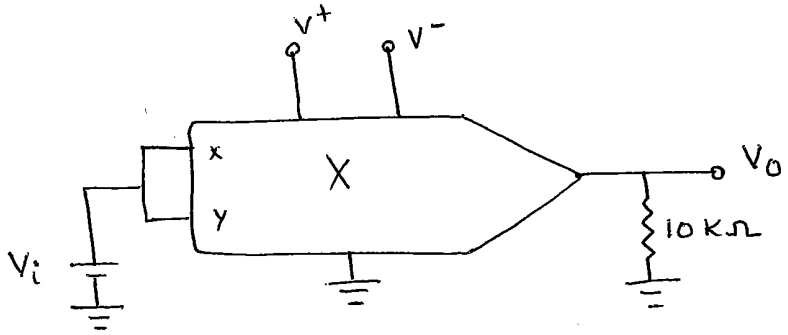
(dc term) (freq doubled)

The dc term can be easily removed by using a 1 μF coupling capacitor between load and the output terminal the circuit works as an ideal doubler if same frequency is applied to both the inputs

$$V_x = V_x \sin\omega t \qquad V_y = V_y \sin\omega t$$

$$V_o = \frac{V_x V_y}{V_{ref}} \sin^2\omega t = \frac{V_x V_y}{V_{ref}} \left[\frac{1 - \cos 2\omega t}{2}\right]$$

2) squarer circuit :



$$V_o = \frac{V_x V_y}{V_{ref}} = \frac{V_i^2}{V_{ref}}$$

3) phase Angle Detection :

$$V_x = V_x \sin\omega t \qquad V_y = V_y \sin(\omega t + \theta)$$

$$V_o = \frac{V_x V_y}{V_{ref}} \sin\omega t \sin(\omega t + \theta)$$

$$V_o = \frac{V_x V_y}{2 V_{ref}} \left[\cos\theta - \cos(2\omega t + \theta)\right]$$

The phase difference between the two input signals can be calculated from the dc component in the output voltage V_o that

$$V_{o,dc} = \frac{V_x V_y}{2 V_{ref}} \cos\theta .$$

Divider:

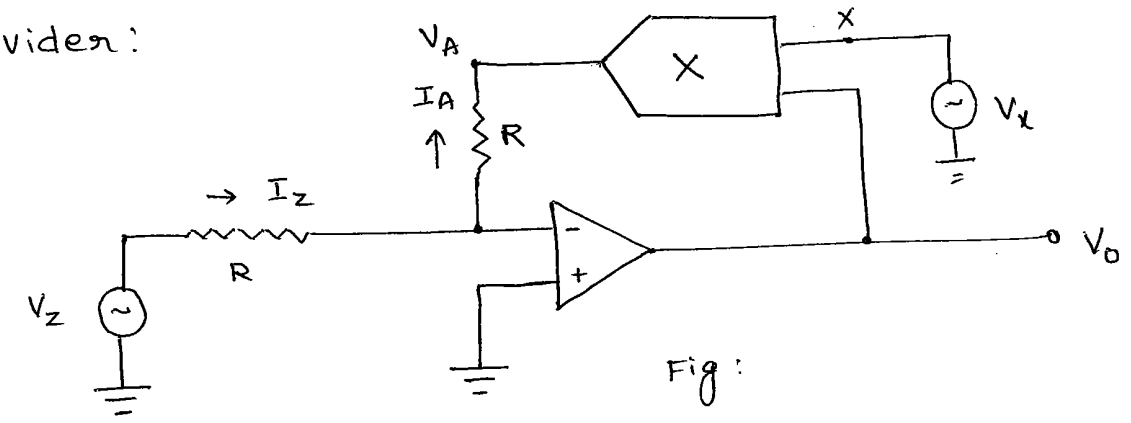


Fig:

Here $I_Z \neq$ Division, the complement of multiplication can be accomplished by placing the multiplier circuit element in the op-Amp's feedback loop.

$$I_Z = \frac{V_Z - 0}{R} = \frac{V_Z}{R} \longrightarrow (1)$$

$$I_A = \frac{0 - V_A}{R} = -\frac{V_A}{R} \longrightarrow (2)$$

$$I_Z = I_A \Rightarrow V_Z = -V_A \longrightarrow (3)$$

and $$V_A = \frac{V_x V_O}{V_{ref}} \longrightarrow (4)$$

$$\therefore (3) \Rightarrow V_Z = -\frac{V_x V_O}{V_{ref}} \Rightarrow V_O = -V_{ref}\left(\frac{V_Z}{V_x}\right)$$

$$\therefore V_O \propto \frac{V_Z}{V_x}$$

Application:

1) Finding Square Roots

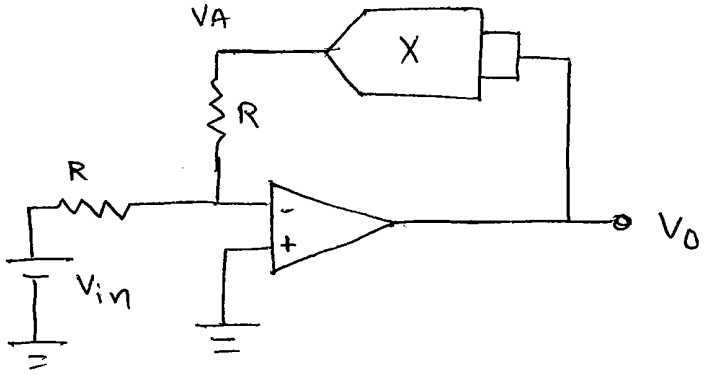
Here $$V_A = \frac{V_O^2}{V_{ref}}$$

$$V_O^2 = V_A V_{ref}$$

$$V_{in} = -V_A$$

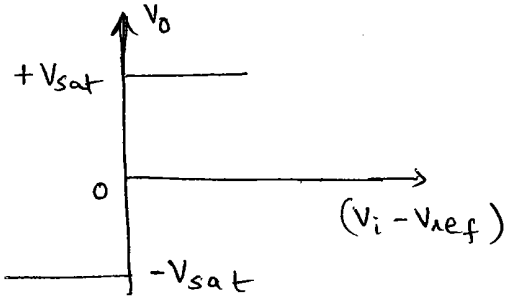
$$V_O^2 = -V_{in} V_{ref}$$

$$V_O = \sqrt{|V_{in}| V_{ref}}$$

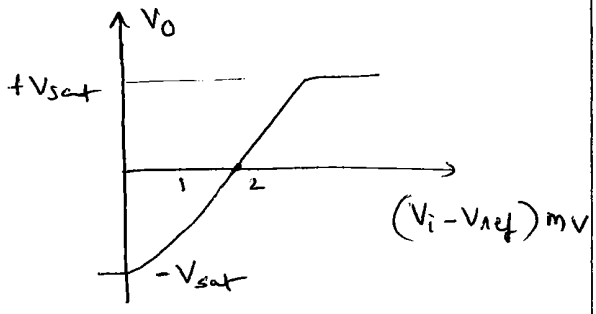


Comparator:

A comparator is a circuit which compares a signal voltage applied at one input of an op-Amp with a known reference voltage at the other input. It is basically an open-loop op-Amp with output ± Vsat (= Vcc) as shown in the ideal transfer characteristics.



a) Ideal Comparator transfer characteristics



b) practical Comparator transfer characteristics.

From the characteristics it may be seen that the change in the output state takes place with an increment in input V_i of only 2mV. This is the uncertainity region where output cannot be directly defined. this region is due to input off-set voltage and offset null compensating techniques can be used to eliminate this.

There are basically two types of Comparators.

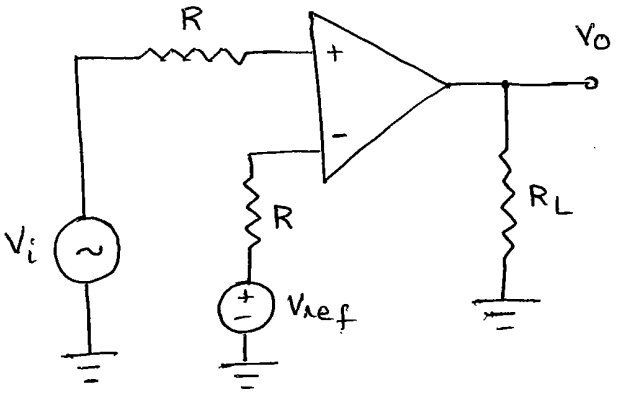
1. Non Inverting Comparator
2. Inverting Comparator.

1. Non Inverting Comparator:

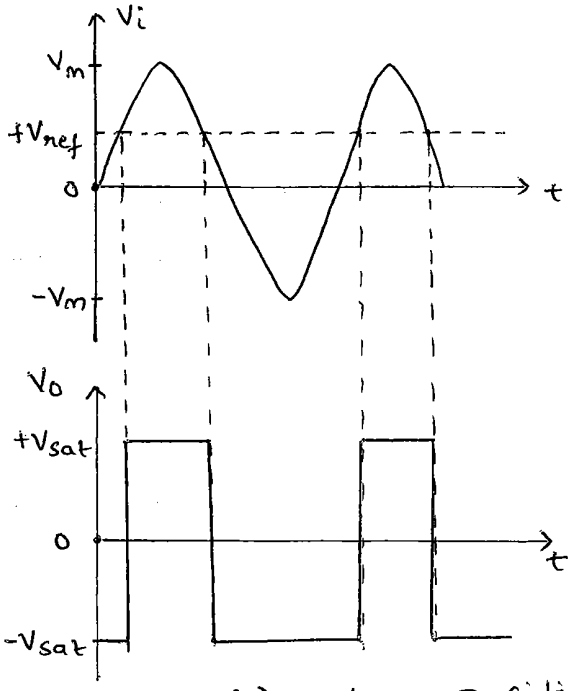
The circuit of Non-inverting Comparator is shown in figure below. A fixed reference voltage Vref is applied to (−) input and a time varying signal V_i is applied to (+) input.

$V_o = +V_{sat}$ if $V_i > V_{ref}$

$V_o = -V_{sat}$ if $V_i < V_{ref}$



Fig(a) Non Inverting Comparator



Fig(b) : V_{ref} positive

In a practical circuit V_{ref} is obtained by using a 10kΩ potentiometer which forms a voltage divider with the supply voltages V+ and V− with the wiper connected to the -ve terminal as shown in figure below.

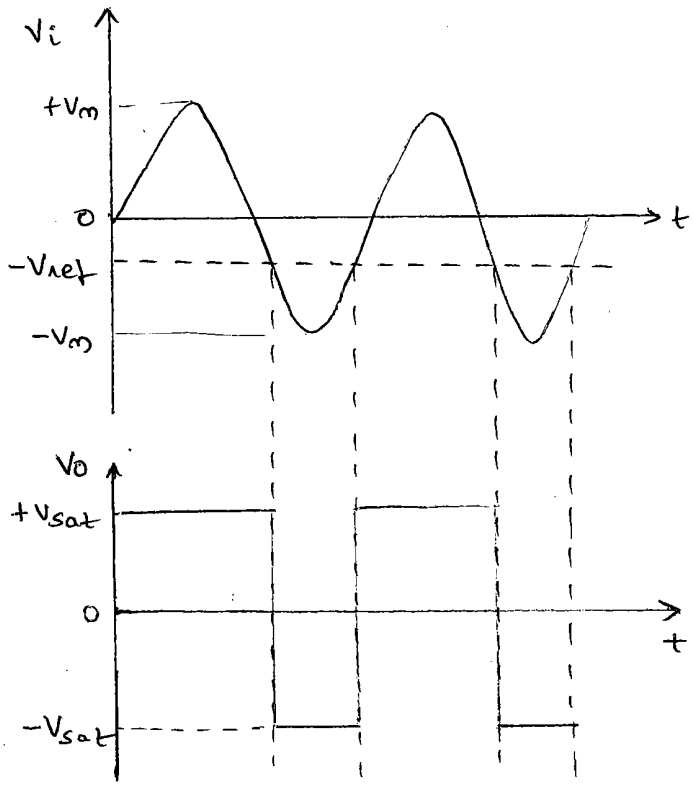
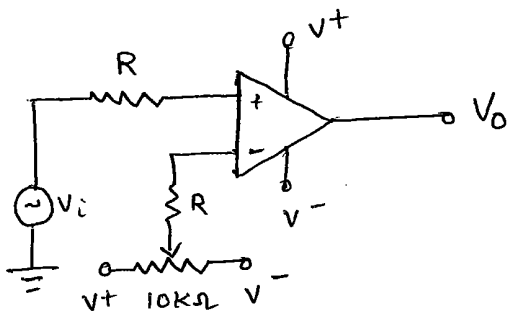


Fig (c) : V



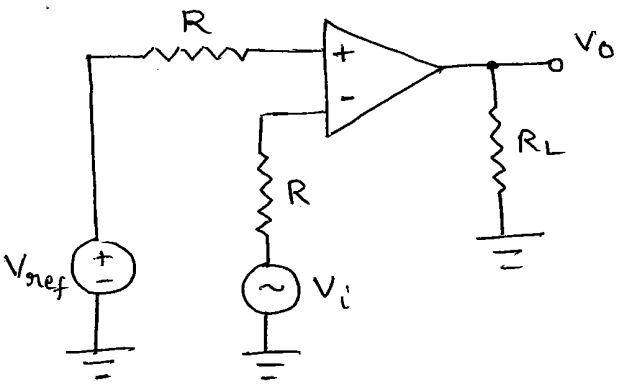
Thus a V_{ref} is obtained of desired amplitude and polarity can be obtained by simply adjusting the 10kΩ potentiometer.

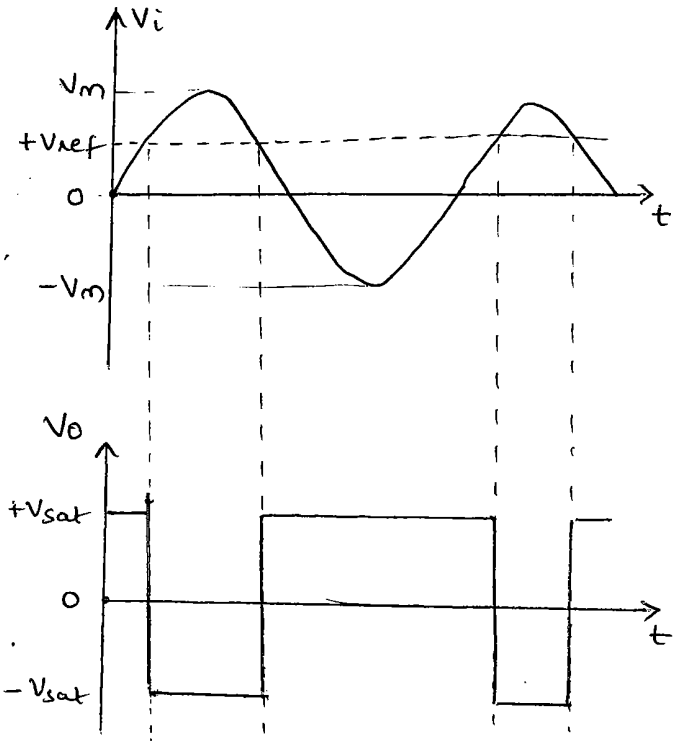
Inverting Comparator:

The circuit of inverting comparator is shown in figure below. A fixed reference voltage V_{ref} is applied to (+) input and a time varying signal V_i is applied to (-) input.

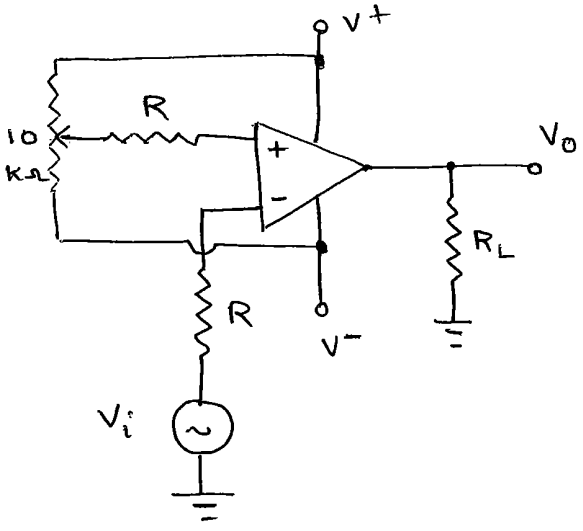
Here $V_o = +V_{sat}$ if $V_i < V_{ref}$

$V_o = -V_{sat}$ if $V_i > V_{ref}$





The practical inverting comparator circuit is shown in figure below.



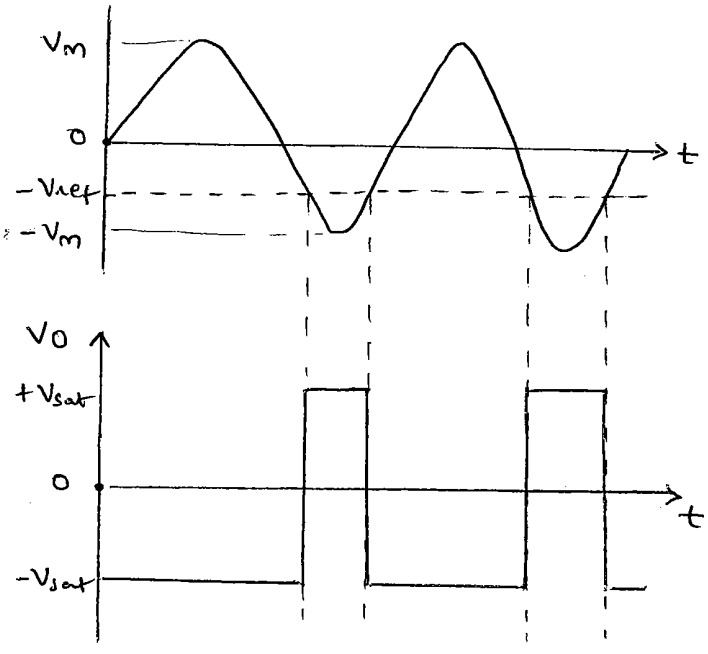


Fig: practical inverting comparator

Applications of Comparator:

Some important Applications of Comparator are

1. zero Crossing detector
2. Window Detector
3. Time marker Generator.

1. zero Crossing Detector:

An inverting zero Crossing detector is shown in figure below. The circuit is also called sine to square wave Generator.

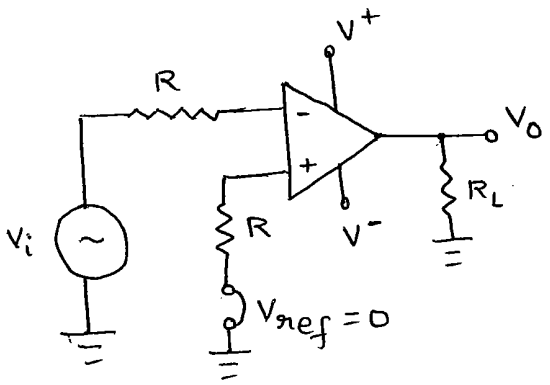


Fig: zero Crossing detector

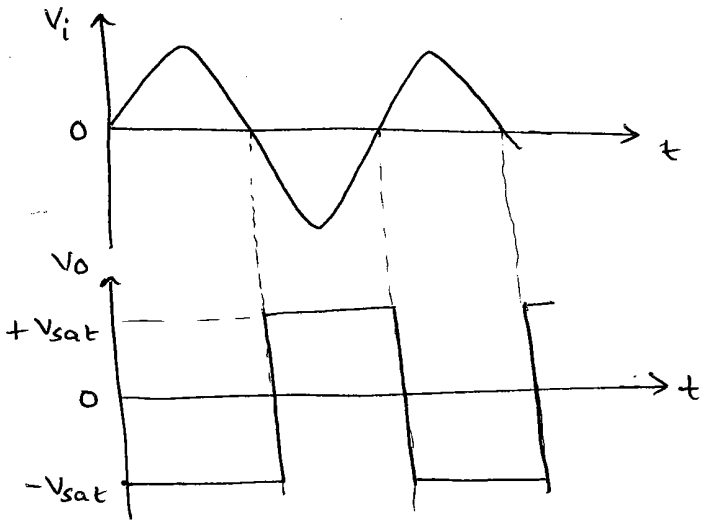


Fig: Input and output waveforms

2. Window Detector:

Sometimes it is required to mark the instant at which an unknown input is between two threshold levels This can be achieved by a circuit called window detector Figure below shows a three level detector with indicator circuit.

There are three indicators:

1. Yellow (LED 3) for input too low (< 3V)
2. Green (LED 2) for safe input (3 - 6V)
3. Red (LED 1) for high input (> 6V)

They are turned on and off as indicated in table below.

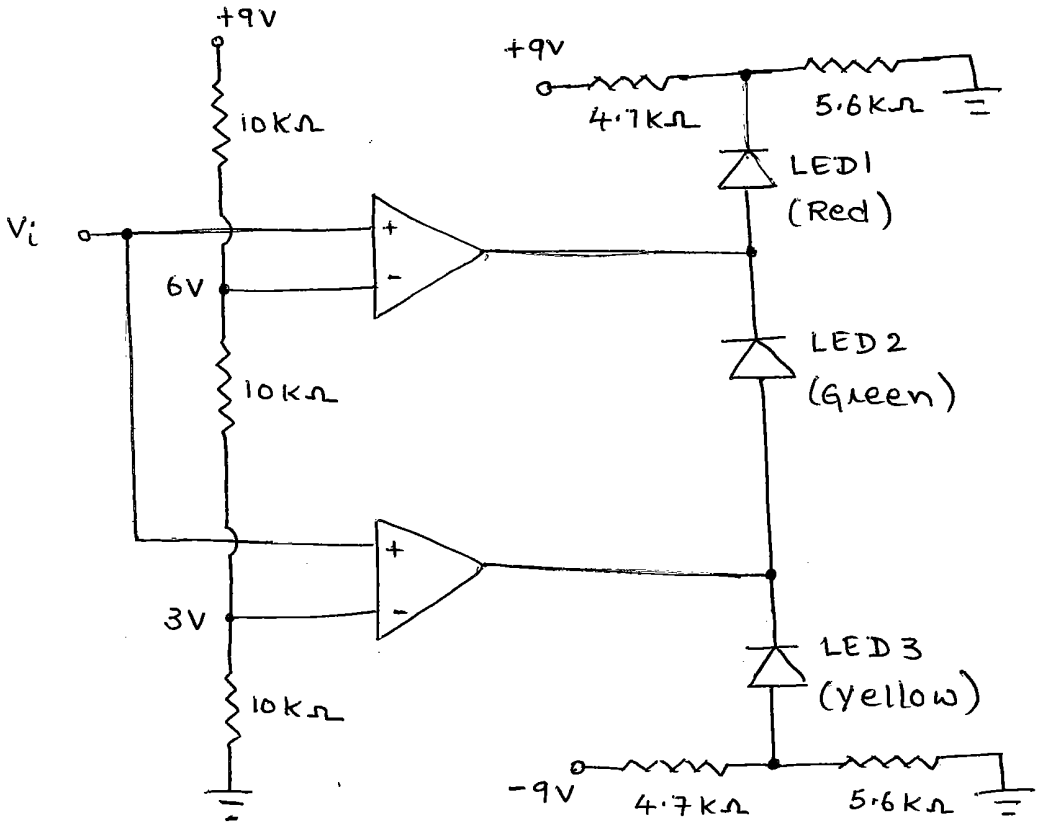


Fig: three level comparator with LED indicator.

Input	Yellow (LED 3)	Green (LED 2)	Red (LED 1)
$< 3V$	ON	OFF	OFF
$3 < V_i < 6V$	OFF	ON	OFF
$\geq 6V$	OFF	OFF	ON

3) Time Marker Generator.

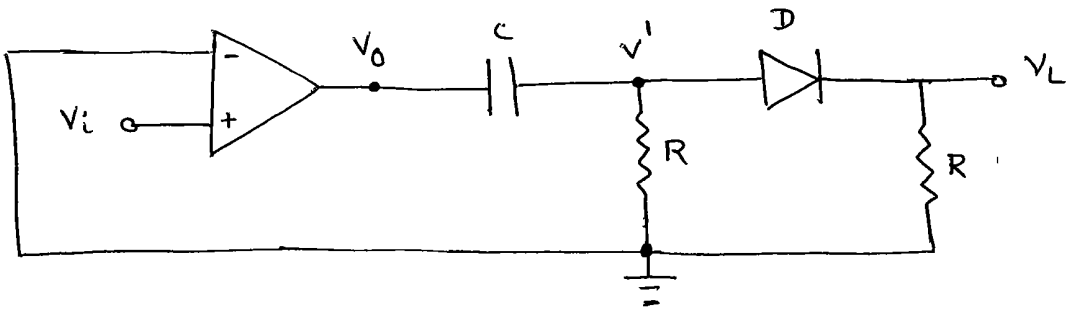
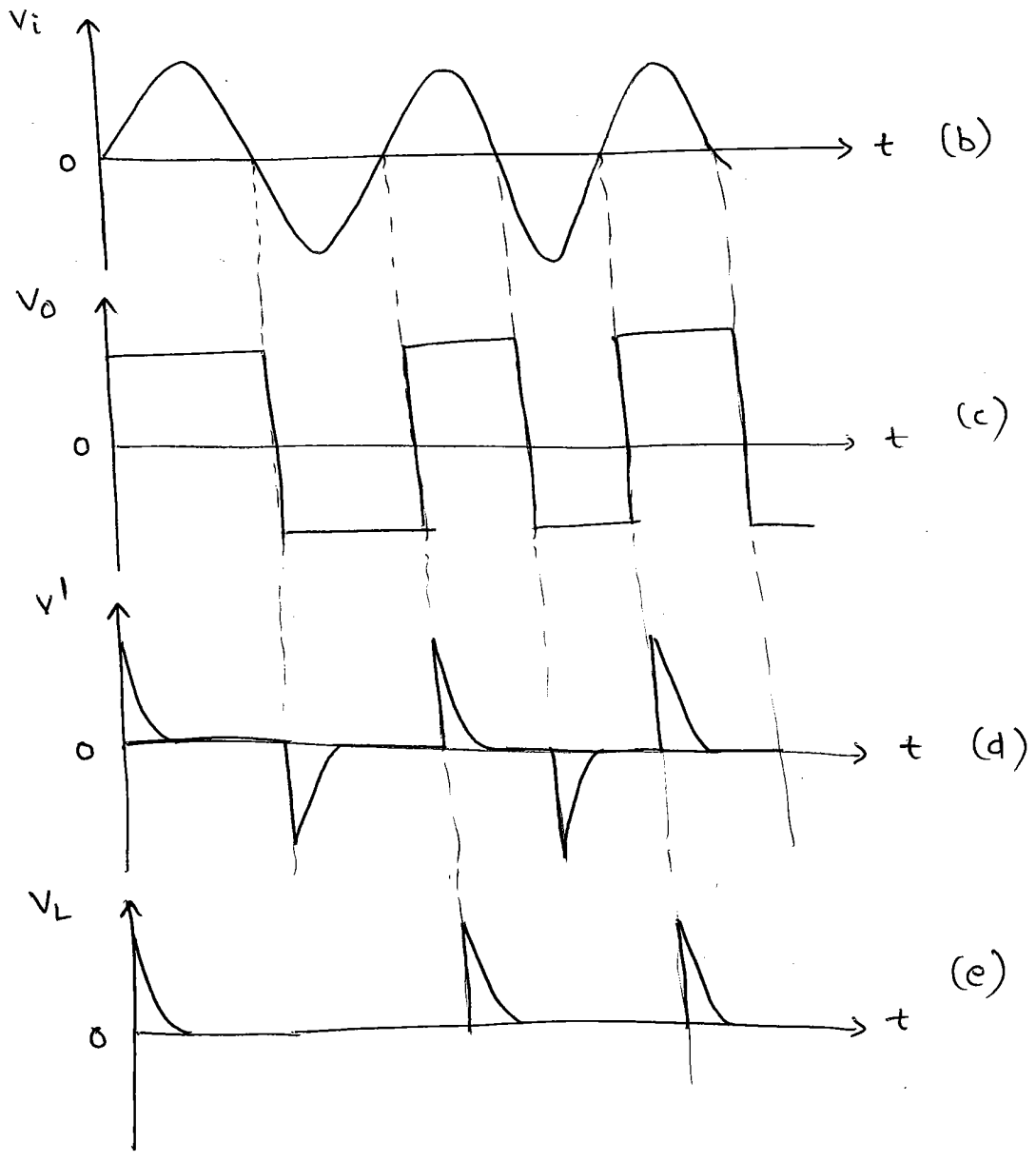


Fig a: Time Marker Circuit

The circuit is shown in figure above. The output of the zero crossing detector is differentiated by an

RC circuit ($RC \ll T$), so that the voltage v' is a series of positive and negative pulses as shown in figure below. The negative portion is clipped off after passing through the diode D and the waveform V_L is shown in figure below. So with the help of this circuit, the sinusoid has been converted in to a train of positive pulses of spacing T and may be used for triggering the monoshots, SCR, sweep voltage of CRT etc.



b) Input waveform (c) output V_o

(d) differentiated output v' (e) output pulses

Schmitt Trigger [Regenerative Comparator]:

In basic comparator circuit, a feedback is not used and the op-Amp is used in the open loop mode. As open loop gain is large, very small noise voltages also can cause triggering of the comparator, to change its state. such a false triggering may cause lot of problems in the applications of comparator as zero crossing detector. this may give a wrong indication of zero crossing due to zero crossing of noise voltage rather than zero crossing of input wanted signal. such unwanted noise causes the output to jump between high and low states. The comparator circuit used to avoid such unwanted triggering is called regenerative comparator or schmitt Trigger, which basically uses a positive feedback.

Figure below shows an inverting comparator with positive feedback. this circuit converts an irregular shaped wave form to a square wave or pulse. The circuit is known as the schmitt trigger or squaring circuit.

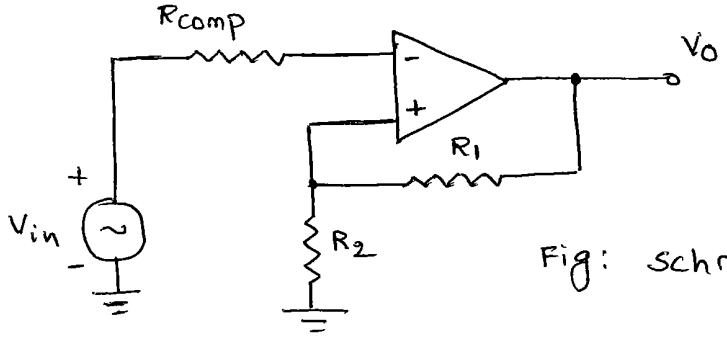
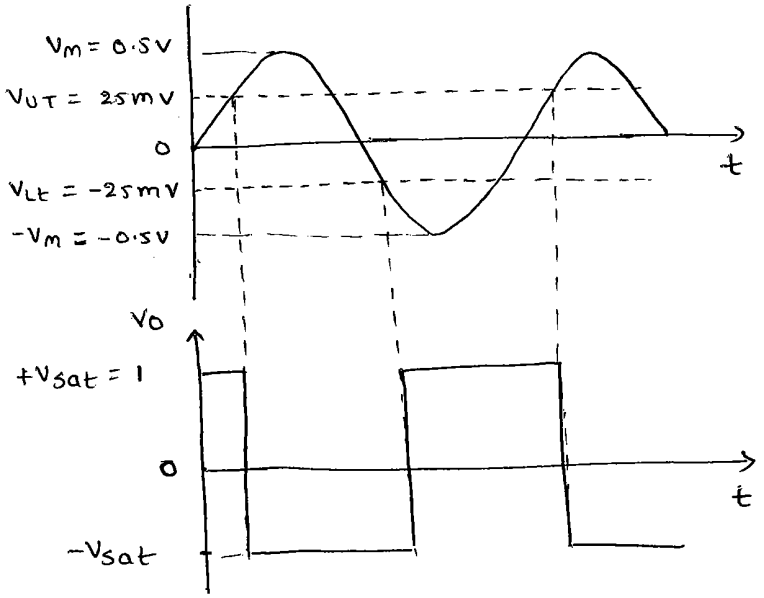


Fig: schmitt trigger

the input voltage V_{in} triggers (changes the state of) the output V_o every time it exceeds certain voltage levels called the upper threshold voltage V_{UT} and

lower threshold voltage V_{LT} as shown in fig below.



The threshold voltages are obtained by using the voltage divider $R_1 - R_2$, where the voltage across R_2 is fed back to the (+) input. The voltage across R_2 is a variable reference threshold voltage that depends on the value and polarity of output voltage V_o.

when $V_o = +V_{sat}$, the voltage across R_2 is called the upper threshold voltage, V_{ut}. the input voltage V_{in} must be slightly more positive than V_{ut} in order to cause the output V_o to switch from $+V_{sat}$ to $-V_{sat}$. As long as $V_{in} < V_{ut}$, V_o is at $+V_{sat}$. using the voltage divider rule

$$V_{ut} = \frac{R_2}{R_1 + R_2} (+V_{sat})$$

on the other hand, when $V_o = -V_{sat}$, the voltage across R_1 is referred to as lower threshold voltage V_{lt}. V_{in} must be slightly more negative than V_{lt} in order to cause V_o to switch from $-V_{sat}$ to $+V_{sat}$.

In other words, for V_{in} greater than V_{lt}, V_o is at $-V_{sat}$ V_{lt} is given by the following equation.

$$V_{lt} = \frac{R_2}{R_1 + R_2} (-V_{sat})$$

Thus, if the threshold voltages V_{ut} and V_{lt} are made larger than the input noise voltages, the positive feedback will eliminate the false output transitions. Also, the positive feedback, because of its regenerative action, will make V_o switch faster between $+V_{sat}$ and $-V_{sat}$ The Resistance $R_{comp} \simeq R_1 || R_2$ is used to minimize the offset problems.

The comparator with positive feedback is said to exhibit hysteresis, a dead band condition. That is, when the input of the comparator exceeds V_{ut}, its output switches from $+V_{sat}$ to $-V_{sat}$ and reverts back to its original state, $+V_{sat}$, when the input goes below V_{lt}. The hysteresis voltage is equal to the difference between V_{ut} and V_{lt}. therefore

$$V_H = V_{ut} - V_{lt} = \frac{R_2}{R_1 + R_2} \left[+V_{sat} - (-V_{sat}) \right]$$

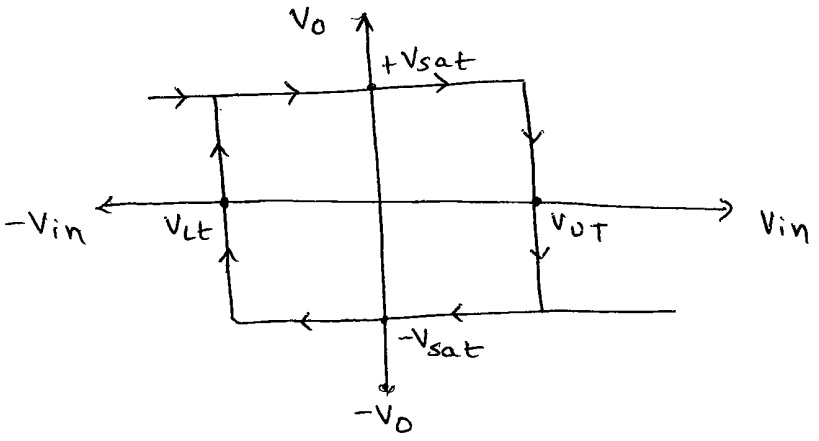
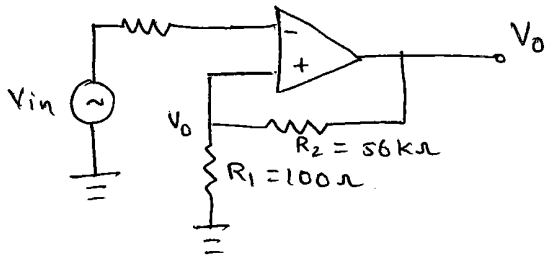


Fig: V_o Versus V_{in} plot of the hysteresis voltage

problem: In the circuit shown in figure $R_1 = 100\Omega$, $R_2 = 56K\Omega$, $V_{in} = 1 V_{pp}$ sine wave and the op-Amp is type 741 with supply voltages $= \pm 15V$. Determine the threshold voltages V_{UT} and V_{LT} and draw the output wave form.

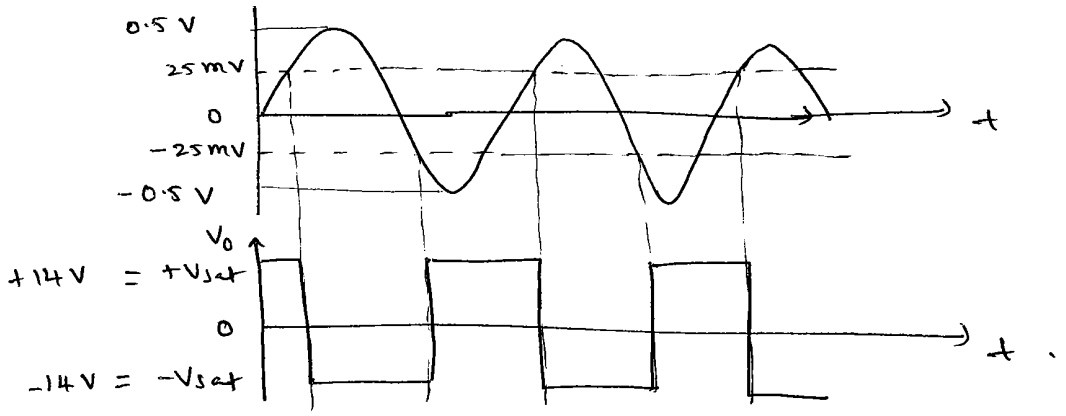


solution: For 741 the maximum output voltage swing is $\pm 14V$. that is $+V_{sat} = +14V$, $-V_{sat} = -14V$

$$V_{UT} = \frac{100}{56000 + 100} \times 14 = 25mV$$

$$V_{LT} = \frac{100}{56000 + 100} \times -14 = -25mV.$$

$$V_H = V_{UT} - V_{LT} = 25 - (-25) = 50mV.$$

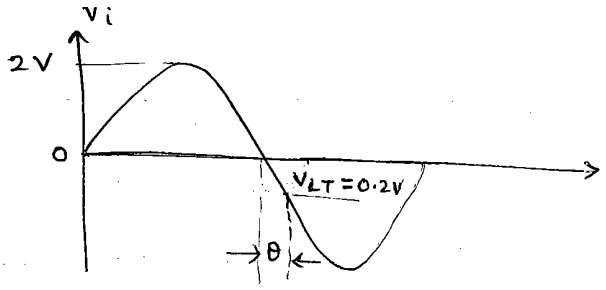


problem: A schmitt trigger with the upper threshold level $V_{UT} = 0V$ and hysteresis width $V_H = 0.2V$ converts a 1KHz sine wave of amplitude $4 V_{pp}$ in to a square wave calculate the time duration of the negative and positive portion of the output waveform.

Solution: $V_{UT} = 0V$

$V_H = 0.2V$, $V_H = V_{UT} - V_{LT}$

So $V_{Lt} = -0.2\,V$



the angle θ can be calculated as

$$-0.2 = V_m \sin(\pi + \theta)$$

$$-0.2 = V_m - \sin\theta$$

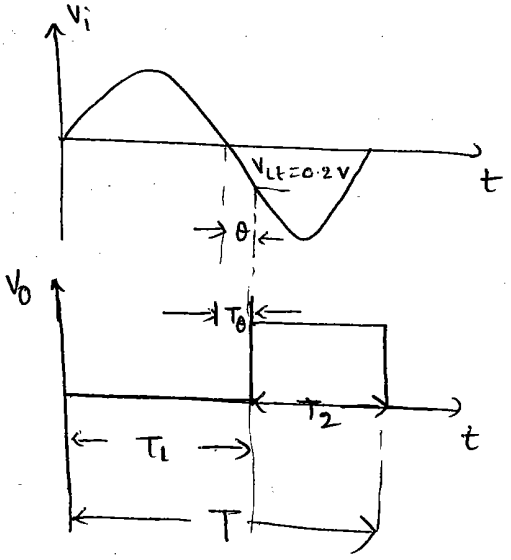
$$-0.2 = -2\sin\theta \Rightarrow \sin\theta = 0.1 \Rightarrow \theta = \sin^{-1}(0.1)$$

$$\theta = 0.1 \text{ radian}$$

$$T = \frac{1}{f} = \frac{1}{1000} = 1\,ms$$

$$\omega T_\theta = 2\pi(1000)\,T_\theta = 0.1$$

$$T_\theta = 0.016\,ms$$

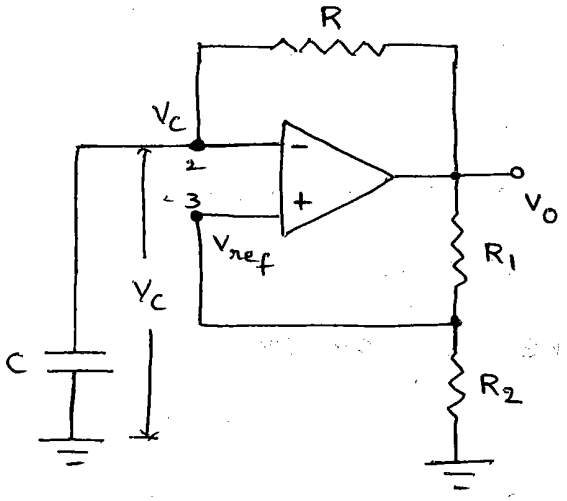


So $T_1 = \frac{T}{2} + T_\theta = 0.516\,ms$

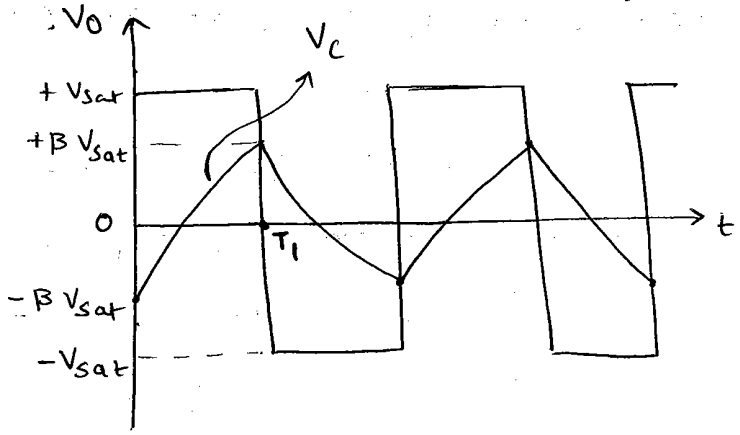
$T_2 = \frac{T}{2} - T_\theta = 0.484\,ms$

Multivibrators:

1. Astable multivibrator (square wave Generator):



Fig(a): Simple op-Amp square wave Generator



Fig(b): waveforms

A simple op-Amp square wave generator is shown in figure above. Also called a free running

oscillator, the principle of generation of square wave output is to force an op-Amp to operate in the saturation region. In fig(a) fraction $\beta = R_2/(R_1+R_2)$ of the output is fed back to the (+) input terminal. thus the reference voltage V_{ref} is βV_o and may take values as $+\beta V_{sat}$ or $-\beta V_{sat}$. The output is also fedback to the (-) input terminal after integrating by means of a lowpass RC combination. whenever input at the (-) input terminal just exceeds V_{ref}, switching takes place resulting in a square wave output. In astable multivibrator both the states are Quasi stable.

consider an instant of time when the output is at $+V_{sat}$. The capacitor now starts charging towards $+V_{sat}$ through resistance R as shown in fig(b). The voltage at the (+) input terminal is held at $+\beta V_{sat}$ by R_1 and R_2 combination. This condition continues as the charge on C rises, until it has just exceeded $+\beta V_{sat}$, the reference voltage.

when the voltage at the (-) input terminal becomes just greater than this reference voltage, the output is driven to $-V_{sat}$. At this instant the voltage on the capa-citor is $+\beta V_{sat}$. It begins to discharge through R, that is discharges towards $-V_{sat}$. when the capacitor voltage just exceeds $-\beta V_{sat}$ the output switches back to $+V_{sat}$. The cycle repeats itself as shown in fig(b).

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and

vice versa. The voltage across the capacitor as a function of time is given by

$$V_c(t) = V_{final} - (V_{final} - V_{initial})\, e^{-t/RC}$$

where the $V_{final} = +V_{sat}$, $V_{initial} = -\beta V_{sat}$

$$\therefore V_c(t) = +V_{sat} - (+V_{sat} + \beta V_{sat})\, e^{-t/RC}$$

At $t = T_1$, voltage across the capacitor reaches βV_{sat} and switching takes place. $V_c(T_1) = \beta V_{sat}$

$$\beta V_{sat} = +V_{sat} - V_{sat}(1+\beta)\, e^{-T_1/RC}$$

$$\therefore T_1 = RC \ln \frac{1+\beta}{1-\beta}$$

Total time period $T = 2T_1 = 2RC \ln\left[\frac{1+\beta}{1-\beta}\right]$

and the output waveform is symmetrical.

If $R_1 = R_2$, then $\beta = 0.5$ and $T = 2RC \ln 3$.

The output swings from $+V_{sat}$ to $-V_{sat}$ so $V_{O(P-P)} = 2V_{sat}$

Problem: For Astable multivibrator $R_1 = 86\,K\Omega$, $R_2 = 100\,K\Omega$, $R = 100\,K\Omega$, $C = 0.1\,\mu F$, $V_{sat} = \pm 15\,V$. Calculate i) Reference voltage (ii) Time period (iii) Frequency of Astable Multivibrator.

Solution: ① $V_{ref} = \frac{R_2}{R_1 + R_2} \times \pm V_{sat} = \frac{100\,K\Omega}{186\,K\Omega} \times \pm 15V$

$$\therefore V_{ref} = \pm 8.06\,V$$

② $T = 2RC \ln\left[\frac{1+\beta}{1-\beta}\right]$ Here $\beta = \frac{100}{186} = 0.537$

$$T = 2 \times 100\,K\Omega \times 0.1 \times \mu \times \ln\left[\frac{1+0.537}{1-0.537}\right] = 24\,ms$$

③ $f = \frac{1}{T} = 41.6\,KHz$.

(2) Monostable Multivibrator:

Monostable multivibrator has one stable state and the other is quasi stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-Amp. The circuit shown in figure is a modified form of the astable multivibrator.

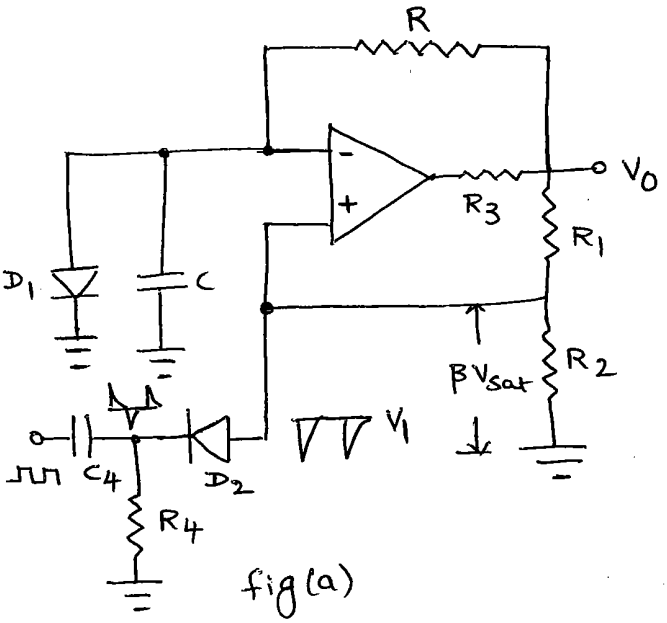
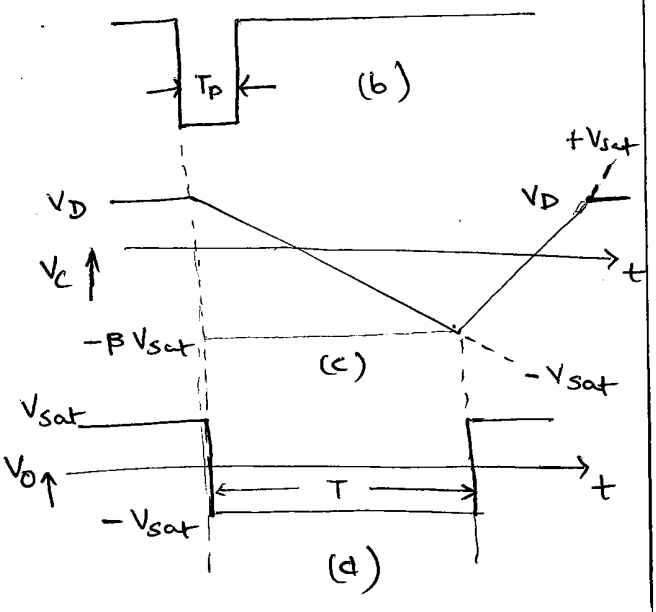


fig (a)



a) Mono stable multivibrator b) Negative going triggering signal (c) capacitor waveform (d) output voltage waveform

A diode D_1 clamps the capacitor voltage to 0.7 V when the output is at $+V_{sat}$. A Negative going pulse signal of Magnitude V_1 passing through the differentiator R_4C_4 and diode D_2 produces a negative ~~tri~~ going triggering impulse and is applied to the (+) input terminal.

Let us assume that in the stable state, the output V_o is at $+V_{sat}$. the diode D_1 conducts and V_C

the voltage across the capacitor C gets clamped to 0.7V. The voltage at the (+) input terminal through R_1R_2 potentiometric divider is $+\beta V_{sat}$.

Now if a negative trigger of magnitude V_1 is applied to the (+) input terminal so that the effective signal at this terminal is less than 0.7V ie $(\beta V_{sat} + (-V_1) < 0.7V)$, the output of the op-Amp will switch from $+V_{sat}$ to $-V_{sat}$. The diode will not get reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through the resistance R. The voltage at the (+) input terminal is now $-\beta V_{sat}$.

When the capacitor voltage V_c becomes just slightly more negative than $-\beta V_{sat}$, the output of the op-Amp switches back to $+V_{sat}$. The capacitor 'C' now starts charging to $+V_{sat}$ through R until V_c is 0.7V as capacitor C gets clamped to the voltage.

The pulse width T of monostable multivibrator is calculated as follows:

$$V_c = V_{final} - (V_{final} - V_{initial})\, e^{-t/RC}$$

$V_{final} = -V_{sat}$ and $V_{initial} = V_D$

$$V_c = -V_{sat} + (V_D + V_{sat})\, e^{-t/RC}$$

at $t = T$, $V_c = -\beta V_{sat}$

$$\therefore -\beta V_{sat} = -V_{sat} + (V_D + V_{sat})\, e^{-T/RC}$$

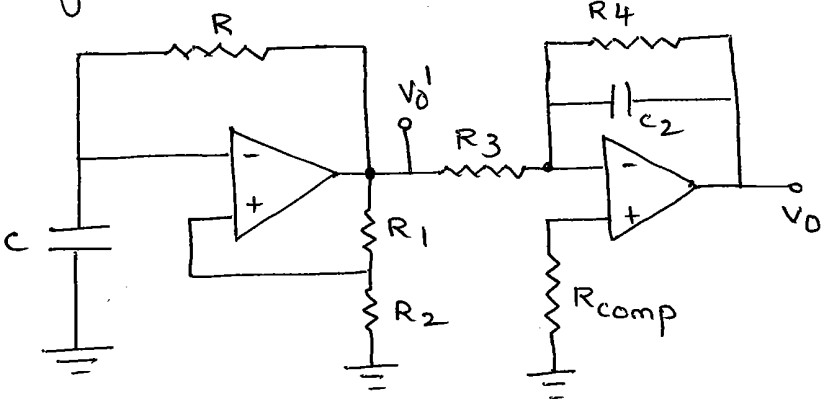
After simplification $T = RC \ln\left(\frac{1 + V_D/V_{sat}}{1 - \beta}\right)$

where $\beta = \frac{R_2}{R_1 + R_2}$

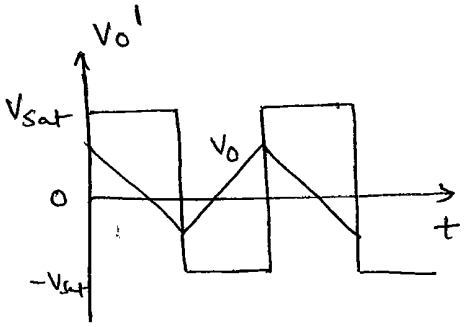
If $V_{sat} >> V_D$ and $R_1 = R_2$ so that $\beta = 0.5$ then

$$T = 0.69\,RC$$

Triangular wave Generator :



Fig(a): Triangular waveform Generator



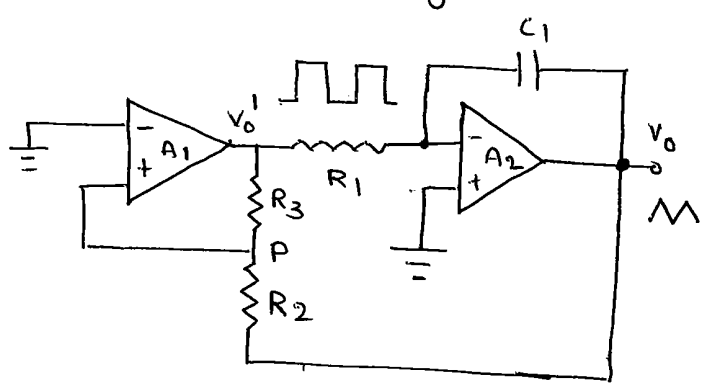
Fig(b) : output waveform.

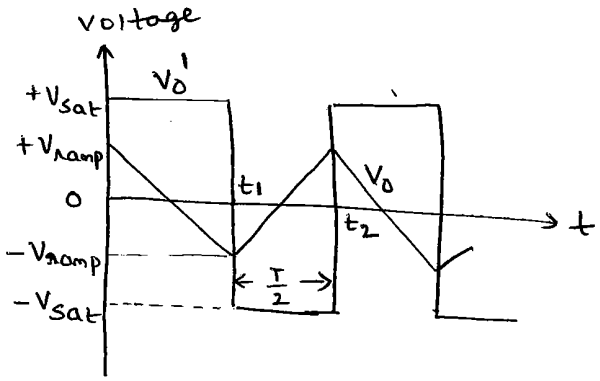
A triangular wave can be simply obtained by integrating a square wave as shown in fig(a). It is obvious that the frequency of the square wave and the triangular wave is the same as shown in figure(b).

Although the amplitude of the square wave is constant at $\pm V_{sat}$, the amplitude of the triangular wave will decrease as the frequency increases. this is because the reactance of the capacitor C_2 in the feedback CKT decreases at high frequencies. A resistance R_4 is connected across C_2 to avoid the saturation problem at low frequencies as in the case of practical integrator.

Another triangular wave generator using lesser number of components is shown in figure below. It basically consists of a two level comparator followed by an integrator. The output of the comparator A_1 is a square wave of

amplitude $\pm V_{sat}$ and is applied to the (−) input terminal of the integrator A_2 producing a triangular wave. This triangular wave is fed back as input to the comparator A_1 through a voltage divider R_2R_3.





Initially, let us consider that the output of comparator A_1 is at $+V_{sat}$. The output of the comparator Integrator A_2 will be a negative going ramp as shown in figure above. Thus one end of the voltage divider R_2R_3 is at a voltage $+V_{sat}$ and the other at the negative going ramp of A_2. At a time $t=t_1$, when the negative going ramp attains a value of $-V_{ramp}$, the effective voltage at point P becomes slightly less than 0V. This switches the output of A_1 from $+V_{sat}$ to $-V_{sat}$.

During the time when the output of A_1 is at $-V_{sat}$, the output of A_2 increases in the positive direction. And at the instant $t=t_2$, the voltage at point P becomes just above 0V, thereby switching the output of A_1 from $-V_{sat}$ to $+V_{sat}$. The cycle repeats and generates a triangular wave form.

It can be seen that the frequency of the square wave and triangular wave will be the same.

the frequency of the triangular waveform can be calculated as follows.

The effective voltage at point P during the time when output of A_1 is at $+V_{sat}$ level is given by

$$-V_{ramp} + \frac{R_2}{R_2+R_3}\left[+V_{sat} - (-V_{ramp})\right] \longrightarrow (1)$$

At $t = T_1$, the voltage at point p becomes equal to zero. Therefore from Eq (1)

$$-V_{ramp} = \frac{-R_2}{R_3}(+V_{sat}) \longrightarrow (2)$$

Similarly at $t = t_2$, when the output of A_1 switches from $-V_{sat}$ to $+V_{sat}$

$$V_{ramp} = \frac{-R_2}{R_3}(-V_{sat}) = \frac{R_2}{R_3}(V_{sat}) \longrightarrow (3)$$

Therefore peak to peak amplitude of triangular wave is $V_{O(P-P)} = +V_{ramp} - (-V_{ramp}) = \frac{2R_2}{R_3} V_{sat} \rightarrow (4)$

The output switches from ~~$-V_{sat}$~~ $-V_{ramp}$ to $+V_{ramp}$ in half the time period $\frac{T}{2}$. Putting the values in the basic integrator Equation.

$$V_O = -\frac{1}{RC}\int V_i\, dt$$

$$V_{O(P-P)} = -\frac{1}{R_1C_1}\int_0^{T/2} (-V_{sat})\, dt = \frac{V_{sat}}{R_1C_1}\left(\frac{T}{2}\right)$$

(or) $$T = 2R_1C_1\,\frac{V_{O(P-P)}}{V_{sat}}$$

Putting the value of $V_{O(P-P)}$ from Eq (4) we get

$$T = \frac{4 R_1 C_1 R_2}{R_3}$$

Hence the frequency of oscillation f_o is given by

$$f_o = \frac{1}{T} = \frac{R_3}{4 R_1 C_1 R_2}$$

Problem: Design the triangular wave generator so that $f_o = 2KHz$ and $V_{o(p-p)} = 7V$. The op-Amp is 1458/772 and supply voltages $= \pm 15V$.

Solution: Let $\pm V_{sat} = \pm 14V$

we know that $V_{o(p-p)} = 2 \frac{R_2}{R_3} V_{sat}$

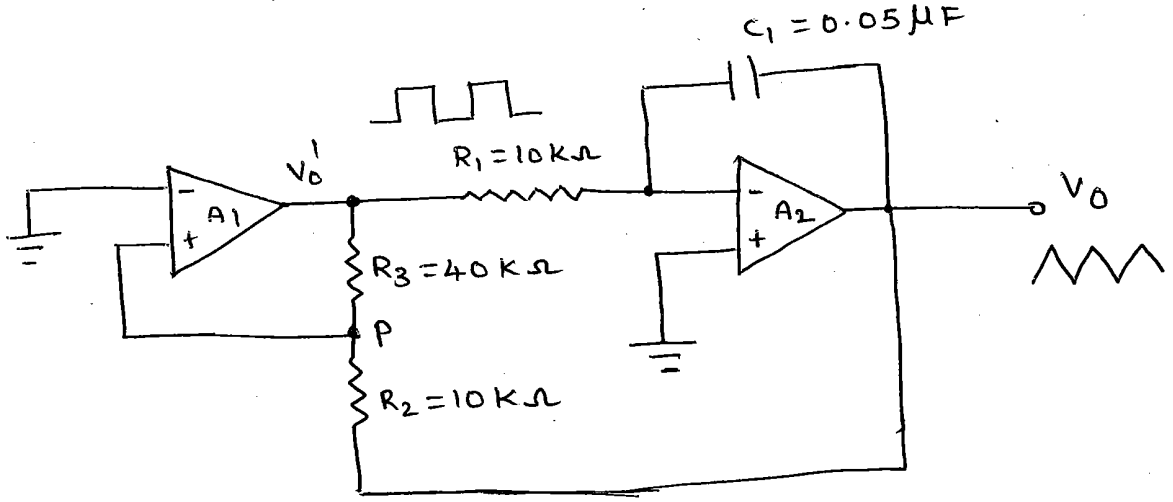
$$7 = 2 \times \frac{R_2}{R_3} \times 14 \Rightarrow R_2 = \frac{R_3}{4}$$

Let $R_2 = 10K\Omega$, then $R_3 = 40K\Omega$

And $f_o = \frac{R_3}{4 R_1 C_1 R_2}$

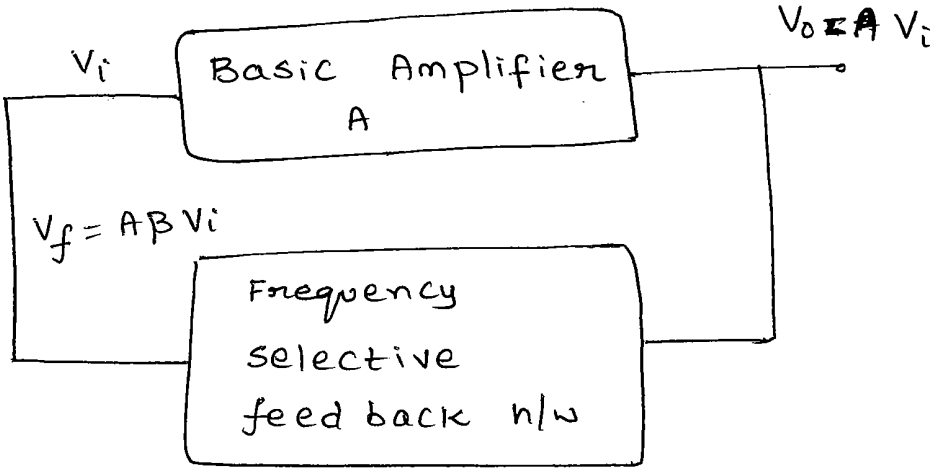
$$2 \times 10^3 = \frac{40K}{4 \times R_1 C_1 \times 10K} \Rightarrow R_1 C_1 = 0.5ms$$

Let $C_1 = 0.05\mu F \Rightarrow R_1 = 10K\Omega$



oscillators :

the basic structure of sine wave oscillators based on the use of feedback in amplifiers is shown below.



Barkhausen criterion :

1) Loop gain $A\beta = 1$

2) Total phase shift around a closed loop is 360° (or) 0°

1) RC phase shift oscillator :

the circuit of an RC phase shift oscillator is shown in figure below. The op-Amp is used in the inverting mode and therefore provides 180° phase shift. The additional phase of 180° is provided by the RC feedback network to obtain a total phase shift of 360°. the feedback network consists of three identical RC stages. Each of the RC stage provides a 60° phase shift so that the total phase shift due to feedback network is 180°.

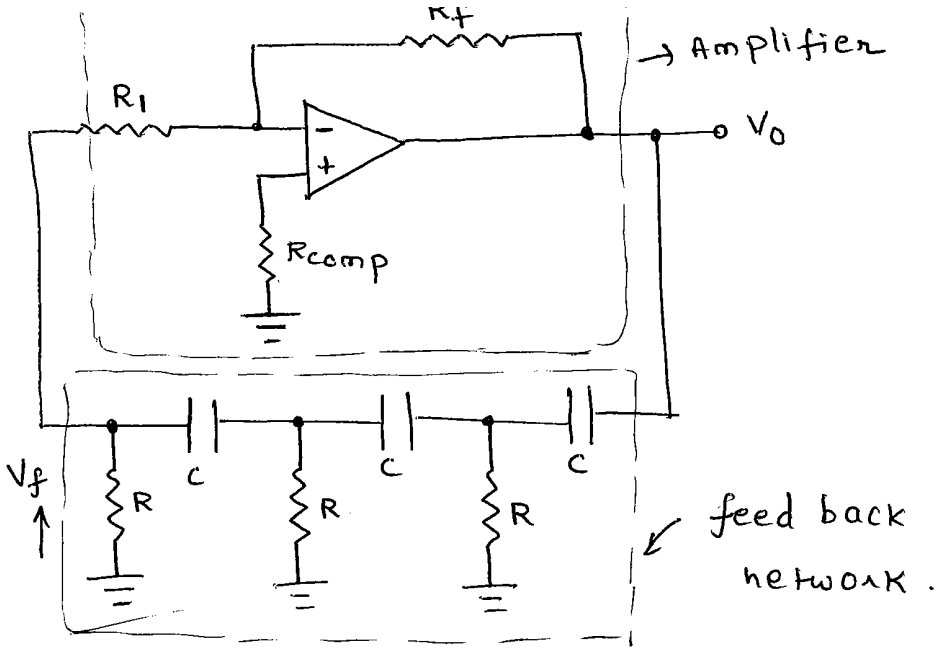
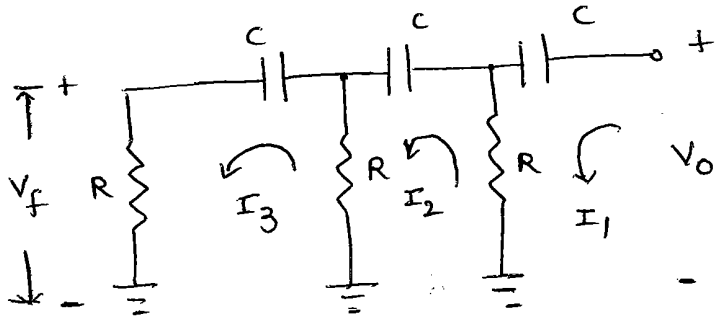


Fig : phase shift oscillator.

The feedback factor β of the RC network can be calculated by writing the KVL equations for fig(b)



Fig(b) : calculating β from the phase shift network.

$$I_1\left(R + \frac{1}{sC}\right) - I_2 R = V_o \longrightarrow (1)$$

$$-I_1 R + I_2\left(2R + \frac{1}{sC}\right) - I_3 R = 0 \longrightarrow (2)$$

$$-I_2 R + I_3\left(2R + \frac{1}{sC}\right) = 0 \longrightarrow (3)$$

and $V_f = I_3 R \longrightarrow (4)$

Solving eq's (1), (2) and (3) for I_3, we get

$$I_3 = \frac{V_o\, s^3 R^3 C^3}{1 + 5sRC + 6s^2R^2C^2 + s^3R^3C^3}$$

and $V_f = I_3 R = \dfrac{V_o s^3 R^3 C^3}{1 + 5SRC + 6s^2R^2C^2 + s^3R^3C^3}$

$$V_f = \frac{V_o}{1 + \frac{6}{SRC} + \frac{5}{s^2R^2C^2} + \frac{1}{s^3R^3C^3}}$$

Replacing $s = j\omega$, $s^2 = -\omega^2$ and $s^3 = -j\omega^3$, we get

$$\beta = \frac{V_f}{V_o} = \frac{1}{1 - \frac{6}{j\omega RC} - \frac{5}{\omega^2R^2C^2} + \frac{1}{j\omega^3R^3C^3}}$$

$$\beta = \frac{1}{(1 - 5\alpha^2) + j\alpha(6 - \alpha^2)} \rightarrow (6)(5) \quad \text{where } \alpha = \frac{1}{\omega RC}$$

For $A\beta = 1$, β should be real, that is imaginary term in Eq (5) must be zero. thus

$$\alpha(6 - \alpha^2) = 0 \quad \Rightarrow \quad \alpha^2 = 6$$

$$\Rightarrow \alpha = \sqrt{6} \quad \Rightarrow \quad \frac{1}{\omega RC} = \sqrt{6} \quad \Rightarrow \quad \omega = \frac{1}{\sqrt{6}RC}$$

The frequency of oscillation

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

putting $\alpha^2 = 6$ in Eq (5) we get $\beta = -\frac{1}{29}$

The negative sign indicates that the feedback network produces a phase shift of 180° so

$$|\beta| = \frac{1}{29} \quad \text{But} \quad A\beta = 1 \quad \Rightarrow \quad A = 29$$

Therefore for sustained oscillations

$$|A| \geq 29$$

That is the gain of the inverting op-Amp should be atleast 29, or $R_f = 29 R_1$. The gain A_V is kept greater than 29 to ensure that variations in circuit parameters will not make $A\beta < 1$, otherwise oscillations will die out.

problem: Design a phase shift oscillator to oscillate at 100 Hz.

Solution: $f_o = \frac{1}{2\pi RC\sqrt{6}}$

[Note: Draw the RC phase shift oscillator circuit and represent all the component values]

Let $C = 0.1\,\mu F$

$$100 = \frac{1}{2\pi \times R \times 0.1 \times 10^{-6} \times \sqrt{6}} \Rightarrow R = 6.49\,K\Omega$$

Use $R = 6.5\,K\Omega$

To prevent loading of the amplifier by RC network

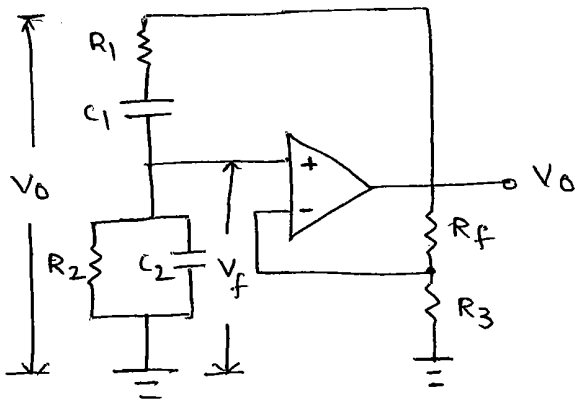
$R_1 \leq 10R$, $R_1 = 10 \times 6.5\,K\Omega = 65\,K\Omega$

Since $R_f = 29 R_1 \Rightarrow R_f = 29 \times 65\,K\Omega = 1885\,K\Omega$.

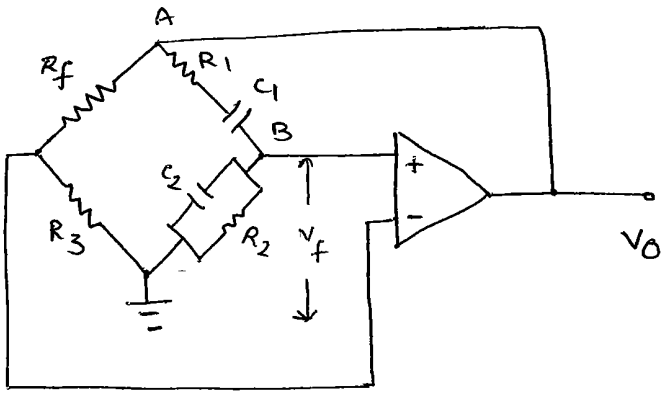
(2) Wien Bridge oscillator:

Another commonly used audio frequency oscillator is a wien bridge oscillator. the circuit is shown in figure below. The feedback signal in this circuit is connected to the non inverting (+) input terminal so that the op-Amp is working as a non-inverting Amplifier. Therefore feedback network need not provide any phase shift. The circuit can be viewed as a wien bridge with a series RC network in one arm and a parallel RC network in the adjoining arm. Resistors R_1 and R_f connected in the remaining two arms.

The condition of zero phase shift around the circuit is achieved by balancing the bridge.

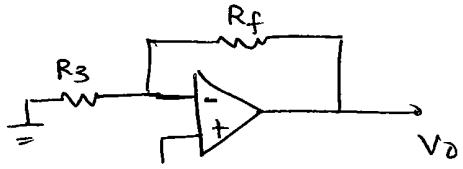


Fig(a) : Wien Bridge oscillator.



Fig(b) : Wien Bridge showing the bridge network.

The circuit has been redrawn to show the bridge network in fig(b). The ac output signal of the op-Amp Amplifier is fed back to point A of the bridge. The feedback signal V_f across the parallel combination R_2C_2 is applied to the non-inverting terminal of op-Amp



The gain of the op-Amp is

$$A = 1 + \frac{R_f}{R_3} \longrightarrow (1)$$

and V_f from fig(a)

$$V_f = V_o \times \frac{Z_2}{Z_1 + Z_2} \longrightarrow (2)$$

where $Z_1 = R_1 + \frac{1}{sC_1}$

$Z_2 = R_1 \,||\, \frac{1}{sC_2}$

Putting the values Z_1 and Z_2 in Eq (2)

$$\beta = \frac{V_f}{V_o} = \frac{sR_2C_1}{1 + s(R_1C_1 + R_2C_2 + R_2C_1) + s^2R_1R_2C_1C_2} \longrightarrow (3)$$

putting $s = j\omega$

$$\beta = \frac{j\omega R_2C_1}{1 + j\omega(R_1C_1 + R_2C_2 + R_2C_1) - \omega^2 R_1R_2C_1C_2} \longrightarrow (4)$$

In order β to be a real quantity, in Eq (4)

$$1 - \omega^2 R_1 R_2 C_1 C_2 = 0$$

$$\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

the frequency of oscillation $f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$

From Eq (4) if $1 - \omega^2 R_1 R_2 C_1 C_2 = 0$ then

$$\beta = \frac{R_2 C_1}{R_1 C_1 + R_2 C_2 + R_2 C_1}$$

For $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C$

$$f_0 = \frac{1}{2\pi RC} \quad \text{and} \quad \beta = \frac{1}{3}$$

Since $|A\beta| \geq 1 \Rightarrow$ $\boxed{A \geq 3}$

$$1 + \frac{R_f}{R_3} = 3 \Rightarrow \boxed{R_f = 2R_3}$$

problem: Design wien bridge oscillator with $f_0 = 1000$ Hz

solution:

$$f_0 = \frac{1}{2\pi RC}$$

Let $C = 0.05\ \mu F \Rightarrow R = \frac{1}{2\pi \times 1000 \times 0.05 \times 10^{-6}}$

$$R = 3.1\ K\Omega$$

Take $R = 3\ K\Omega$

Take $R_1 = 10R = 30\ K\Omega$

$R_f = 2R_1 \Rightarrow R_f = 60\ K\Omega$ (use 100 KΩ potentiometer)

[Note: Draw the wien bridge oscillator circuit and represent all the component values]

UNIT - III

ACTIVE FILTERS

Introduction:

Electric filters are used in circuits which require the separation of signals according to their frequencies. Filters are widely used in communication and signal processing and in form or another in almost all sophisticated electronic instruments. such filters can be built from

i) Passive RLC components ii) Crystals

iii) Resistors, capacitors and op-Amps [Active filters]

RC Active Filters :

A frequency selective electric circuit that passes electric signals of specific band of frequencies and attenuates the signals of frequencies outside the band is called an electric filter.

The simplest way to make a filter is by using passive components (Resistors, capacitors, inductors) This works well for high frequencies that is radio frequencies. However at audio frequencies inductors become problematic, as the inductors become large, heavy and expensive. so at low frequencies passive filter are not suitable.

Active filters overcome aforementioned problems of passive filters. they use op-Amp as the active element and resistors and capacitors as the passive

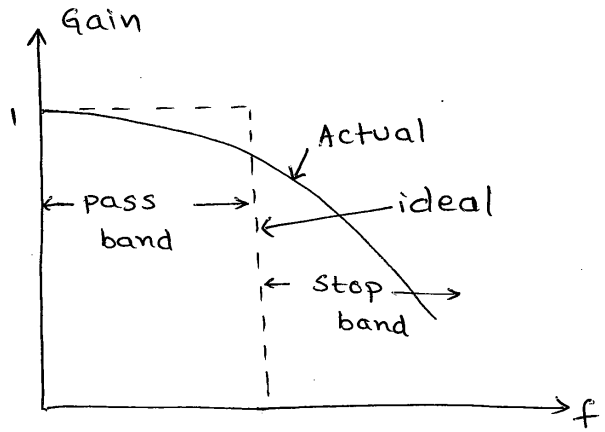
elements. The active filters by enclosing a capacitor in the feedback loop avoid using inductors. In this way inductorless active RC filters can be obtained.

Also op-Amps is used in non inverting configuration, it offers high input impedance and low output impedance. This will improve the load drive capacity and is isolated from the frequency determining network. Because of the high input impedance of the op-Amps large value resistors can be used, there by reducing the size and cost of the capacitors required in the design.

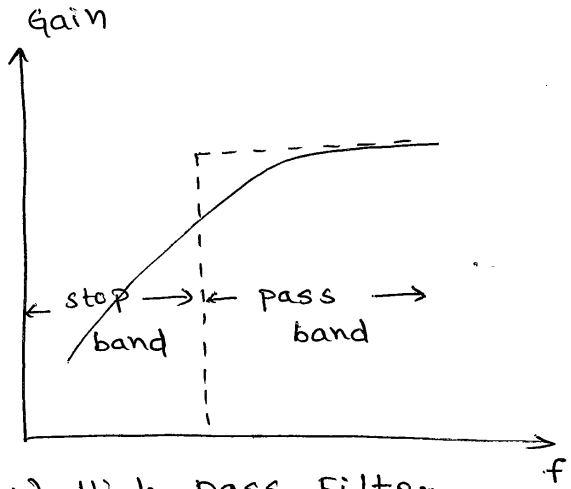
The most commonly used Filters are

1. Low pass Filter (LPF)
2. High pass Filter (HPF)
3. Band pass Filter (BPF)
4. Band Reject Filter (BRF) (or) Band stop Filter (BSF)

The Frequency response of these filters is shown in figure below where dashed curve indicates the ideal response and solid curve shows the practical filter response.



a) Low pass Filter.



b) High pass Filter

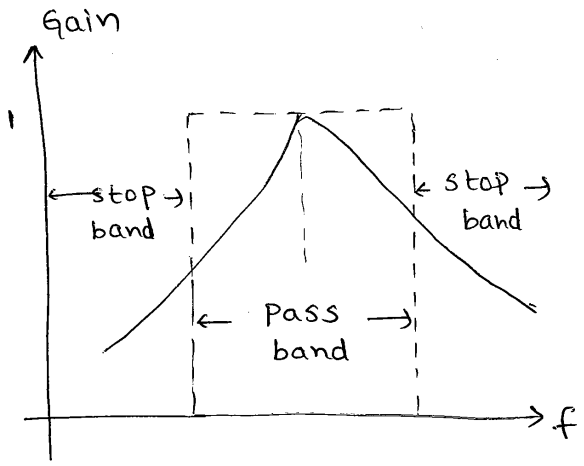


Fig: Band pass Filter.

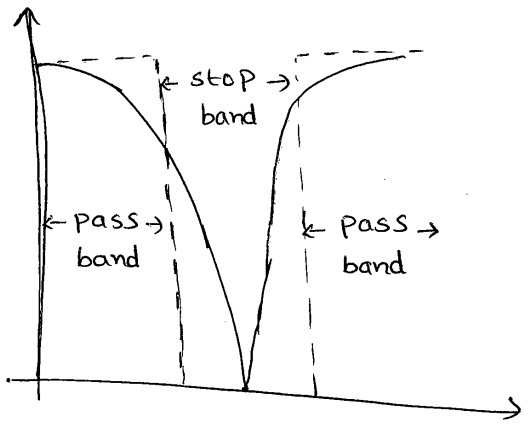
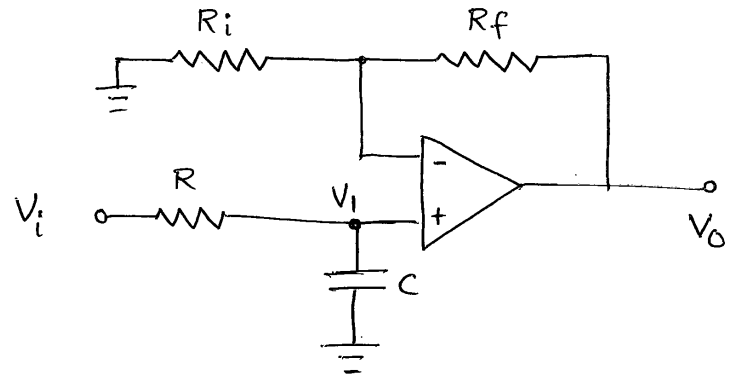


Fig: Band Reject Filter.

First order lowpass Filter:

A first order filter consists of a single RC network connected to the (+) input terminal of a non-inverting op-Amp amplifier and is shown in figure below. Resistors R_i and R_f determine the gain of the Filter in the pass band.



The closed loop gain A_o of the op-Amp is

$$A_o = \frac{V_o(s)}{V_1(s)} = 1 + \frac{R_f}{R_i} \longrightarrow (1)$$

$$V_1(s) = V_i(s) \times \frac{\frac{1}{sC}}{R + \frac{1}{sC}}$$

$$\Rightarrow \frac{V_1(s)}{V_i(s)} = \frac{1}{1 + sRC} \longrightarrow (2)$$

$$\therefore \quad H(s) = \frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_1(s)} \times \frac{V_1(s)}{V_i(s)}$$

$$H(s) = \left[1 + \frac{R_f}{R_i}\right] \frac{1}{1+sRC} \qquad \left[\text{From } ① \wedge ②\right]$$

$$H(s) = \frac{A_0}{1+sRC} \longrightarrow ③$$

$$H(s) = \frac{A_0}{1 + \frac{s}{\omega_h}} \quad \text{where} \quad \omega_h = \frac{1}{RC}$$

$$H(j\omega) = \frac{A_0}{1 + j\left(\frac{\omega}{\omega_h}\right)} = \frac{A_0}{1 + j\left(\frac{f}{f_h}\right)}$$

Here $\omega_h = \frac{1}{RC} \implies f_h = \frac{1}{2\pi RC}$

where f_h = upper cut-off frequency.

$$H(j\omega) = \frac{A_0}{1 + j\left(\frac{f}{f_h}\right)}$$

$$\Rightarrow |H(j\omega)| = \frac{A_0}{\sqrt{1 + \left(\frac{f}{f_h}\right)^2}}$$

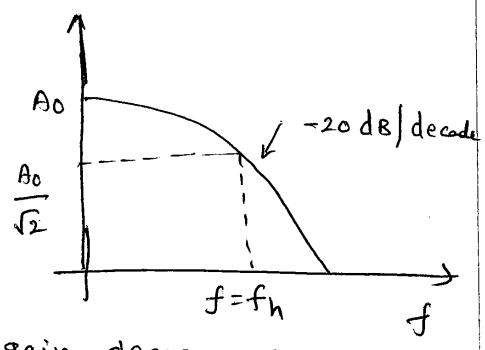
If $f << f_h \longrightarrow \frac{f}{f_h}$ is negligible, $|H(j\omega)| = A_0$

At $f = f_h \implies |H(j\omega)| = \frac{A_0}{\sqrt{2}}$

If $f >> f_h \implies |H(j\omega)| = 0$

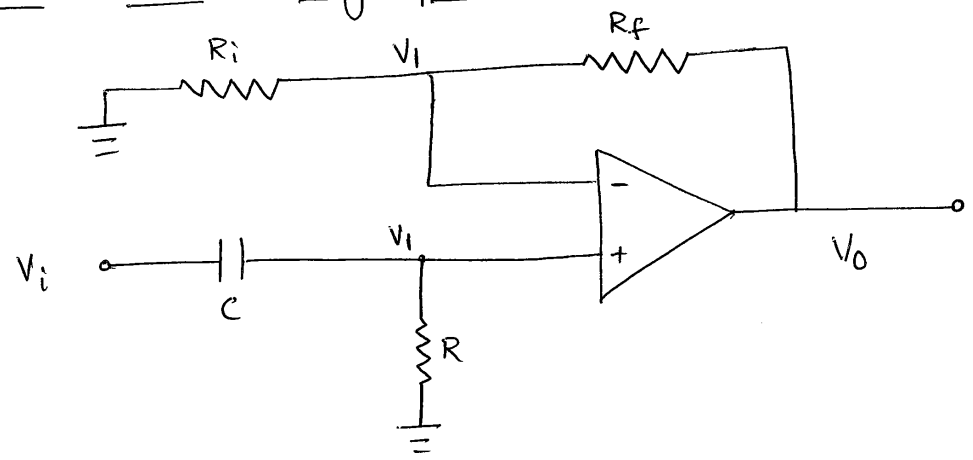
Here $H(s) = \frac{A_0}{1 + \frac{s}{\omega_h}}$

$$\Rightarrow H(s) = \frac{A_0 \omega_h}{s + \omega_h}$$



Here the gain decreases at a rate of $-20\,dB/decade$

First order High pass filter :



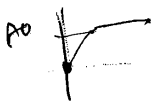
Here $A_0 = \frac{V_0}{V_1} = 1 + \frac{R_f}{R_i}$ ⟶ ①

$$V_1(s) = V_i(s) \frac{R}{R + \frac{1}{sC}} \longrightarrow ②$$

$$\frac{V_1(s)}{V_i(s)} = \frac{R}{R + \frac{1}{sC}} = \frac{1}{1 + \frac{1}{SRC}} \longrightarrow ③$$

$$H(s) = \frac{V_0(s)}{V_i(s)} = \frac{V_0(s)}{V_1(s)} \times \frac{V_1(s)}{V_i(s)}$$

$$H(s) = A_0 \times \frac{1}{1 + \frac{1}{SRC}}$$



$$H(j\omega) = \frac{A_0}{1 + \frac{1}{j\omega RC}}$$

$$H(j\omega) = \frac{A_0}{1 - j\frac{\omega_L}{\omega}} \quad \text{where} \quad \omega_L = \frac{1}{RC}$$

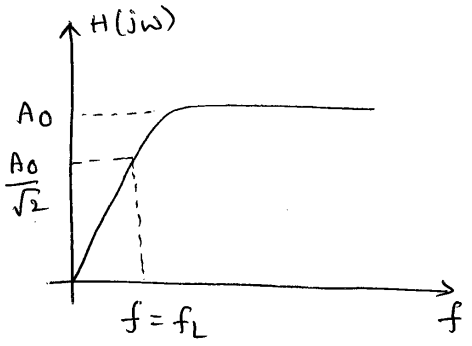
$$|H(j\omega)| = \frac{A_0}{\sqrt{1 + \left(\frac{\omega_L}{\omega}\right)^2}} = \frac{A_0}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$$

where $f_L = \frac{1}{2\pi RC}$ = Lower cut-off frequency

$f << f_L \Rightarrow |H(j\omega)| = 0$

$f = f_L \Rightarrow |H(j\omega)| = \frac{A_0}{\sqrt{2}}$

$f >> f_L \Rightarrow |H(j\omega)| = A_0$



Second order Active Filter :

An improved filter response can be obtained by using a second order active filter. A second order filter consists of two RC pairs and has a roll-off rate of -40 dB/decade.

A General second order filter (sallen Key filter) is shown in figure below.

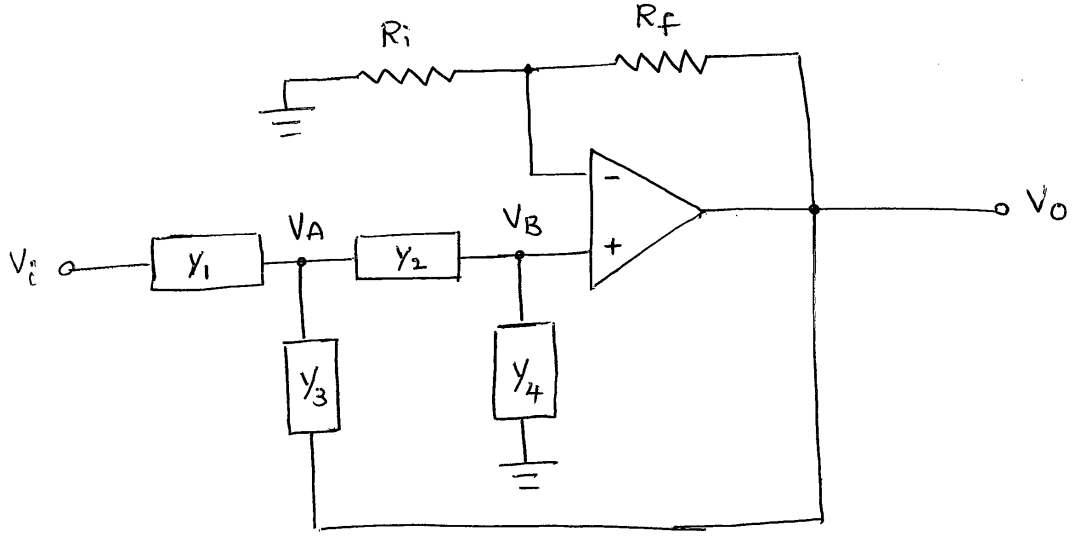


Fig: sallen-Key filter (General second order filter)

Here $A_0 = 1 + \frac{R_f}{R_i} = \frac{V_o}{V_B} \Rightarrow \left[V_B = \frac{V_o}{A_0} \longrightarrow (1) \right]$

writing KCL at node A

$(V_i - V_A) Y_1 = (V_A - V_B) Y_2 + (V_A - V_o) Y_3$

$$V_i Y_1 = V_A (Y_1 + Y_2 + Y_3) - V_B Y_2 - V_0 Y_3$$

$$V_i Y_1 = V_A (Y_1 + Y_2 + Y_3) - \frac{V_0}{A_0} Y_2 - V_0 Y_3 \rightarrow (2) \quad [\because \text{From } (1)]$$

writing KCL at node B

$$(V_A - V_B) Y_2 = V_B Y_4$$

$$V_A Y_2 = V_B (Y_2 + Y_4)$$

$$\Rightarrow V_A = \frac{V_0 (Y_2 + Y_4)}{A_0 Y_2} \longrightarrow (3)$$

Substituting (3) in (2)

$$V_i Y_1 = \frac{V_0 (Y_2 + Y_4)}{A_0 Y_2} (Y_1 + Y_2 + Y_3) - \frac{V_0}{A_0} Y_2 - V_0 Y_3$$

simplifying $$\frac{V_0}{V_i} = \frac{A_0 Y_1 Y_2}{Y_4 (Y_1 + Y_2 + Y_3) + Y_1 Y_2 + (1 - A_0) Y_2 Y_3} \rightarrow (4)$$

second order low pass filter :

To make a low pass filter $Y_1 = Y_2 = \frac{1}{R}$

$$Y_3 = Y_4 = sC$$

Substituting the above values in Eq (4)

$$\frac{V_0(s)}{V_i(s)} = \frac{A_0 / R^2}{sC\left[\frac{2}{R} + sC\right] + \frac{1}{R^2} + (1 - A_0)\frac{sC}{R}}$$

$$H(s) = \frac{A_0}{3SRC + 1 + s^2 R^2 C^2 - A_0 SRC}$$

$$H(s) = \frac{A_0}{s^2 R^2 C^2 + SRC(3 - A_0) + 1}$$

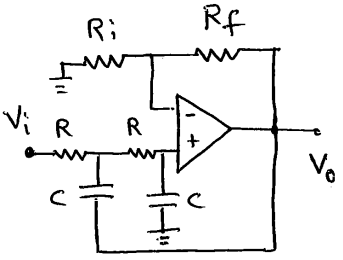


Fig: second order Low pass filter.

$$H(s) = \frac{A_0 / R^2C^2}{s^2 + \frac{s}{RC}(3 - A_0) + \frac{1}{R^2C^2}}$$

Put $\omega_h = \frac{1}{RC}$

$$H(s) = \frac{A_0 \omega_h^2}{s^2 + s\omega_h(3 - A_0) + \omega_h^2} \longrightarrow (5)$$

$$H(s) = \frac{A_0 \omega_h^2}{s^2 + \alpha \omega_h s + \omega_h^2}$$

where α is damping co-efficient $\alpha = 3 - A_0$

$$H(j\omega) = \frac{A_0 \omega_h^2}{(j\omega)^2 + \alpha \omega_h (j\omega) + \omega_h^2}$$

$$H(j\omega) = \frac{A_0}{\left(\frac{j\omega}{\omega_h}\right)^2 + j\frac{\omega}{\omega_h}\alpha + 1}$$

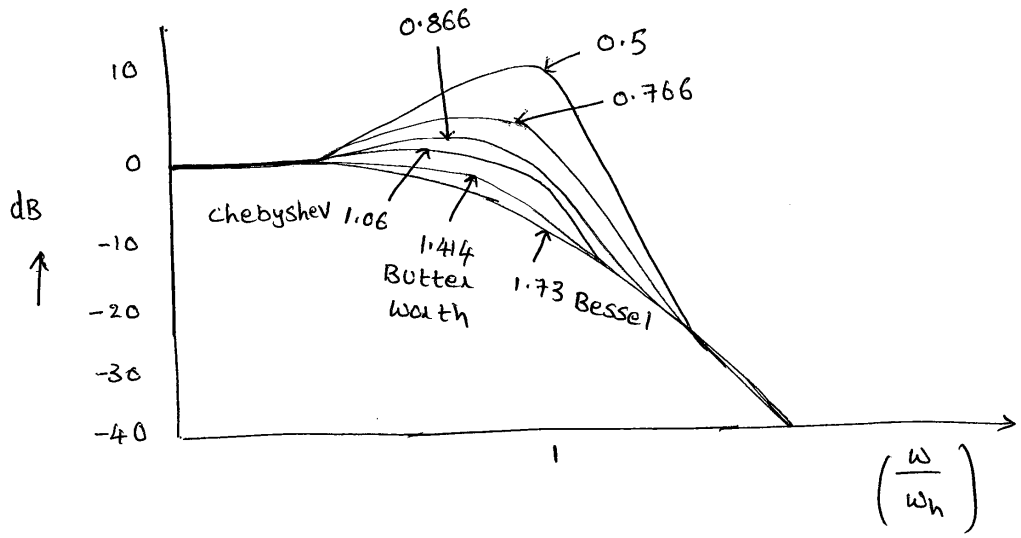
Let $s_h = \frac{j\omega}{\omega_h} \Rightarrow H(j\omega) = \frac{A_0}{s_h^2 + \alpha s_h + 1}$

$$20 \log\left(H(j\omega)\right) = 20 \log \frac{A_0}{\left(\frac{j\omega}{\omega_h}\right)^2 + \alpha\left(\frac{j\omega}{\omega_h}\right) + 1}$$

$$20 \log\left|H(j\omega)\right| = 20 \log \frac{A_0}{1 - \left(\frac{\omega}{\omega_h}\right)^2 + j\alpha\left(\frac{\omega}{\omega_h}\right)}$$

$$20 \log\left|H(j\omega)\right| = 20 \log \frac{A_0}{\sqrt{\left[1 - \left(\frac{\omega}{\omega_h}\right)^2\right]^2 + \left(\alpha \frac{\omega}{\omega_h}\right)^2}} \longrightarrow (6)$$

The frequency response for different values of α is shown in figure below



The frequency response for different values of α is shown in figure above. It may seen that

① For a heavily damped filter ($\alpha > 1.7$) the response is stable

② As α is reduced, the response exhibits overshoot. and ripple begins to appear at the early stage of pass band.

③ If α is reduced too much, the filter may become oscillatory.

④ the flattest pass band occurs for damping co-efficient of 1.414. this is called a butterworth ~~or~~ filter. Audio filters are usually Butterworth. Audio filters are usually butterworth.

⑤ the chebyshev filters are more lightly damped that is the damping co-efficient α is 1.06. However this increases overshoot. The advantage however is a faster initial roll-off compared to butterworth.

⑥ A Bessel filter is heavily damped and has a damping co-efficient of 1.73. this gives better pulse response. however causes attenvation in the upper band of the pass band.

Here the butterworth filter is generally prefered because of his maximally flat response with damping co-efficient $\alpha = 1.414$.

Eq ⑥ becomes

$$20 \log |H(j\omega)| = 20 \log \frac{A_0}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^4 - 2\left(\frac{\omega}{\omega_h}\right)^2 + \left(1.414 \frac{\omega}{\omega_h}\right)^2}}$$

$$\alpha = 1.414 = \sqrt{2}, \quad (1.414)^2 = \alpha^2 = 2$$

$$20 \log |H(j\omega)| = 20 \log \frac{A_0}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^4 - 2\left(\frac{\omega}{\omega_h}\right)^2 + 2\left(\frac{\omega}{\omega_h}\right)^2}}$$

$$20 \log |H(j\omega)| = 20 \log \frac{A_0}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^4}} = 20 \log \frac{A_0}{\sqrt{1 + \left(\frac{f}{f_h}\right)^4}}$$

For n^{th} order Butterworth low pass filter

$$|H(j\omega)| = \frac{A_0}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^{2n}}}$$

$$\frac{|H(j\omega)|}{A_0} = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^{2n}}}$$

Problem 1 : Design a first order low pass filter so that cut-off frequency by 2KHz and pass band gain 1

Solution: $f_h = \frac{1}{2\pi RC} \Rightarrow 2 \times 10^3 = \frac{1}{2\pi RC}$

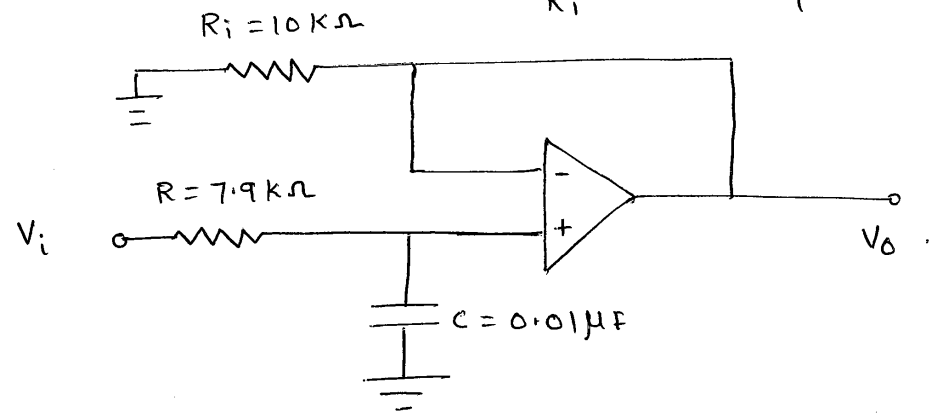
choose $C = 0.01\mu F$, $R = 7.9k\Omega$

pass band gain = 1

$A_0 = 1 \Rightarrow A_0 = 1 + \frac{R_f}{R_i}$

$1 = 1 + \frac{R_f}{R_i}$

$\Rightarrow \frac{R_f}{R_i} = 0$ $\left[\text{if } R_f = 0\Omega, \; R_i = 10k\Omega \right]$



Problem 2 : Design a second order butterworth low pass filter having upper cut-off frequency 1 KHz.

Solution : $f_h = \frac{1}{2\pi RC}$

Here $f_h = 1KHz$, choose $C = 0.01\mu F$

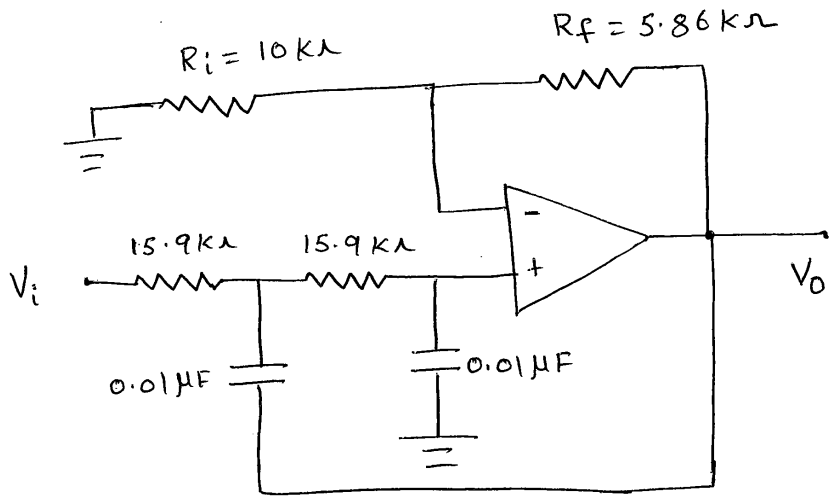
then $R = 15.9k\Omega$

$\alpha = 1.414$

$3 - A_0 = 1.414 \Rightarrow A_0 = 1.586$

$$1 + \frac{R_f}{R_i} = 1.586 \Rightarrow \frac{R_f}{R_i} = 0.586$$

Let $R_i = 10\ K\Omega$, $R_f = 5.86\ K\Omega$.



Problem-3 :

Determine the order of a low pass butter worth filter to provide 40 dB attenuation at $\frac{\omega}{\omega_h} = 2$

Solution : $\frac{\omega}{\omega_h} = 2$

$$\frac{H(j\omega)}{A_0} = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^{2n}}} \longrightarrow (1)$$

$$20 \log \frac{|H(j\omega)|}{A_0} = -40$$

$$\frac{|H(j\omega)|}{A_0} = 0.01 \longrightarrow (2)$$

Equating (1) and (2) $\frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^{2n}}} = 0.01$

After simplifying $n = 6.63$

Since the order of the filter must be an integer so $\boxed{n = 7}$

Second order High pass filter :

From the generalized second order filter putting $Y_1 = Y_2 = sC$ and $Y_3 = Y_4 = \frac{1}{R}$ then

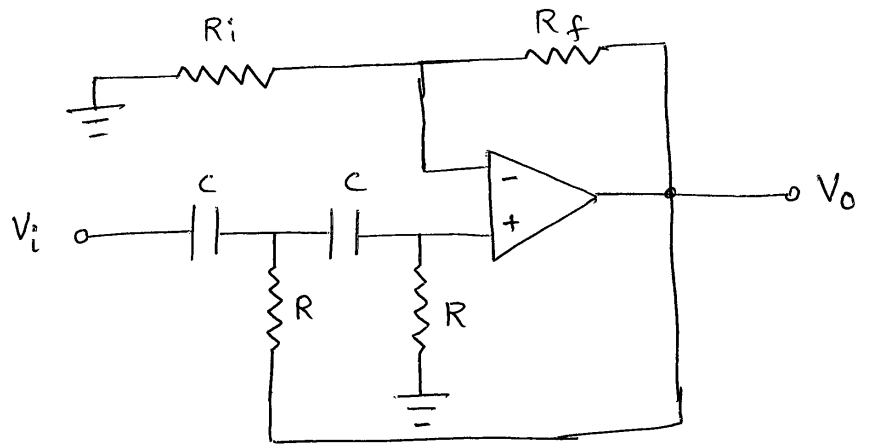


Fig: second order Highpass butterworth filter.

The transfer function of generalized second order filter is given by

$$\frac{V_o}{V_i} = \frac{A_o Y_1 Y_2}{Y_4(Y_1 + Y_2 + Y_3) + (1 - A_o) Y_2 Y_3 + Y_1 Y_2} \longrightarrow (1)$$

Here $Y_1 = sC$, $Y_2 = sC$, $Y_3 = \frac{1}{R}$, $Y_4 = \frac{1}{R}$

$$H(s) = \frac{A_o s^2 C^2}{\frac{1}{R}\left(sC + sC + \frac{1}{R}\right) + (1 - A_o)\frac{sC}{R} + s^2C^2}$$

$$H(s) = \frac{A_o}{\frac{1}{s^2R^2C^2} + (3 - A_o)\frac{1}{sRC} + 1}$$

Put $s = j\omega$

$$|H(j\omega)| = \frac{A_o}{1 + \frac{1}{j^2\omega^2R^2C^2} + (3 - A_o)\frac{1}{j\omega RC}}$$

$$|H(j\omega)| = \frac{A_0}{1 - \frac{1}{\omega^2 R^2 C^2} - j\alpha \frac{1}{\omega RC}}$$

$$|H(j\omega)| = \frac{A_0}{1 - \left(\frac{\omega_L}{\omega}\right)^2 - j\alpha\left(\frac{\omega_L}{\omega}\right)}$$

where $\omega_L = \frac{1}{RC}$

$$|H(j\omega)| = \frac{A_0}{\sqrt{\left[1 - \left(\frac{\omega_L}{\omega}\right)^2\right]^2 + \left(\alpha \frac{\omega_L}{\omega}\right)^2}}$$

$\alpha = 1.414 = \sqrt{2}$ [For Butterworth filter]

$\alpha^2 = 2$, so for second order High pass filter,

$$|H(j\omega)| = \frac{A_0}{\sqrt{1 + \left(\frac{\omega_L}{\omega}\right)^4}}$$

For nth order Highpass filter

$$\frac{|H(j\omega)|}{A_0} = \frac{1}{\sqrt{1 + \left(\frac{\omega_L}{\omega}\right)^{2n}}} = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^{2n}}}$$

Problem 4: Design a first order highpass filter so that lower cut-off frequency by 1KHz and pass band gain of 2.

Solution: Here $f_L = \frac{1}{2\pi RC}$

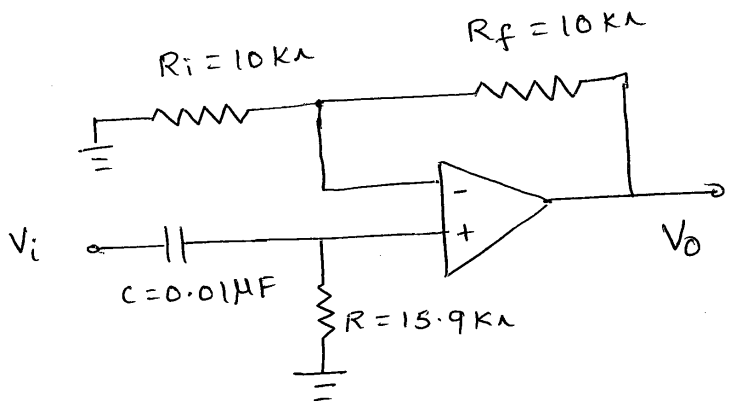
$f_L = 1 \times 10^3$, Choose $C = 0.01\,\mu F$

then $R = 15.9\,K\Omega$

pass band gain = 2

$2 = 1 + \frac{R_f}{R_i}$

then $R_f = R_i = 10\,K\Omega$



Band pass filters:

There are two types of band pass filters which are classified as per the figure of merit or Quality factor 'Q'.

i) Narrow Band pass filter ($Q > 10$)

ii) Wide Band pass filter ($Q < 10$)

The following Relationship is important

$$Q = \frac{f_o}{BW} = \frac{f_o}{f_h - f_L} \quad \text{and} \quad f_o = \sqrt{f_h f_L}$$

where f_h = Upper Cut-off frequency

f_L = Lower Cut-off frequency

f_o = central frequency.

i) Narrow Band pass filter:

The circuit of Narrow Band pass filter has two feedback paths and the op-Amp is used in inverting mode of operation. The circuit is shown in figure below.

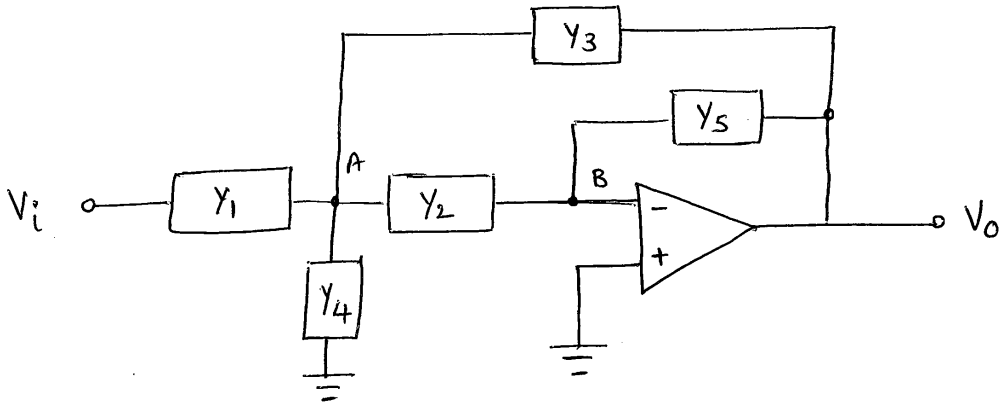


Fig: Band Pass Configuration

writing KCL at node 'A' $\left[V_B = 0 \right]$

$$(V_i - V_A) Y_1 = (V_A - 0) Y_2 + (V_A - V_o) Y_3 + V_A Y_4$$

$$V_i Y_1 + V_o Y_3 = V_A (Y_1 + Y_2 + Y_3 + Y_4) \longrightarrow (1)$$

writing KCL at node 'B'

$$(V_A - 0) Y_2 = (0 - V_o) Y_5$$

$$V_A = \frac{-V_o Y_5}{Y_2} \longrightarrow (2)$$

Substituting (2) in (1)

$$V_i Y_1 + V_o Y_3 = \frac{-V_o Y_5}{Y_2} (Y_1 + Y_2 + Y_3 + Y_4)$$

$$V_i Y_1 = \frac{-V_o Y_5}{Y_2} (Y_1 + Y_2 + Y_3 + Y_4) - V_o Y_3$$

$$V_i Y_1 = V_o \left[\frac{-Y_5}{Y_2} (Y_1 + Y_2 + Y_3 + Y_4) - Y_3 \right]$$

$$\frac{V_o}{V_i} = \frac{-Y_1 Y_2}{Y_5 (Y_1 + Y_2 + Y_3 + Y_4) + Y_2 Y_3} \longrightarrow (2)$$

Consider the circuit of Narrow Band pass filter

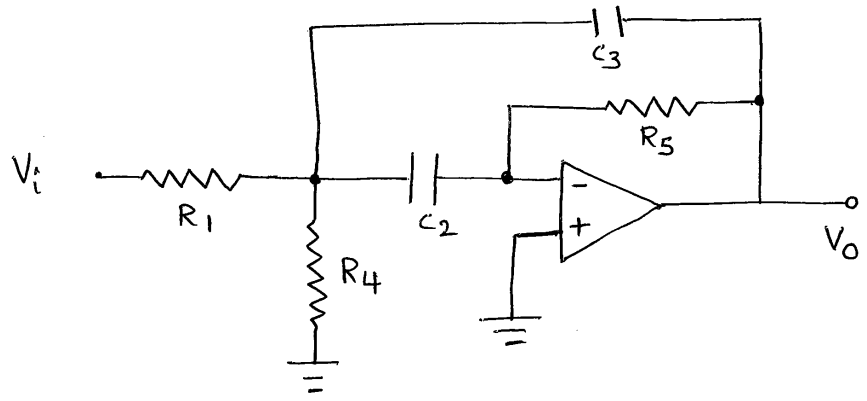


Fig : second order Narrow Band pass filter.

on comparing the above circuit with ~~sta~~ Band pass configuration, ~~put~~

$Y_1 = G_1$, $Y_2 = sC_2$, $Y_3 = sC_3$, $Y_4 = G_4$ and $Y_5 = G_5$

Then the transfer function becomes

$$H(s) = \frac{V_0(s)}{V_i(s)} = \frac{-sG_1C_2}{s^2C_2C_3 + s(C_2+C_3)G_5 + G_5(G_1+G_4)} \longrightarrow (3)$$

(or)

$$H(s) = \frac{-G_1}{sC_3 + G_5\frac{C_2+C_3}{C_2} + \frac{(G_1+G_4)G_5}{sC_2}} \longrightarrow (4)$$

The transfer function of above equation is equivalent to the gain expression of a parallel RLC circuit shown in figure below driven by a current source $G'V_i$

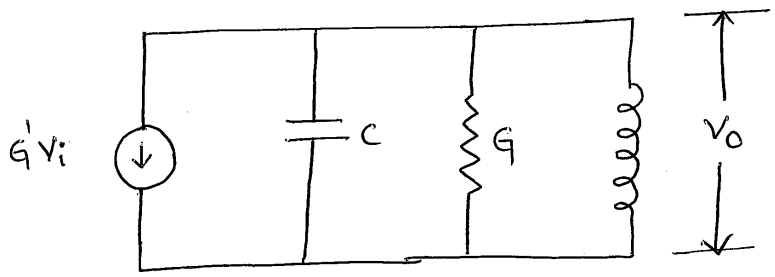


Fig : A parallel RLC circuit.

the gain expression is

$$\frac{V_o(s)}{V_i(s)} = -\frac{G'}{Y} = -\frac{G'}{sC + G + \frac{1}{sL}} \longrightarrow (5)$$

comparing Eq (4) and (5)

$$G' = G_1 \longrightarrow (6)$$

$$L = \frac{C_2}{G_5 (G_1 + G_4)} \longrightarrow (7)$$

$$G = \frac{G_5 (C_2 + C_3)}{C_2} \longrightarrow (8)$$

$$C = C_3 \longrightarrow (9)$$

At resonance the parallel RLC circuit has a unity power factor ie imaginary part is zero which gives the resonant frequency ω_0 as

$$\omega_0^2 = \frac{1}{LC} = \frac{G_5 (G_1 + G_4)}{C_2 C_3} \longrightarrow (10)$$

the gain at resonance is

$$\left.\frac{V_o}{V_i}\right|_{\omega=\omega_0} = -\frac{G'}{G} = -\frac{G_1}{G} = -\frac{\left(\frac{G_1}{G_5}\right) C_2}{C_2 + C_3} \longrightarrow (11)$$

$$\left.\frac{V_o}{V_i}\right|_{\omega=\omega_0} = -\frac{\left(\frac{R_5}{R_1}\right) C_2}{C_2 + C_3} \longrightarrow (12)$$

The Q-factor at resonance is

$$Q_0 = \frac{\omega_0 L}{R} = \omega_0 RC = \frac{\omega_0 C}{G} = \frac{\omega_0 C_2 C_3}{(C_2 + C_3) G_5} \longrightarrow (13)$$

The Bandwidth BW is given by

$$BW = f_h - f_L = \frac{f_0}{Q_0} = \frac{\omega_0}{2\pi Q_0} = \frac{\omega_0}{2\pi R \omega_0 C}$$

$$BW = \frac{1}{2\pi RC} = \frac{G}{2\pi C} = \frac{G_5 (C_2 + C_3)}{2\pi C_2 C_3} \longrightarrow (14)$$

and the centre freq $f_0 = \sqrt{f_h f_L}$

Now for $C_2 = C_3 = C$, the gain at resonance freq from Eq (12) is

$$\left.\frac{V_0}{V_i}\right|_{\omega=\omega_0} = -\frac{R_5}{2R_1} = -A_0 \longrightarrow (15)$$

$$\omega_0 = \frac{\sqrt{G_5 (G_1 + G_4)}}{C} \longrightarrow (16)$$

$$BW = \frac{G_5}{\pi C} = \frac{1}{\pi R_5 C} \longrightarrow (17)$$

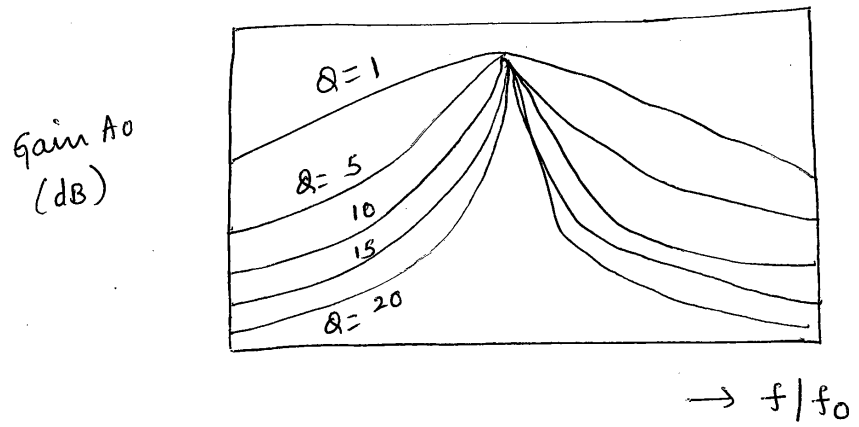
Using Eq's (13), (15), (16) the standard transfer function of a bandpass filter is obtain as

$$H(s) = \frac{-A_0 \left(\frac{\omega_0}{Q}\right) s}{s^2 + \left(\frac{\omega_0}{Q}\right) s + \omega_0^2} = \frac{-A_0 \alpha \omega_0 s}{s^2 + \alpha \omega_0 s + \omega_0^2} \longrightarrow (18)$$

$$20 \log |H(s)| = 20 \log \left| \frac{A_0 \alpha \omega_0 s}{s^2 + \alpha \omega_0 s + \omega_0^2} \right| \longrightarrow (19)$$

Single opAmp It is obivious from Eq (18) that for $\omega << \omega_0$ and $\omega >> \omega_0$ the gain is zero and for $\omega = \omega_0$ the gain is A_0.

Single op-Amp band pass filter response is given by



Wide band pass filter :

A wide band pass filter can be formed by cascading a high pass filter and low pass filter sections.

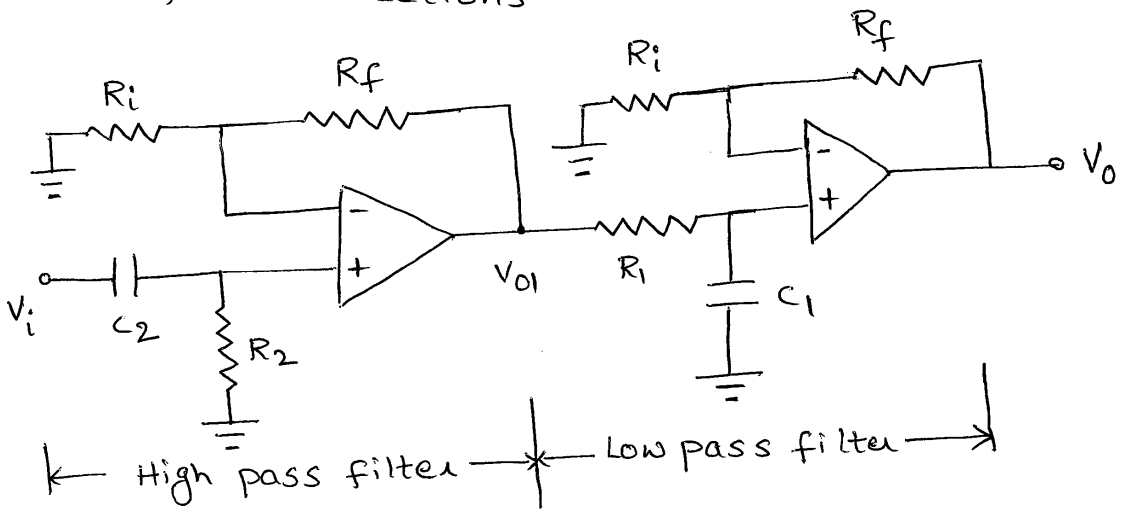


Fig : wide band pass filter

$$H_{HP} = \left(1 + \frac{R_f}{R_i}\right)\left(\frac{j2\pi f R_2 C_2}{1 + j2\pi f R_2 C_2}\right)$$

Let $A_{01} = 1 + \frac{R_f}{R_i}$

$$H_{HP} = \frac{A_{01}\, j\left(\frac{f}{f_L}\right)}{1 + j\left(\frac{f}{f_L}\right)} \quad \text{where} \quad f_L = \frac{1}{2\pi R_2 C_2}$$

$$|H_{HP}| = \frac{A_{01} \frac{f}{f_L}}{\sqrt{1 + \left(\frac{f}{f_L}\right)^2}} \longrightarrow (1)$$

$$H_{LP} = \left(1 + \frac{R_f}{R_i}\right) \frac{1}{1 + j 2\pi f R_1 C_1}$$

$$H_{LP} = A_{02} \frac{1}{1 + j \frac{f}{f_h}} \quad \text{where} \quad f_h = \frac{1}{2\pi R_1 C_1}$$

$$|H_{LP}| = \frac{A_{02}}{\sqrt{1 + \left(\frac{f}{f_h}\right)^2}} \longrightarrow (2)$$

$$|H_{WBP}| = |H_{HP}| \, |H_{LP}|$$

$$= \frac{A_{01} \frac{f}{f_L}}{\sqrt{1 + \left(\frac{f}{f_L}\right)^2}} \times \frac{A_{02}}{\sqrt{1 + \left(\frac{f}{f_h}\right)^2}}$$

$$|H_{WBP}| = \frac{A_{01} A_{02} \frac{f}{f_L}}{\sqrt{\left[1 + \left(\frac{f}{f_L}\right)^2\right]\left[1 + \left(\frac{f}{f_h}\right)^2\right]}}$$

$$|H_{WBP}| = \frac{A_0 \frac{f}{f_L}}{\sqrt{\left[1 + \left(\frac{f}{f_L}\right)^2\right]\left[1 + \left(\frac{f}{f_h}\right)^2\right]}} \quad \text{where} \quad A_0 = A_{01} A_{02}$$

Problem: Design a wide band pass filter having $f_L = 400\,Hz$, $f_h = 2\,KHz$ and pass band gain of 4

b. Find the value of Q of the filter.

Solution:

Given $f_L = 400\,Hz$

$$f_L = \frac{1}{2\pi R_2 C_2}$$

choose $C_2 = 0.01\,\mu F$

then $R_2 = 39.7\,K\Omega$

Given $f_h = 2\,KHz$

$$f_h = \frac{1}{2\pi R_1 C_1}$$

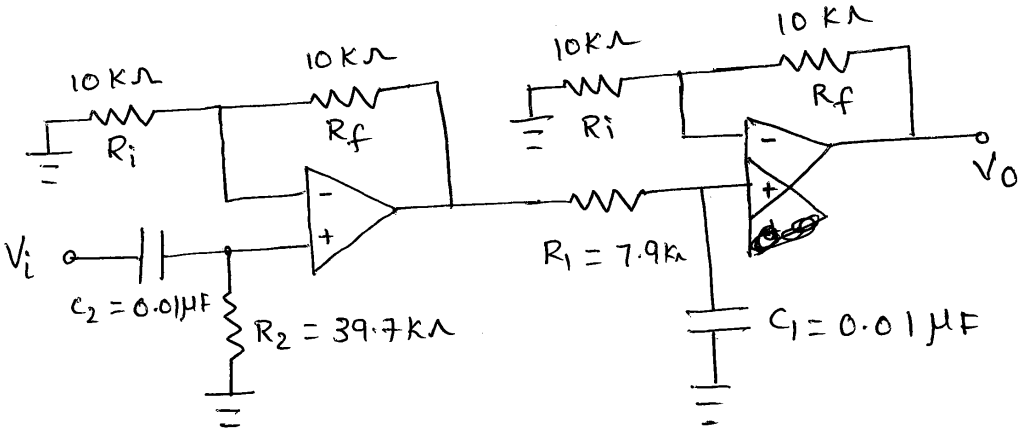
choose $C_1 = 0.01\,\mu F$

then $R_1 = 7.9\,K\Omega$

$$\text{Gain} = 4 = A_{01} \times A_{02} = A_0$$

$$A_0 = \left(1 + \frac{R_f}{R_i}\right)\left(1 + \frac{R_f}{R_i}\right) = 4$$

$$1 + \frac{R_f}{R_i} = 2 \Rightarrow R_f = R_i = 10\,K\Omega.$$



ii) $f_0 = \sqrt{f_h f_L} = 894.42$, $BW = f_h - f_L = 1600$

$$Q = \frac{f_0}{BW} = \frac{894.42}{1600} = 0.56 \quad (< 10)$$

↳ wide band pass filter.

Band Reject Filter:

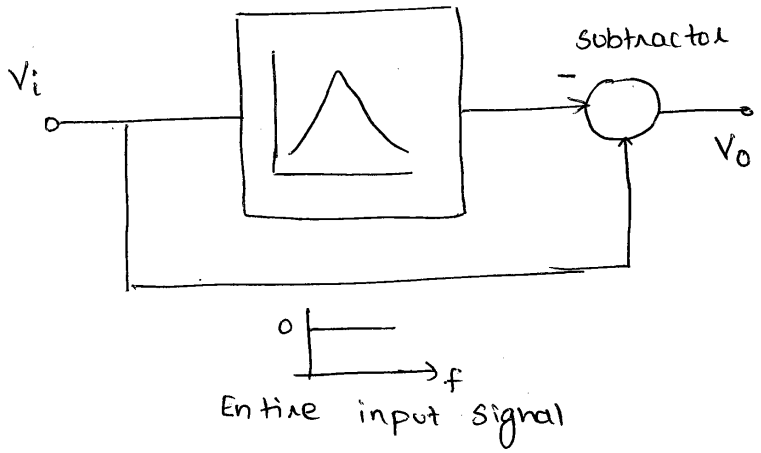
A band reject filter (also called a band stop or band elimination) can be either

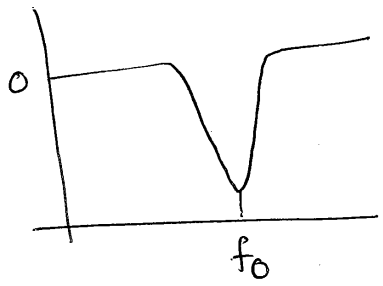
i) Narrow band reject (or)

ii) wide band reject filter.

The narrow band reject filter is commonly called a notch filter and is useful for the rejection of a single frequency, such as 50 Hz power line frequency hum.

There are several ways to make notch filters one simple technique is to subtract the band pass filter output from its input. This principle is shown in figure below.

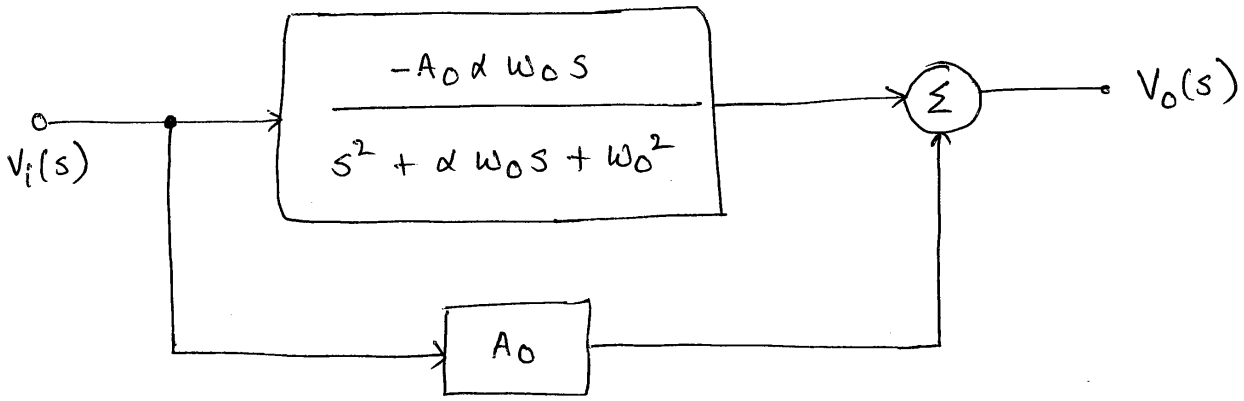




Notch Response.

The band pass filter has an inverted output as the gain is negative. Therefore while implementing the notch filter, we must use a summer

instead of a subtractor. Also the band pass filter has a gain of A_0, so that output at the centre frequency will be $-A_0V_i$. To completely subtract this output, the input of the summer must be precisely A_0V_i. Thus a gain of A_0 must be added between the input signal and the summer as shown in figure below.



the output of the circuit in the s-domain is

$$V_o(s) = A_0 V_i(s) + \left[\frac{-A_0 \alpha \omega_0 s \; V_i(s)}{s^2 + \alpha \omega_0 s + \omega_0^2} \right]$$

$$\frac{V_o(s)}{V_i(s)} = A_0 - \frac{A_0 \alpha \omega_0 s}{s^2 + \alpha \omega_0 s + \omega_0^2}$$

$$\frac{V_o(s)}{V_i(s)} = A_0 \left[1 - \frac{\alpha \omega_0 s}{s^2 + \alpha \omega_0 s + \omega_0^2} \right]$$

$$\frac{V_o(s)}{V_i(s)} = \frac{A_0 \left(s^2 + \omega_0^2 \right)}{s^2 + \alpha \omega_0 s + \omega_0^2} \longrightarrow (1)$$

This is the transfer function for a second order notch filter and the circuit schematic is shown below.

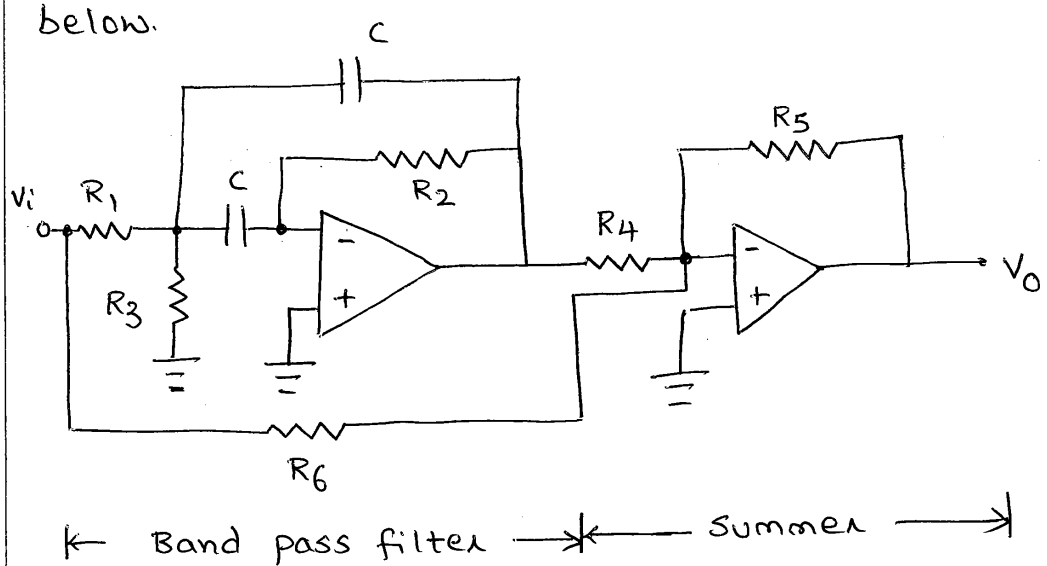


Fig: Notch filter schematic

It is evident from Eq ① that for $\omega << \omega_0$, and for $\omega >> \omega_0$, the pass band gain is $|A_0|$ and at frequency $\omega = \omega_0$ the gain is zero.

Wide Band Reject Filter:-

A wide band reject filter ($Q < 10$) can be made using a LPF, HPF and a Summer.

It is of course necessary that

i) the lower cut-off frequency f_L of the HPF should be much greater than the upper cut-off frequency f_h of the LPF

ii) the pass band gain of LPF and HPF should be the same.

The circuit for wide Band Reject filter is shown in figure below.

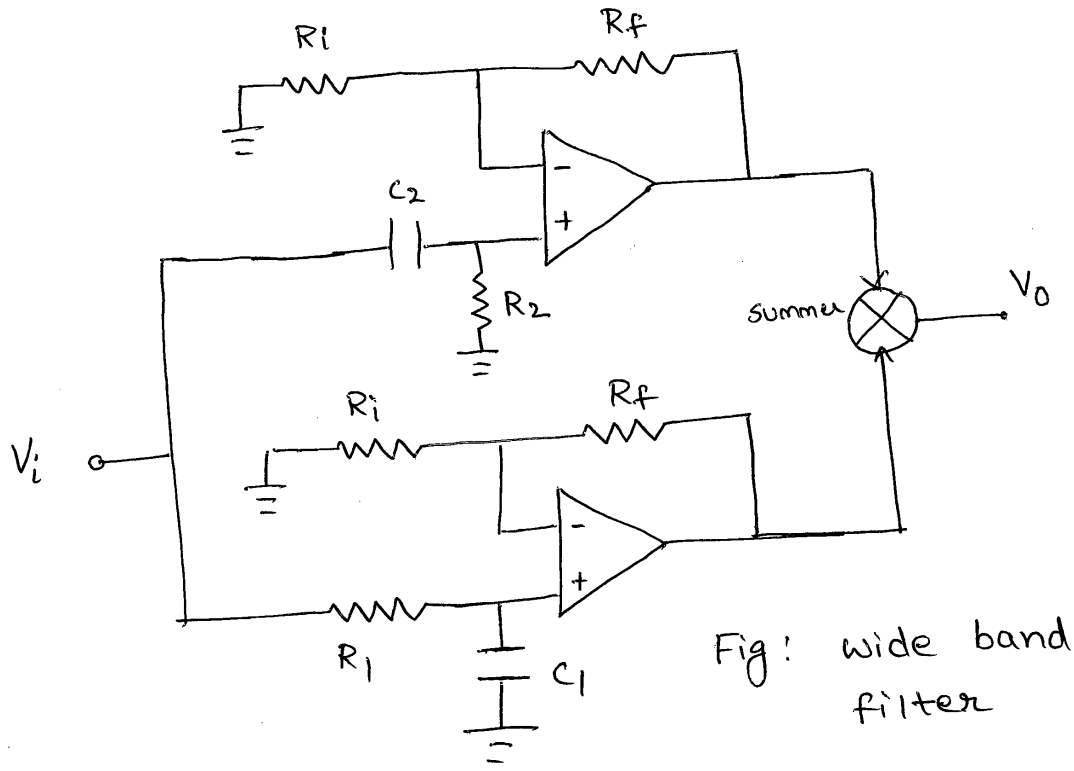


Fig: wide band Reject filter

The frequency response of wide band reject filter is shown in figure below.

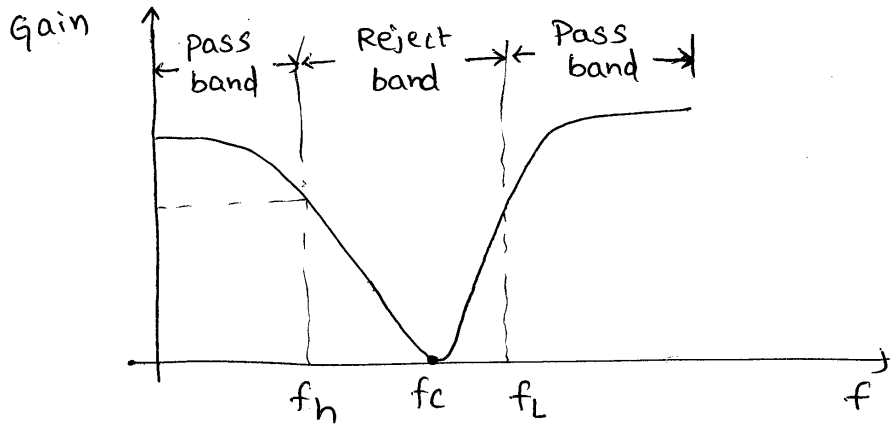
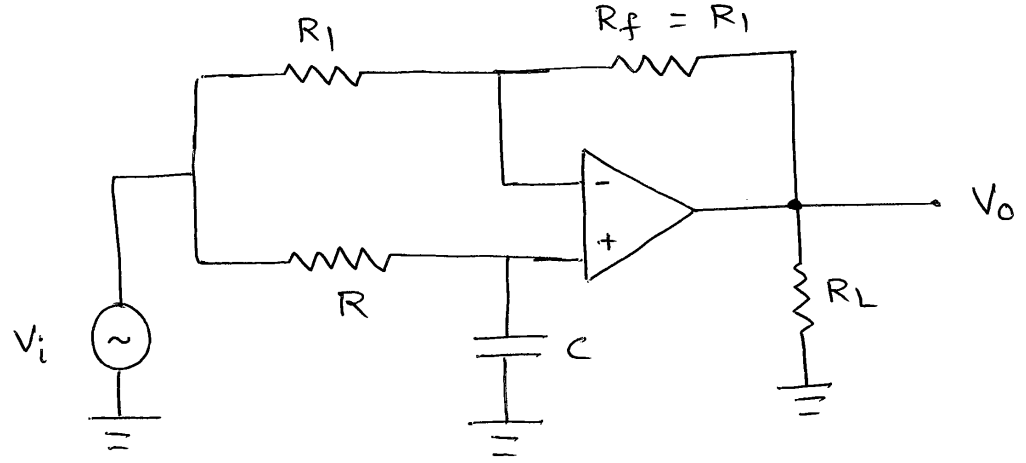


Fig: Frequency response

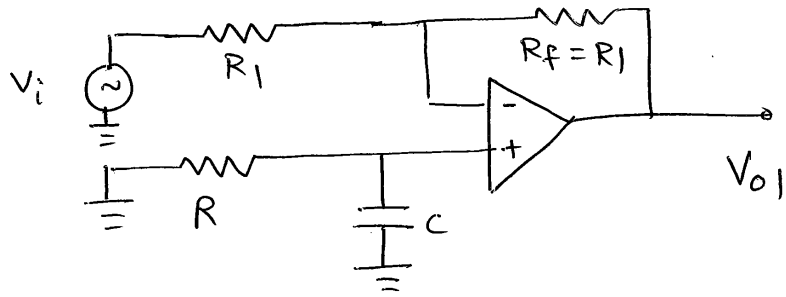
All pass Filter:

An all pass filter passes all frequency components of the input signal without any attenuation.



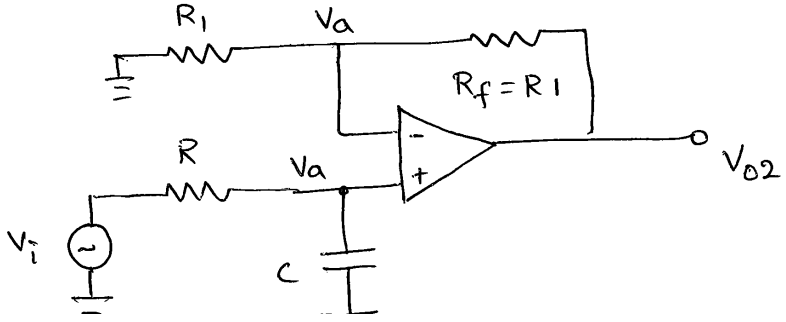
By using superposition principle, the output voltage will be calculated.

case(i): V_i at inverting input.



Here $\frac{V_{o1}}{V_i} = -\frac{R_f}{R_1} = -1 \Rightarrow \boxed{V_{o1} = -V_i} \rightarrow (1)$

case(ii): V_i at non-inverting input



Here $\frac{V_{02}}{V_a} = 1 + \frac{R_f}{R_1} = 2 \Rightarrow V_{02} = 2V_a \rightarrow (2)$

and $\frac{V_i - V_a}{R} = \frac{V_a}{1/sC} \Rightarrow \frac{V_i}{R} = V_a\left[\frac{1}{R} + sC\right]$

$\Rightarrow V_a = V_i\left[\frac{1}{1+sRC}\right] \rightarrow (3)$

By using superposition principle

$$V_o = V_{01} + V_{02}$$

$$V_o = -V_i + 2V_a$$

$$V_o = -V_i + 2\left[V_i\left(\frac{1}{1+sRC}\right)\right] \quad \{\text{from Eq (3)}\}$$

Put $s = j\omega$

$$V_o = -V_i\left[\frac{2}{1+j\omega RC} - 1\right] \Rightarrow \frac{V_o}{V_i} = \frac{1-j\omega RC}{1+j\omega RC} \rightarrow (4)$$

$$\Rightarrow \boxed{\frac{V_o}{V_i} = \frac{1-sRC}{1+sRC}}$$ Transfer function of all pass filter $\rightarrow (5)$

Eq (4) $\Rightarrow \frac{V_o}{V_i} = \frac{1-j2\pi fRC}{1+j2\pi fRC} = H(\omega)$

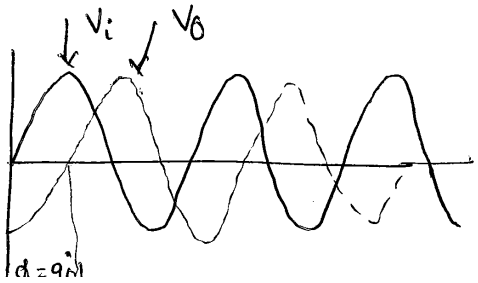
$$\left|\frac{V_o}{V_i}\right| = 1 \Rightarrow |V_o| = |V_i|$$

$$\phi = -\tan^{-1}(2\pi fRC) - \tan^{-1}(2\pi fRC)$$

$$\phi = -2\tan^{-1}(2\pi fRC)$$

If $R = 15.9\ K\Omega$, $C = 0.01\mu F$, $f = 1KHz$

then $\phi = -90^\circ$



555 Timer

Introduction:

In most of the industries, operations are scheduled according to specific time requirements. In process industry, raw material is processed in different stages. In each stage raw material is processed for a particular time period. For example process may be the heating process and the heat may be required for say, 5 minutes. There are number of applications where event must be delayed for specific delay periods. For example, one can snap by setting proper time period in automatic cameras.

To achieve these requirements, an electronic circuitary which is used to generate time delays. the 555 timer is a highly stable device for generating accurate time delay or oscillation.

Features:

* A single 555 timer can provide time delay ranging from microseconds to hours where as counter timer can have a maximum timing range of days.
* the 555 timer can be used with supply voltage in the range of +5V to +18V and can drive

load up to 200mA.

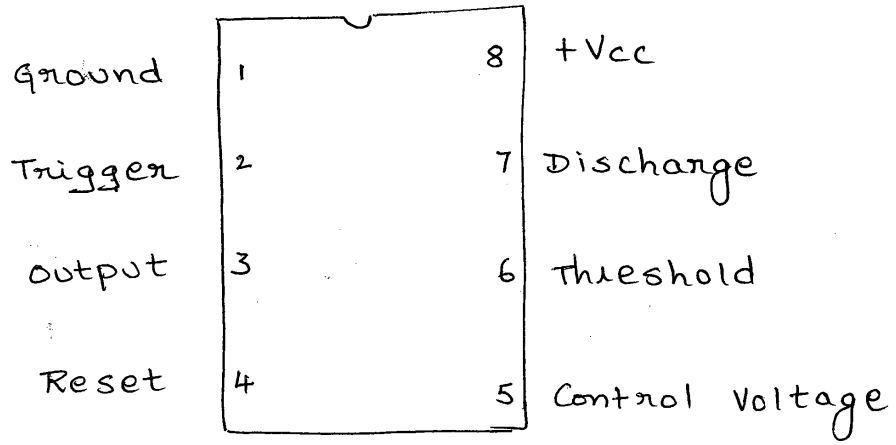
* It is compatible with both TTL and CMOS logic circuits.
* Because of the wide range of supply voltage, the 555 timer is versatile and easy to use in various applications.

Applications:

1. oscillator 2. pulse Generator
3. Ramp and square wave Generator
4. mono shot multivibrator 5. Burglar Alarm
6. Traffic light Control 7. Voltage Monitor.

Functional Block diagram of IC 555:

The figure below shows the pin diagram and the block diagram of the IC NE 555 timer. This is 8 pin IC timer.



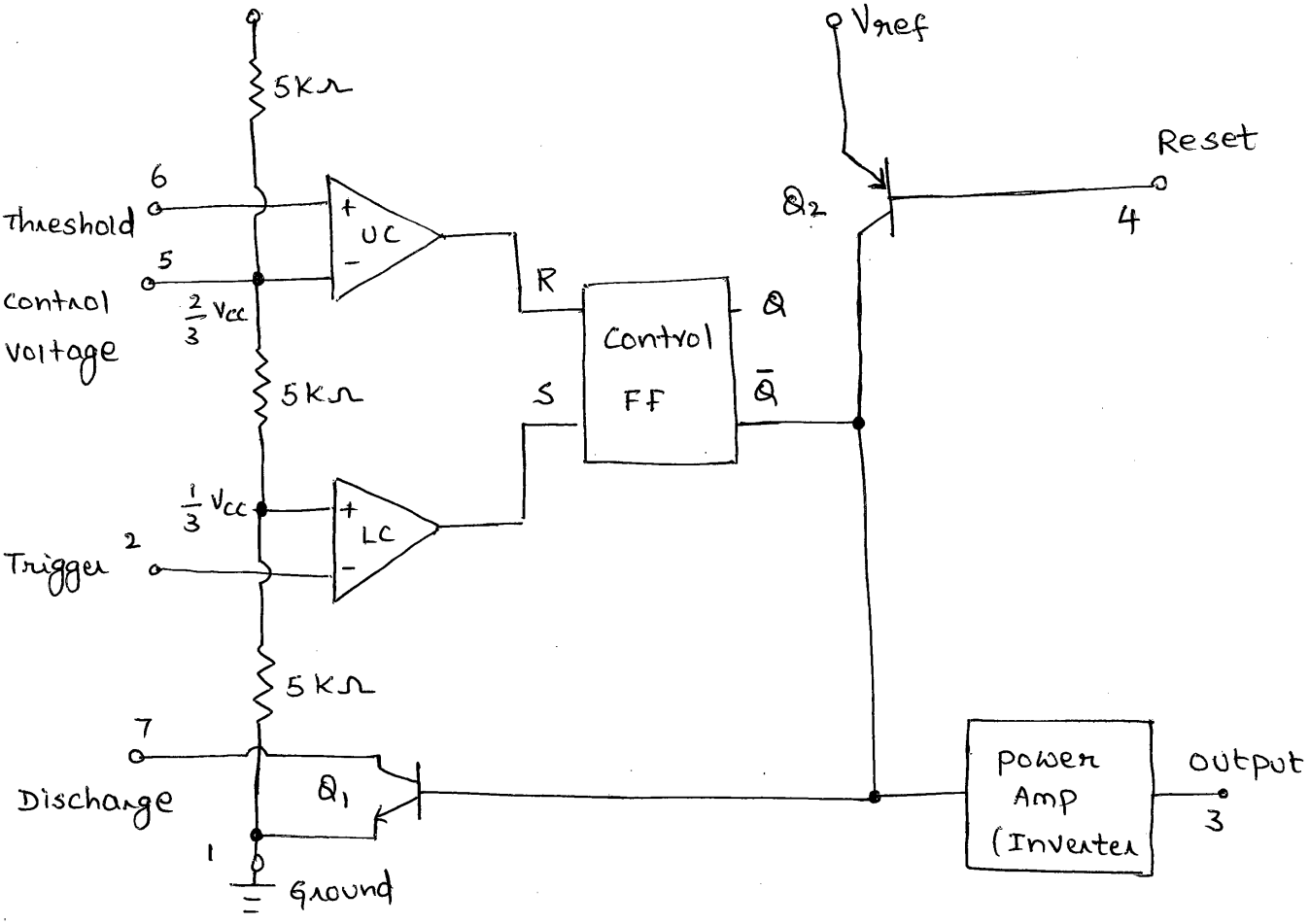


Fig: Functional diagram of 555 timer

Description:

Here three 5 kΩ internal resistors act as voltage divider, providing bias voltage of $\frac{2}{3}V_{cc}$ to the upper comparator and $\frac{1}{3}V_{cc}$ to the lower comparator (LC), where V_{cc} is the supply voltage.

Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval. It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (Pin5)

→ In application where no such modulation is intended, it is recommended that a capacitor (0.01 μF) be connected between control voltage terminal (Pin 5) and ground to bypass noise or ripple from the supply.

→ In the standby (stable) state, the output $\bar{Q}$ of the control flip-flop is high. This makes the output low because of power amplifier which is basically an inverter.

→ A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator (ie $\frac{V_{cc}}{3}$)

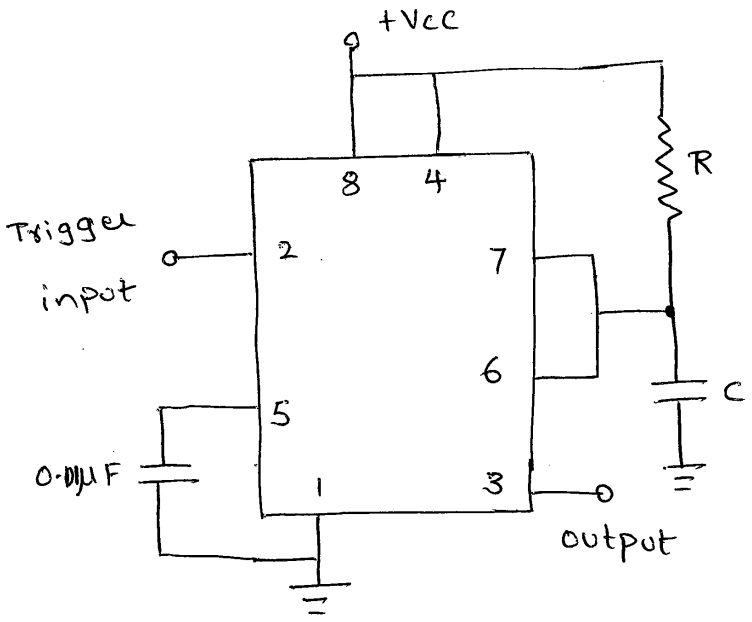
→ At the negative going edge of the trigger, as the trigger passes through $\frac{V_{cc}}{3}$, the output of the lower comparator goes High and sets the flip flop ($Q = 1$, $\bar{Q} = 0$)

→ During the positive excursion, when the threshold voltage at pin 6 passes through $\frac{2}{3} V_{cc}$, the output of the upper comparator goes High and resets the FF ($Q = 0$, $\bar{Q} = 1$)

→ The reset input (Pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator

→ The transistor Q_2 serves as a buffer to isolate the reset input from the FF and the transistor Q_1.

Monostable operation:



Fig(a): Monostable Multivibrator.

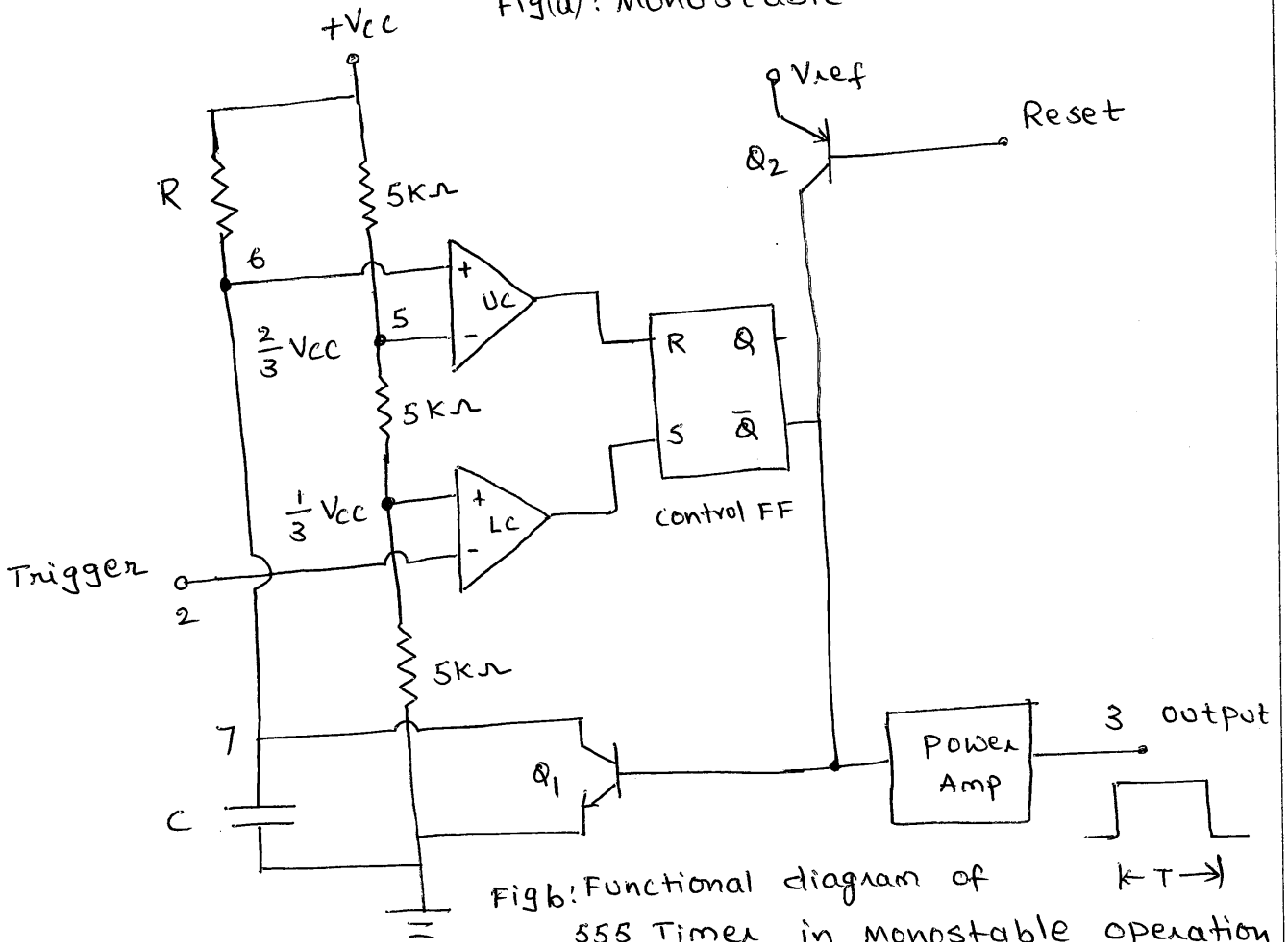


Fig b: Functional diagram of 555 Timer in monostable operation

→ Figure (a) shows a 555 timer connected for monostable operation and its functional diagram is shown in fig(b).

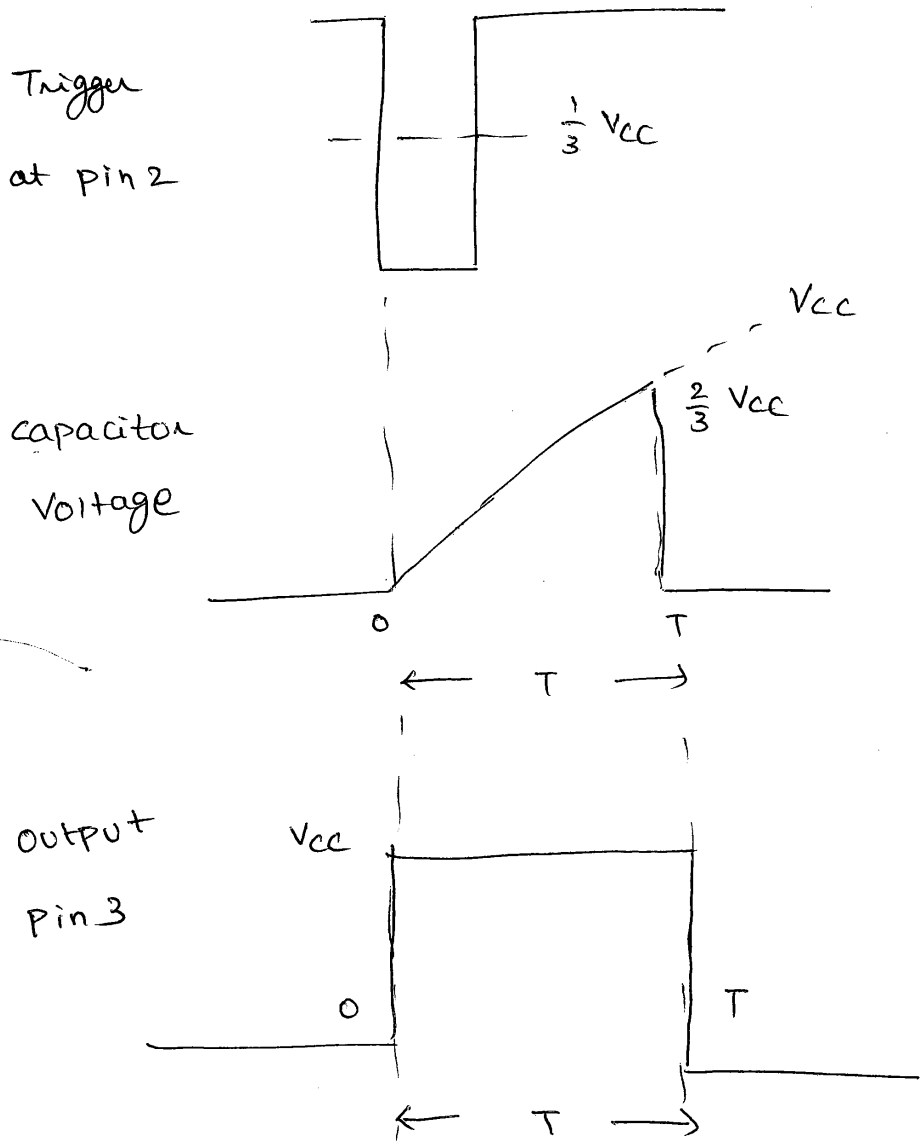
In the stand by mode FF holds the transistor Q_1 on, thus clamping the external timing capacitor C to ground. The output remains at ground potential ie low.

As the trigger passes through $\frac{V_{cc}}{3}$, the FF is set ie $\bar{Q} = 0$. This makes the transistor Q_1 off and the short circuit across the timing capacitor C is released.

As $\bar{Q}$ is low, output goes High $(=V_{cc})$. Now timing cycle begins. Voltage across the capacitor rises exponentially through R towards V_{cc} with a time constant RC.

After a time period (T) the capacitor voltage is just greater than $\frac{2}{3} V_{cc}$ and the upper comparator resets the FF, that is R=1, S=0. This makes $\bar{Q} = 1$, transistor Q_1 goes on (ie saturates), thereby discharging the capacitor C rapidly to ground potential. Then the output returns to the standby mode (or) ground potential as shown in fig(c).

wave forms :



Derivation of Pulse width :

The voltage across capacitor increases exponentially and is given by

$$V_c = V_f - (V_f - V_{ini})\, e^{-t/RC}$$

Here $V_{ini} = 0$, $V_f = V_{CC}$

$$\therefore \quad V_c = V_{cc}\left(1 - e^{-t/RC}\right)$$

At $t = T$, $V_c = \frac{2}{3}V_{cc}$

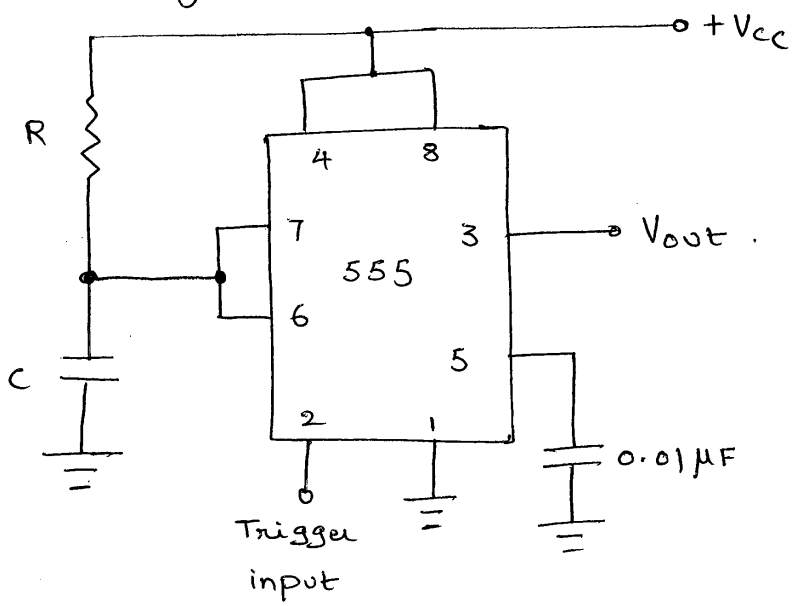
$$\therefore \quad \frac{2}{3}V_{cc} = V_{cc}\left[1 - e^{-T/RC}\right]$$

$$\therefore \quad T = 1.1\,RC$$

Thus the pulse width T is given by

$$\boxed{T = 1.1\,RC}$$

Schematic Diagram:



Applications of IC 555 timer in Monostable Mode:

1. Frequency Divider:

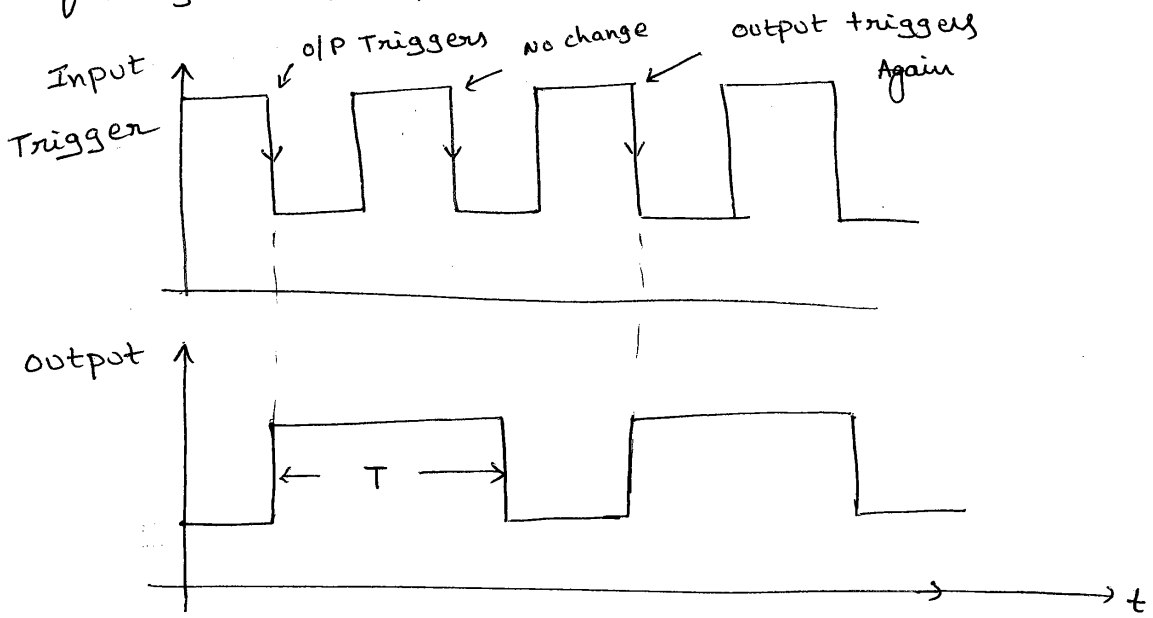


Fig: Frequency divider circuit.

A continuosly triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal. The monostable multivibrator will be

triggered by the first negative going edge of the square wave input signal. but the output will remain high for next negative going edge of the input square wave as shown in figure above. The monoshot will however be triggered on the third negative going input depending on the choice of time delay. In this way the output can be made integral fractions of the frequency of the input triggering square wave.

2. Missing pulse detector:

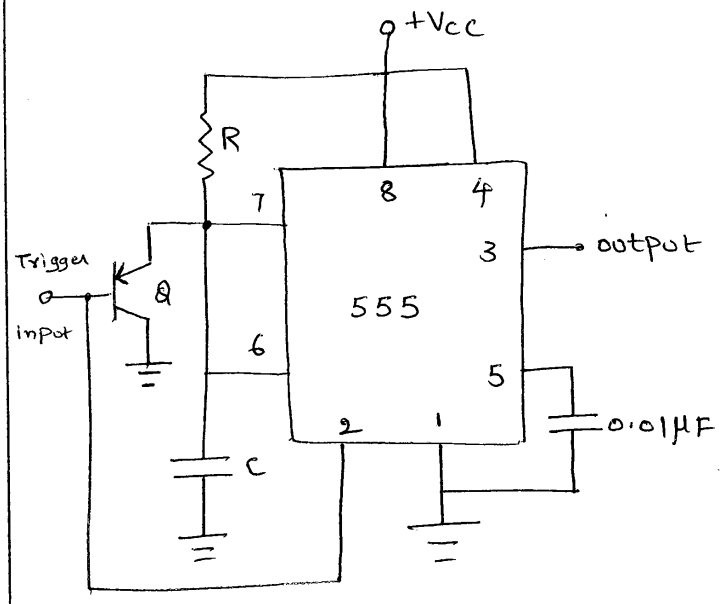


Fig: A missing pulse detector monostable circuit.

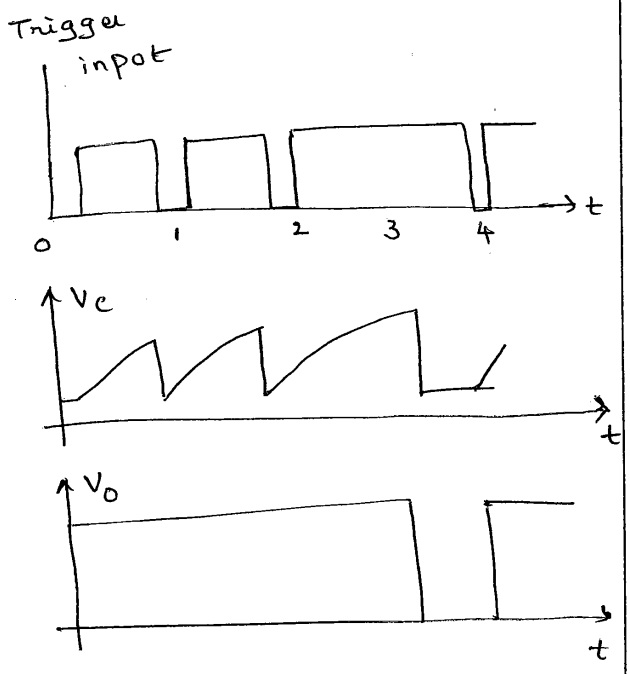


Fig: Output of Missing pulse detector.

Missing pulse detector circuit using 555 timer is shown in figure above. whenever, input trigger is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (~0.7V). The output of the timer goes high. The circuit is designed so that the time period

of the monostable circuit is slightly greater ($\frac{1}{3}$ longer) than that of the triggering pulses. So long the trigger pulse train keeps coming at pin 2, the output remains High. However, if a pulse misses, the trigger input is high and transistor Q is cut-off. The 555 timer enters in to normal state of monostable operation.

The output goes low after time T of the mono shot. Thus this type of circuit can be used to detect missing heart beat. It can also be used for speed control and measurement.

3. Linear Ramp Generator :

Linear ramp can be generated by the circuit shown in figure. The resistor R of the monostable circuit is replaced by a constant current source.

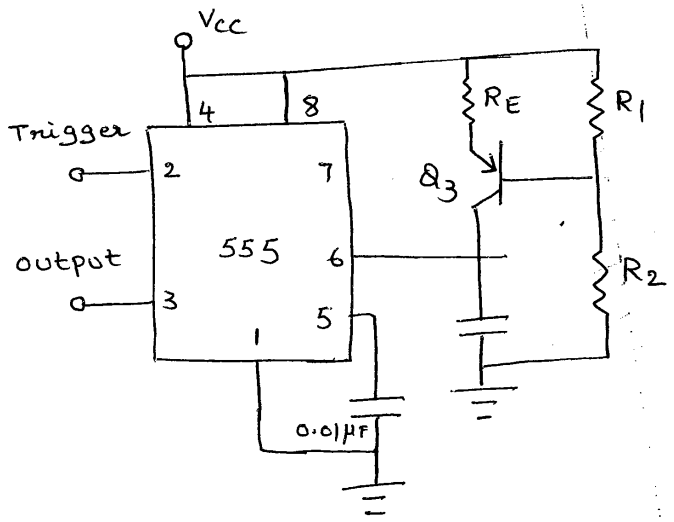


Fig: Linear Ramp Generator.

The capacitor is charged linearly by the constant current source formed by the transistor Q_3. The capacitor voltage V_c can be written as

$$V_c = \frac{1}{C}\int_0^t i\,dt \longrightarrow (1)$$

where i is the current supplied by the constant current source. Further the KVL equation can be written as

$$\frac{R_1}{R_1+R_2} V_{CC} - V_{BE} = (\beta+1) I_B R_E \simeq \beta I_B R_E = I_C R_E = i R_E \longrightarrow (2)$$

where I_B, I_C are the base current and collector current respectively, β is the current amplification factor in CE-mode and is very high. therefore.

$$i = \frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{R_E (R_1+R_2)} \longrightarrow (3)$$

Now putting the value of the current i in eq (1), we get

$$V_C = \frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{C R_E (R_1+R_2)} t$$

At time $t = T$, the capacitor voltage V_C becomes $\frac{2}{3} V_{CC}$, then we get

$$\frac{2}{3} V_{CC} = \frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{R_E (R_1+R_2) C} \times T$$

$$\text{Now} \quad T = \frac{\left(\frac{2}{3}\right) V_{CC} R_E (R_1+R_2) C}{R_1 V_{CC} - V_{BE}(R_1+R_2)} \longrightarrow (4)$$

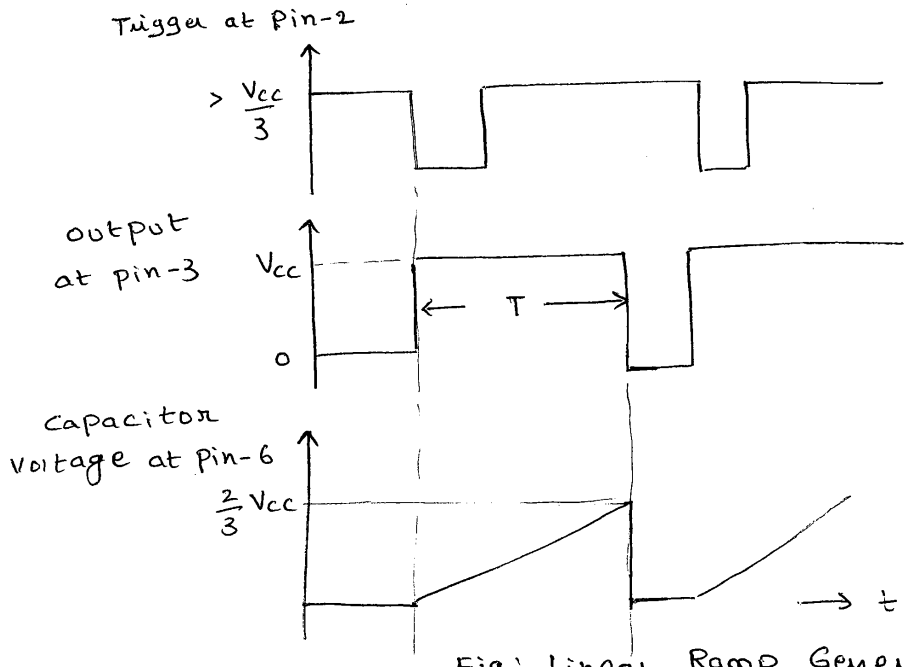
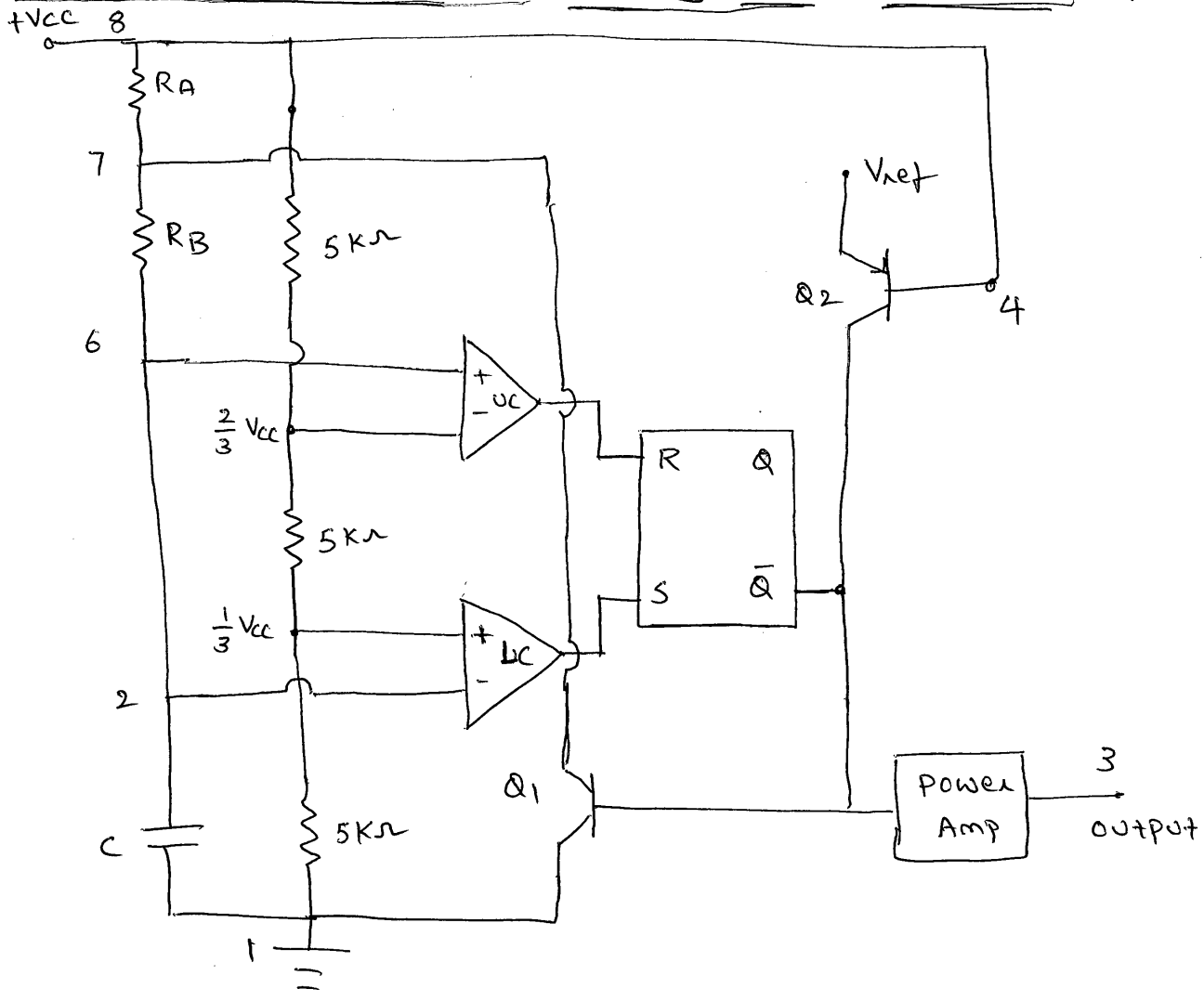


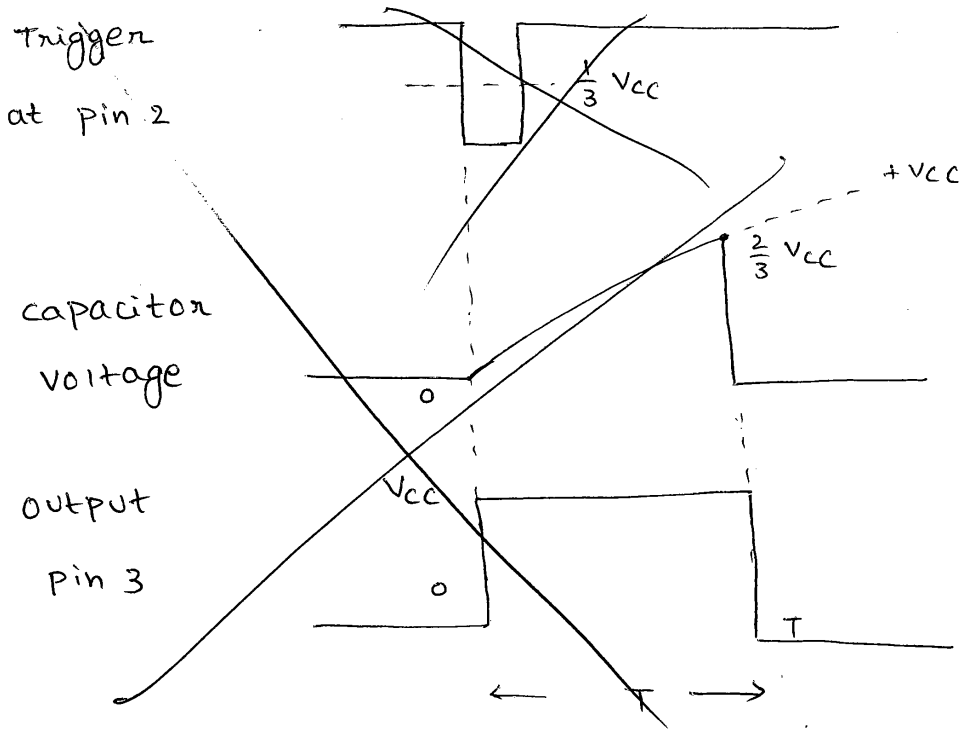
Fig: Linear Ramp Generator output.

The capacitor discharges as soon as its voltage reaches $\frac{2}{3}V_{cc}$ which is the threshold of the upper Comparator in the monostable circuit functional diagram. The capacitor voltage remains zero till another trigger is applied. The wave forms are shown in figure above.

Astable Multivibrator using IC 555 Timer:



when the power supply V_{cc} is connected, the external timing capacitor C charges towards V_{cc} with a time constant $(R_A + R_B)C$



Derivation of Pulse width

The voltage across capacitor increases exponentially an is given by

$$V_c = V_f - (V_f - V_{ini})\, e^{-t/RC}$$

Here $V_{ini} = 0$, $V_f = V_{CC}$

$$\therefore V_c = V_{CC}\left(1 - e^{-t/RC}\right)$$

At $t = T$, $V_c = \frac{2}{3} V_{CC}$

$$\therefore \frac{2}{3} V_{CC} = V_{CC}\left(1 - e^{-T/RC}\right)$$

$$\therefore T = 1.1\, RC$$

Thus the pulse width T is given by

$$\boxed{T = 1.1\, RC}$$

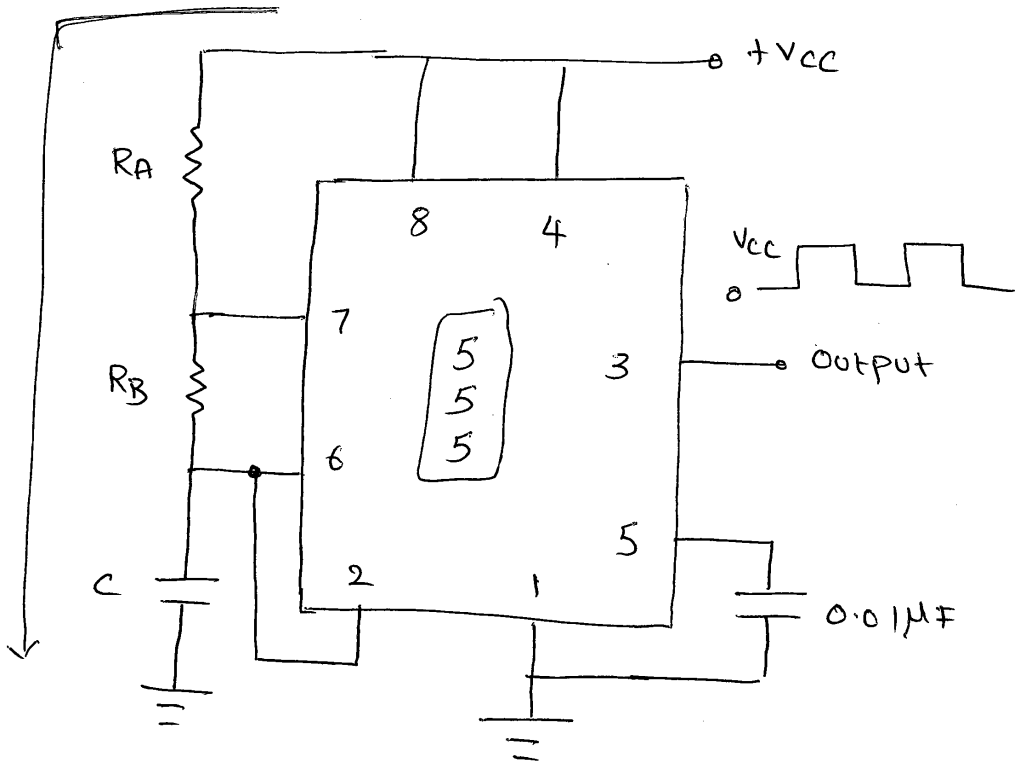
During this time output (Pin 3) is high (equals V_{cc}) as Reset $R=0$, set $S=1$, and this combination makes $\bar{Q}=0$ which has unclamped the timing capacitor C.

when the capacitor voltage equals to $\frac{2}{3}V_{cc}$, the upper comparator triggers the control FF so that $\bar{Q}=1$. This inturn makes transistor Q_1 on and capacitor C starts discharging towards ground through R_B and transistor Q_1 with a time constant R_BC.

During the discharge of timing capacitor C, as it reaches $\frac{V_{cc}}{3}$, the lower comparator is triggered and at this stage $S=1$, $R=0$, which turns $\bar{Q}=0$. Now $\bar{Q}=0$ unclamps the external timing capacitor C.

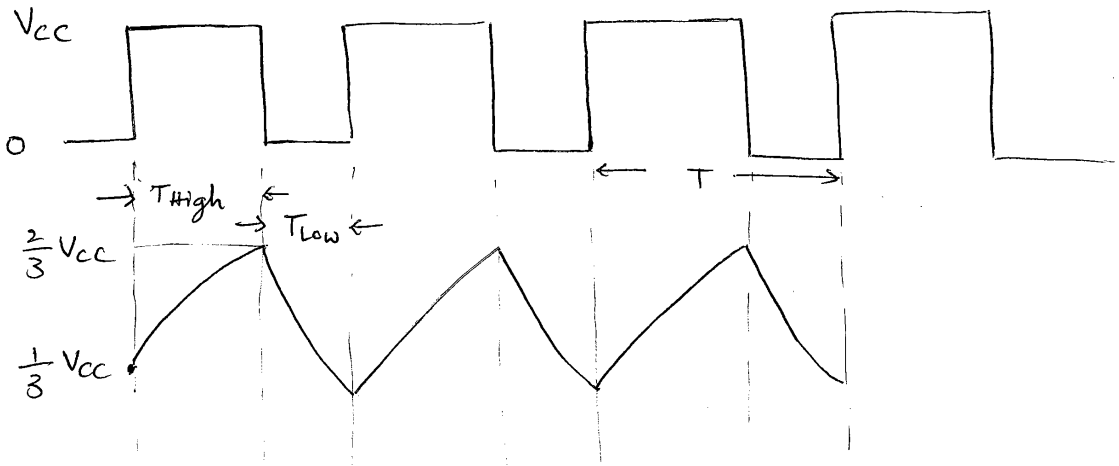
The capacitor C is thus periodically charged and discharged between $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$ respectively.

The schematic diagram of Astable multivibrator using IC 555 timer is shown in figure below

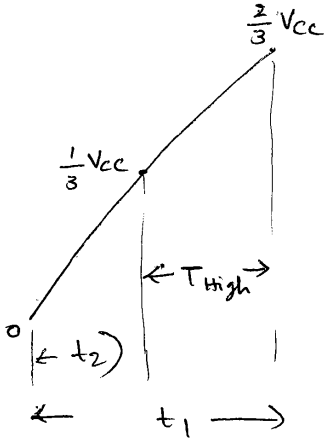


~~the~~ ~~timing~~

~~rising~~ ~~and~~ ~~falling~~. the waveforms are shown in figure below.



the time t_1 taken by the circuit to change from 0 to $\frac{2}{3}V_{cc}$ is



$$V_c = V_f - (V_f - V_{ini})\, e^{-t/RC}$$

$V_f = V_{cc}$, $V_{ini} = 0$

$$V_c = V_{cc} - (V_{cc} - 0)\, e^{-t/RC}$$

$$V_c = V_{cc}\left(1 - e^{-t/RC}\right)$$

when $t = t_1$, $V_c = \frac{2}{3}V_{cc}$

$$\frac{2}{3}V_{cc} = V_{cc}\left(1 - e^{-t_1/RC}\right)$$

$$t_1 = 1.09\,RC$$

Ily when $t = t_2$, $V_c = \frac{1}{3}V_{cc}$

$$\frac{1}{3}V_{cc} = V_{cc}\left(1 - e^{-t_2/RC}\right)$$

$$t_2 = 0.405\,RC$$

$$\therefore \quad T_{High} = t_1 - t_2 = 1.09\,RC - 0.405\,RC$$

$$T_{High} = 0.69\,RC = 0.69(R_A + R_B)C \rightarrow (1)$$

the output is low while the capacitor discharges from $\frac{2}{3} V_{cc}$ to $\frac{1}{3} V_{cc}$ and the voltage across the capacitor is given by

$$V_c = V_f - (V_f - V_{ini})\, e^{-t/RC}$$

$V_{ini} = \frac{2}{3} V_{cc}$, $V_f = 0$

$$V_c = 0 - \left(0 - \frac{2}{3} V_{cc}\right) e^{-t/RC}$$

At $t = T_{low}$ $V_c = \frac{1}{3} V_{cc}$

$$\frac{1}{3} V_{cc} = \frac{2}{3} V_{cc}\, e^{-T_{low}/RC}$$

$$T_{low} = 0.69\, RC = 0.69\, R_B C$$

$$T = T_{High} + T_{low}$$

$$T = 0.69 (R_A + 2R_B) C$$

$$f = \frac{1}{T} = \frac{1.45}{0.69 (R_A + 2R_B) C}$$

In the circuit, when the transistor Q_1 is ON, the output goes low. Hence

$$\% \text{ Duty cycle} = \frac{T_{low}}{T} \times 100$$

$$\% \text{ Duty cycle} = \frac{R_B}{R_A + 2R_B} \times 100$$

$$\% D = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100$$

Applications of ~~As~~ 555 timer in Astable Mode

1) FSK Generator:

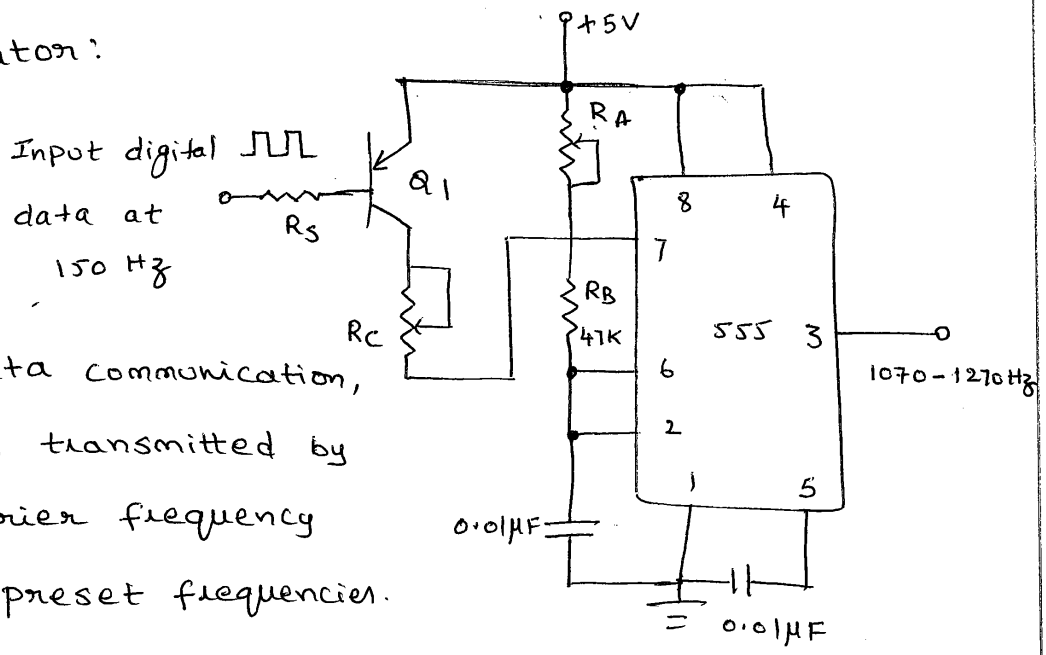


Fig: FSK Generator

In digital data communication, binary code is transmitted by shifting a carrier frequency between two preset frequencies. This type of transmission is called frequency shift keying (FSK) technique.

A 555 timer in astable mode can be used to generate FSK signal. The circuit is shown in figure above. The standard digital data input frequency is 150Hz. when input is high, transistor Q is off and 555 timer works in the normal astable mode of operation. The frequency of the output wave form is given by

$$f_0 = \frac{1.45}{(R_A + 2R_B)C}$$

In a tele-type writer using a modulator-demodulator (MODEM), a frequency between 1070Hz to 1270 Hz is used as one of the standard FSK signals. the components R_A, R_B and the capacitor C can be selected so that f_0 is 1070 Hz

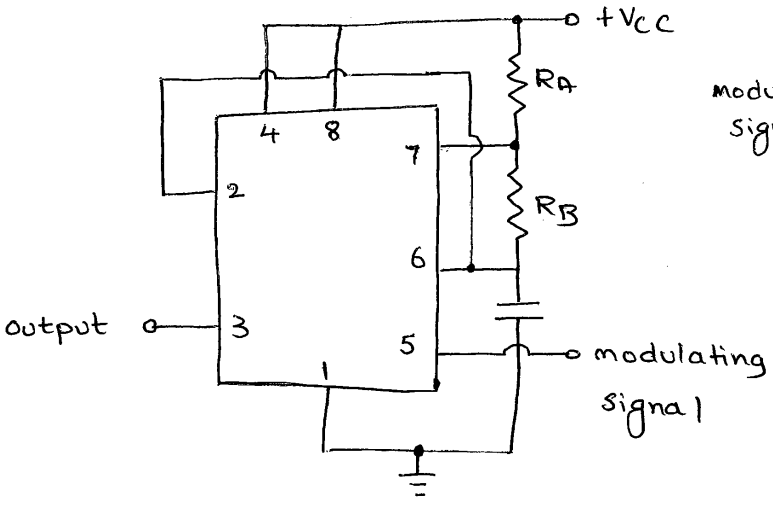
when the input is low, Q goes on and connects the resistance R_C across R_A. The output frequency is now given by

$$f_o = \frac{1.45}{(R_A || R_C) + 2R_B}$$

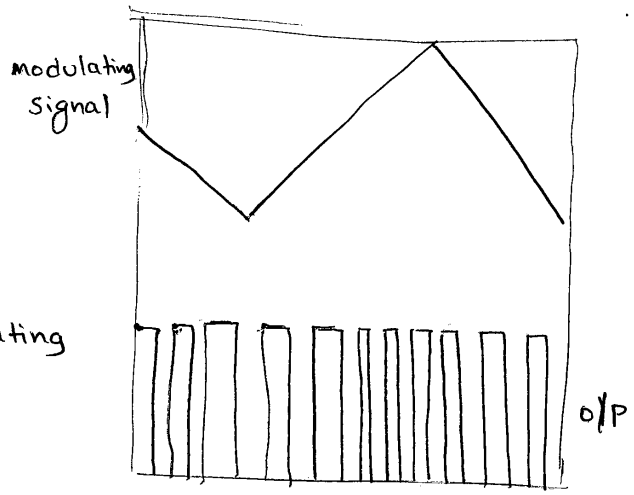
The resistance R_C can be adjusted to get an output frequency 1270 Hz.

d) Pulse position Modulator:

The pulse position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation as shown in figure below. The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.



Fig(a) pulse position modulator



Fig(b): pulse position modulator output

Fig(b) shows the output waveform generated for a triangular wave modulation signal. It may be noted that from the output waveform that the frequency is varying leading

Schmitt trigger using 555 timer:

The use of 555 timer as a schmitt trigger is shown in fig. Here the two internal comparators are tied together and externally biased at $\frac{V_{cc}}{2}$ through R_1 and R_2.

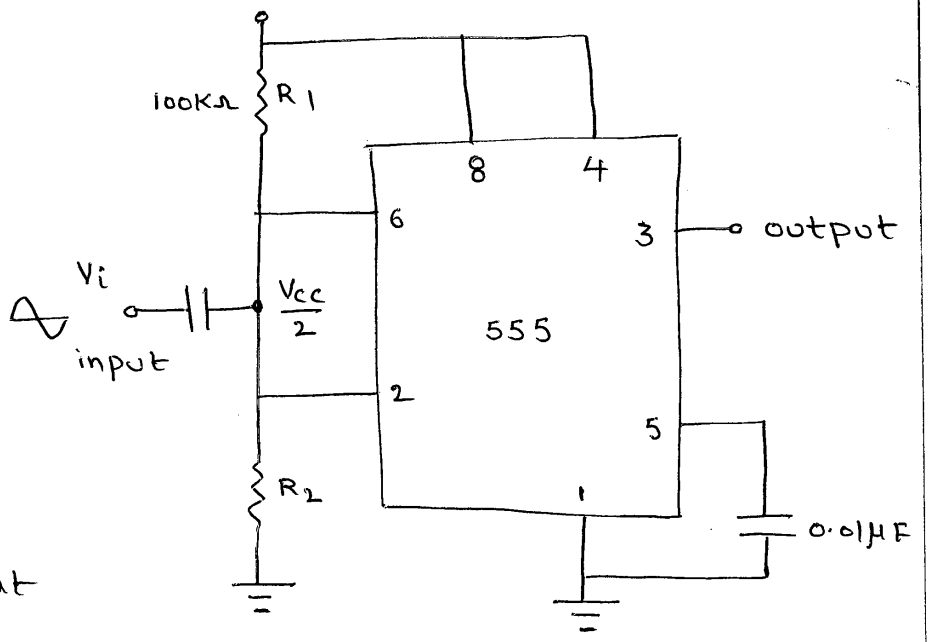
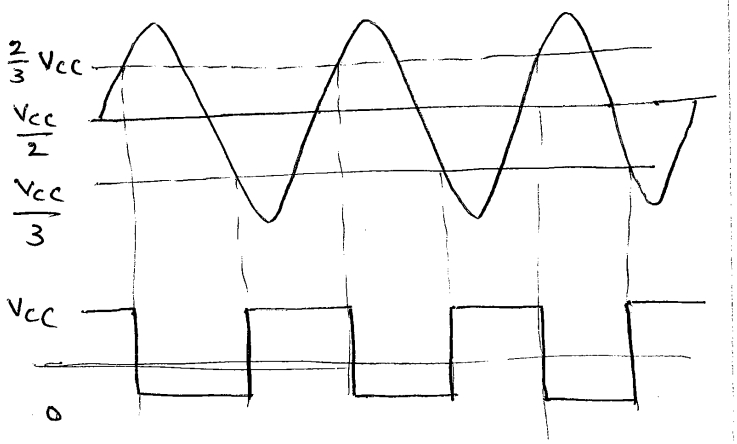


Fig: Timer in schmitt trigger operation.

Since the upper comparator will trip at $\frac{2}{3}V_{cc}$ and lower comparator at $\frac{1}{3}V_{cc}$, the bias provided by R_1 and R_2 is centered with in these two thresholds.

Thus a sine wave of sufficient amplitude $> \frac{V_{cc}}{6}$ $\left(\text{ie } \frac{2}{3}V_{cc} - \frac{V_{cc}}{2}\right)$ to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave output as shown in figure (b).



(Fig b): Input and output waveforms of schmitt trigger.

phase - Locked Loops

Introduction: A phase locked loop is basically a closed loop system designed to lock the output frequency and phase to the frequency and phase of an input signal. It is commonly abbreviated as PLL. Now with the advanced Ic technology, PLL's are available as inexpensive monolithic Ic's. They are used in applications such as frequency synthesis, frequency modulation/ demodulation, AM detection, tracking filters, FSK demodulator, tone detector etc.

Basic principle and operation of PLL:

The basic block schematic of the PLL is shown in figure below.

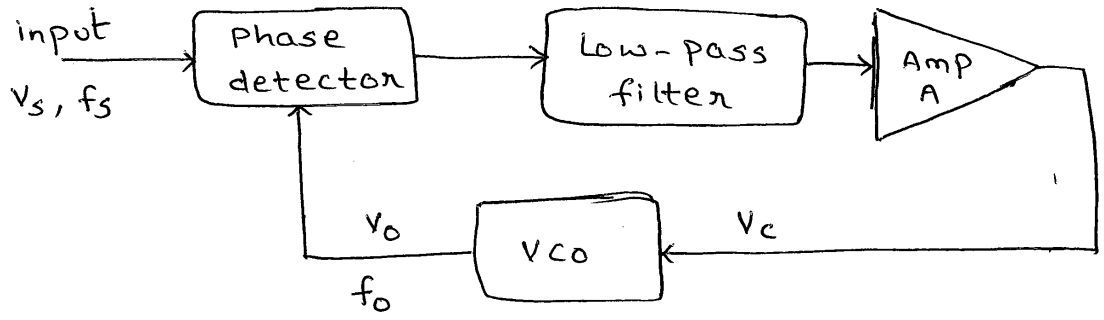


Fig: Block schematic of PLL

This feedback system consists of

1. phase detector/ comparator
2. Low pass filter
3. An Error Amplifier
4. A [illegible] (VCO)

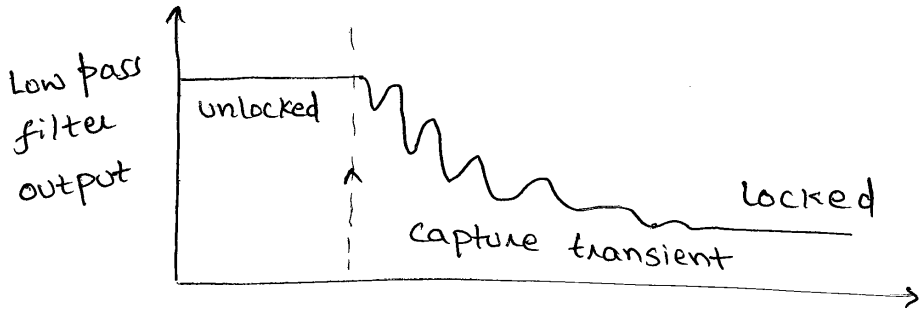
The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency (f_o). This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage V_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called voltage Controlled oscillator or in short VCO.

If an input signal V_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output V_o of the VCO.

If the two signals differ in frequency/phase, an error voltage V_e is generated. The phase detector is basically a multiplier and produces the sum $f_s + f_o$ and difference $f_s - f_o$ components at its output. The high frequency component $f_s + f_o$ is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage V_c to VCO. The signal V_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. Once this action starts, we say that the signal is in the capture range.

The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. the circuit is then said to be locked. once locked, the output frequency f_0 of VCO is identical to f_s except for a finite phase difference ϕ. this phase difference ϕ generates a corrective control voltage V_c to shift the VCO frequency from f_0 to f_s and thereby maintain the lock. once locked, PLL tracks the frequency changes of the input signal. thus, a PLL goes through three stages.
i) free running ii) capture and iii) locked or tracking.

Figure below shows the capture transient.



the capture transient

As capture starts, a small sine wave appears. this is due to the difference frequency between the VCO and the input signal. the dc component of the beat drives the VCO towards lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency.

the difference in frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further. the process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat (f_{diff}) frequency will be too high to pass through the filter and the PLL will not respond. we can say that the signal is out of the capture band.

However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus lock range is always larger than the capture range.

Some important definitions related to PLL.

1) Lock-in range: once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range.

The lock range is usually expressed as a percentage of f_0.

Capture Range: The range of frequencies over which PLL can acquire lock with an input signal is called the capture range. this parameter is also expressed as percentage of fo.

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the over all loop gain and loop filter characteristics.

PHASE DETECTOR

The phase detection is the most important part of the PLL system. There are two types of phase detectors used ① Analog ② Digital.

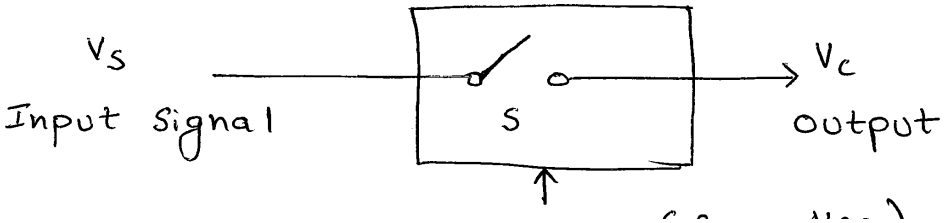
1) Analog phase detector

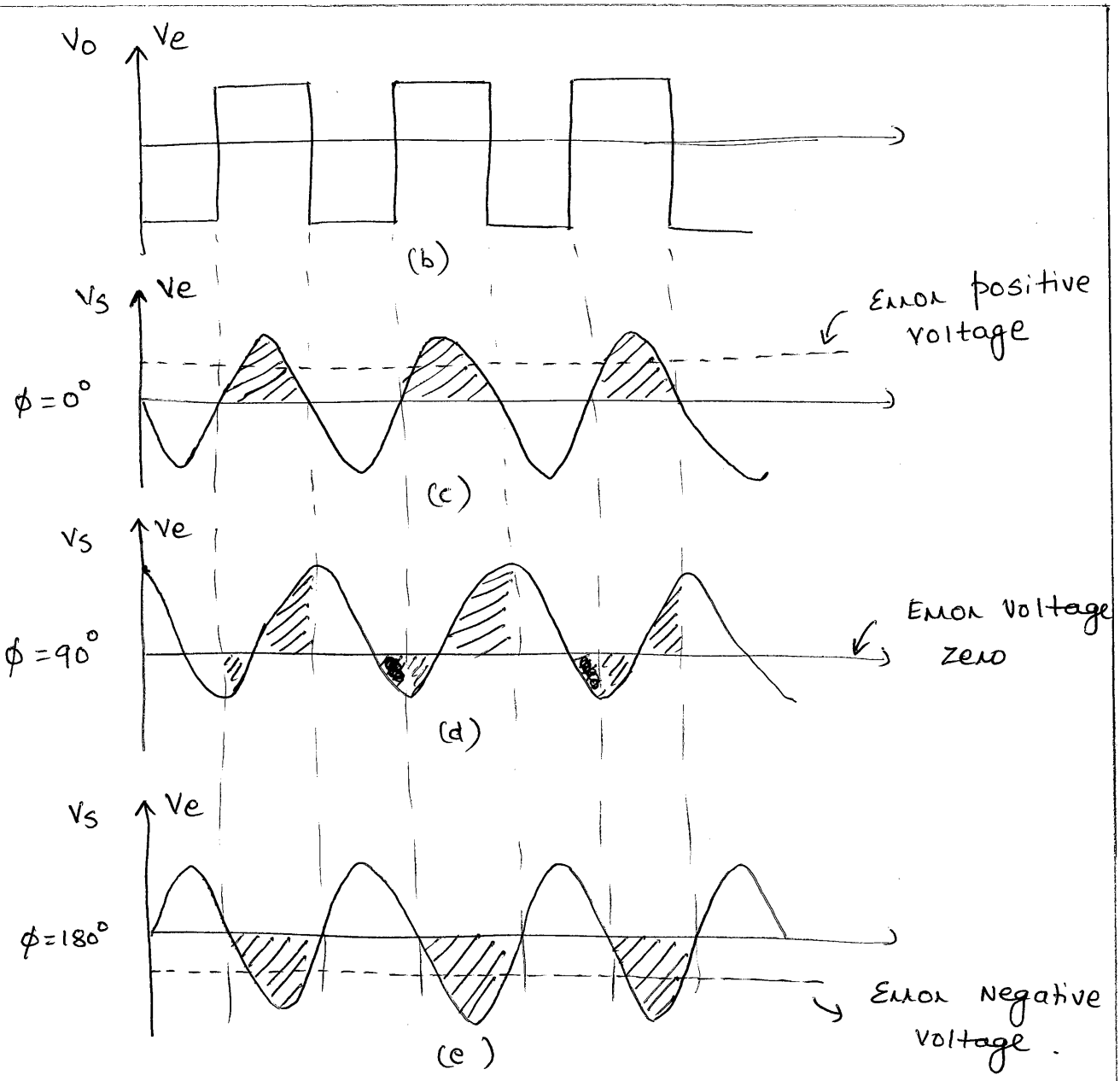
   a) Analog phase detector using electronic switch

   b) Analog phase detector using balanced modulator

a) Analog phase detector using Electronic switch:

The principle of analog phase detection using switch type phase detector is shown in figure below.





(b) VCO output wave form.

Input and output (Hatched) wave form of phase detector for (c) $\phi = 0$ (d) $\phi = 90^\circ$ (e) $\phi = 180^\circ$.

An electronic switch S is opened and closed by signal coming from VCO (normally a square wave) the input signal is therefore chopped at a repetition rate determined by VCO frequency.

Figure (e) shows the input signal Vs assumed to be in phase ($\phi = 0^\circ$) with VCO output Vo.

Since the switch S is closed only when VCO output is positive, the output wave form V_e will be half sinusoids. similarly, the output wave form for $\phi = 90^\circ$ and $\phi = 180^\circ$ is shown in fig (d) and fig(e).

This type of phase detector is called a Half wave detector, since the phase information for only one half of the input wave form is detected and averaged.

The output of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output wave form shown by a dotted line.

It may be seen that error voltage is zero when the phase shift between the two inputs is 90°. so for perfect lock, the VCO output should be 90° out of phase with respect to the input signal.

Analysis:

A phase comparator is basically a multiplier which multiplies the input signal by the VCO signal

$$V_s = V_s \sin 2\pi f_s t \quad , \quad V_o = V_o \sin (2\pi f_o t + \phi)$$

Then the phase comparator output is

$$V_e = K V_s V_o \sin 2\pi f_s t \sin (2\pi f_o t + \phi) \longrightarrow (1)$$

where K → phase comparator gain

and ϕ is the phase shift between the input signal and the VCO output. Eq ① can be simplified as

$$V_e = \frac{K V_s V_o}{2}\left[\cos\left(2\pi f_s t - 2\pi f_o t - \phi\right) - \cos\left(2\pi f_s t + 2\pi f_o t + \phi\right)\right]$$

when at lock ie. $f_s = f_o$

$$\text{then } V_e = \frac{K V_s V_o}{2}\left[\cos(-\phi) - \cos\left(2\pi \times 2 f_o t + \phi\right)\right]$$

This shows that the phase comparator output contains a double frequency term and a dc term $(K V_s V_o/2)\cos\phi$ which varies as a function of phase ϕ, ie. $\cos\phi$ between the two signals.

The double frequency term is eliminated by the low pass filter and the dc signal is applied to the modulating input terminal of a VCO. It can be seen that in the perfect locked state ($f_s = f_o$), the phase shift should be 90° ($\cos 90^\circ = 0$), in order to get zero error signal, that is $V_e = 0$

There are two problems associated with the switch type phase detector.

1. The output voltage V_e is proportional to the input signal amplitude V_s. This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude
2. The output is proportional to $\cos\phi$ and not proportional to ϕ making it non-linear.

Both these problems can be eliminated by limiting the amplitude of the input signal, that is converting the input to a constant amplitude square wave. A circuit which performs phase comparison with square wave input is called Balanced modulator.

Analog phase detector using Balanced modulator:

Balanced modulator is used as full-wave switching phase detector. Here the input signals is applied to the differential pair $Q_1 Q_2$.

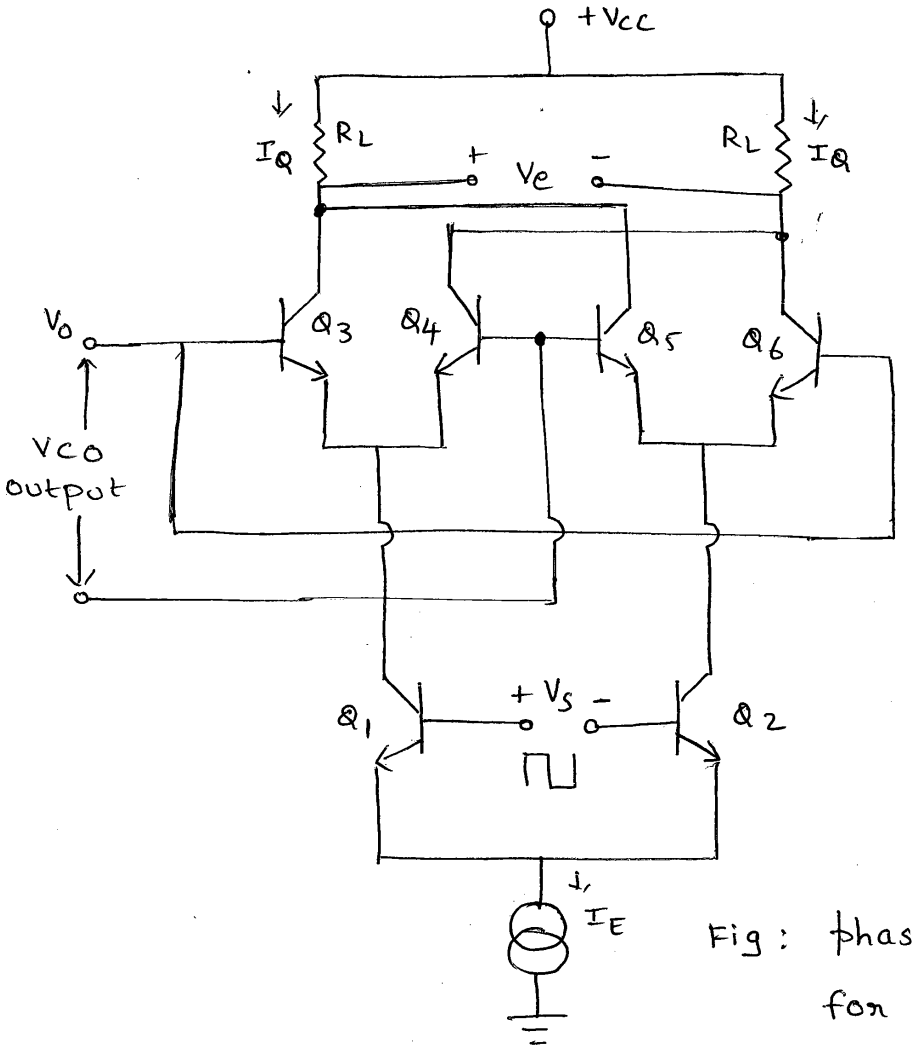
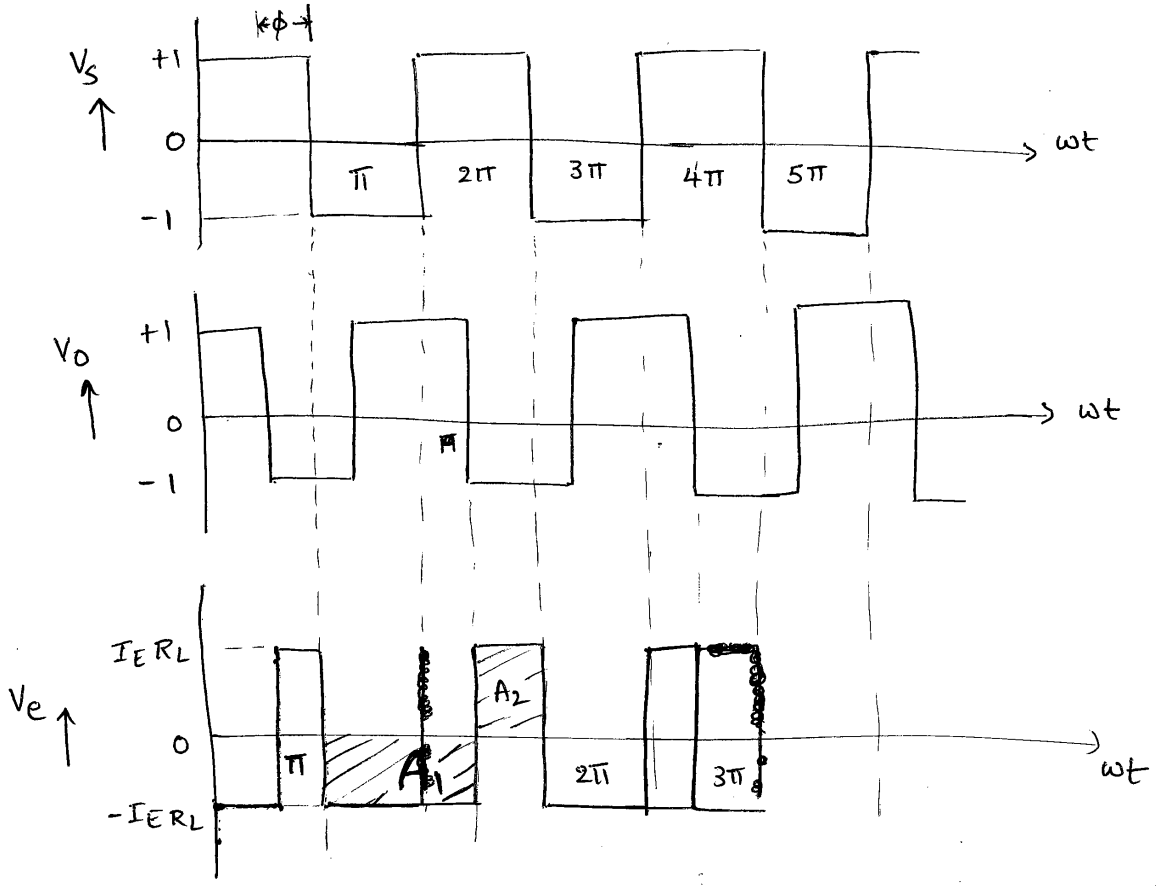


Fig: phase detector for IC PLL

Transistors $Q_3 - Q_4$ and $Q_5 - Q_6$ are two sets of SPDT switches activated by the VCO output.

The inpot signal V_S and the VCO output V_o are assumed to be high enough to switch the transistors in figure above fully on or off.



Fig(b): Timing diagram of inpot and outpot waveforms for balanced modulator circuit.

In figure (b) when V_S and V_o both are high during the time 0 to $(\pi - \phi)$, transistors Q_1 and Q_3 are driven on and current I_E flows through Q_1 and Q_3. This gives an output voltage

$$V_e = -I_E R_L$$

Next for the period $(\pi - \theta)$ for π, when V_S is high and V_o is low, transistors Q_1 and Q_4 are driven on resulting in an output voltage $V_e = I_E R_L$

In this way, the output voltage waveform Ve is obtained

$$V_{e(avg)} = \frac{1}{\pi}\left[(\text{area } A_1) + \text{area}(A_2)\right]$$

$$= \frac{1}{\pi}\left[I_E R_L \phi + (-I_E R_L) \times (\pi - \phi) \right]$$

$$= I_E R_L \left[\frac{2\phi}{\pi} - 1 \right]$$

$$V_{e(avg)} = \frac{2 I_E R_L}{\pi}\left[\phi - \frac{\pi}{2} \right] \quad \text{--- (1)}$$

$$V_{e(avg)} = K_\phi \left(\phi - \frac{\pi}{2} \right)$$

where $K_\phi = \frac{2 I_E R_L}{\pi} = \frac{4 I_Q R_L}{\pi}$ $\left[\because I_E = 2 I_Q \right]$

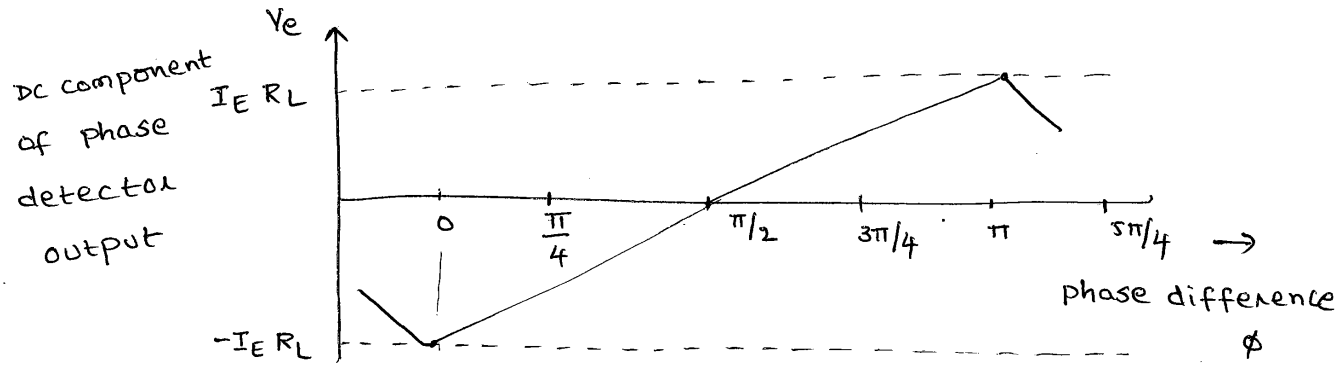


Fig (c)

where K_ϕ is the phase angle to voltage transfer co-efficient or the conversion ratio of the phase detector. This linear relationship between Ve and ϕ is shown in figure (c).

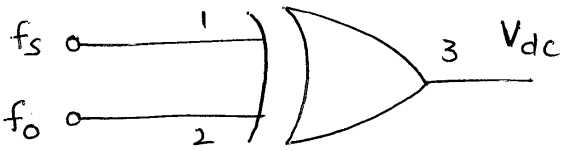
2) ~~Digition~~ Digital phase detector :

There are two types of digital phase detectors available

a) Digital phase detector using EX-OR detector

b) Edge triggered phase detector.

a) EXOR phase detector :



Fig(a): EXOR phase detector

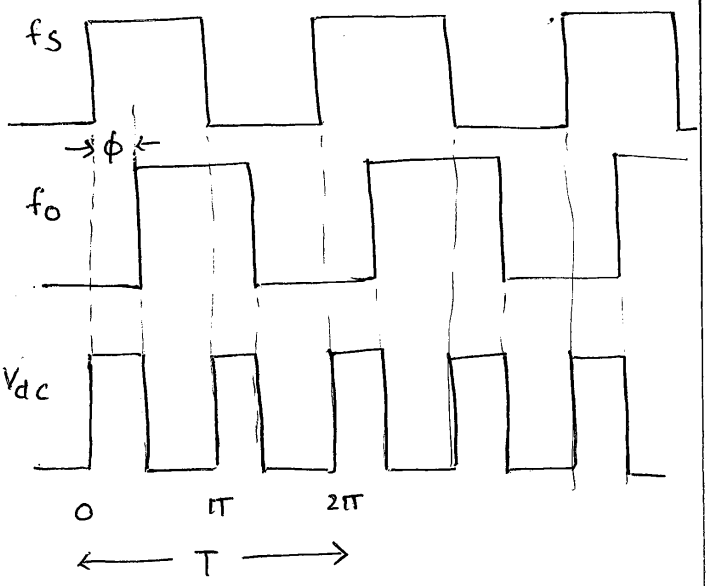


Fig: Input and output waveforms

Figure shows the digital type XOR phase detector. It uses CMOS type 4070 Quad 2-input XOR gate. The output of the XOR Gate is high when only one of the input signals f_s (or) f_o is high. This type of detector is used when both the input signals are square waves. The input and output waveforms for $f_s = f_o$ are shown in fig(b). In this figure f_s is leading f_o by ϕ degrees. The variation of dc output voltage with phase difference ϕ is shown in fig(c).

It can be seen that the maximum dc output voltage occurs when the phase difference is π because the output of the gate remains high throughout.

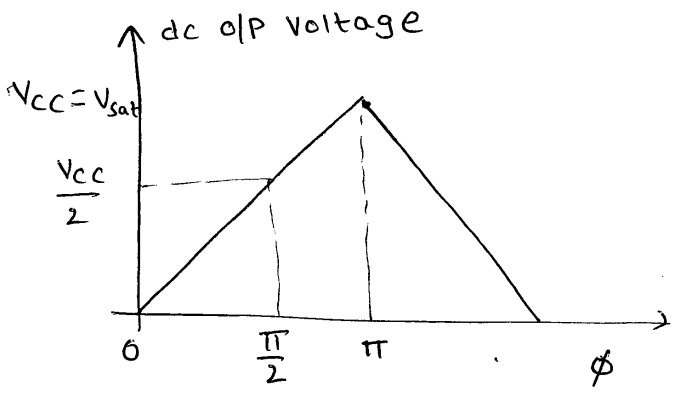


Fig (c): DC output voltage versus ϕ

the slope of the curve gives the conversion ratio K_ϕ of the phase detector. so the conversion ratio K_ϕ for a supply voltage $V_{cc} = 5V$ is , $K_\phi = \frac{5}{} = 1.59$ V/rad

b) Edge triggered phase Detector :

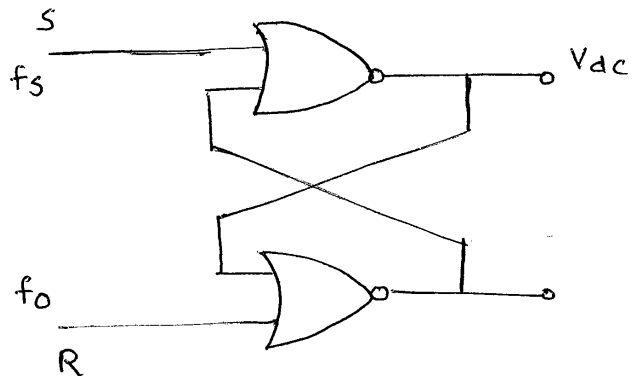


Fig (a) : Edge triggered phase detector

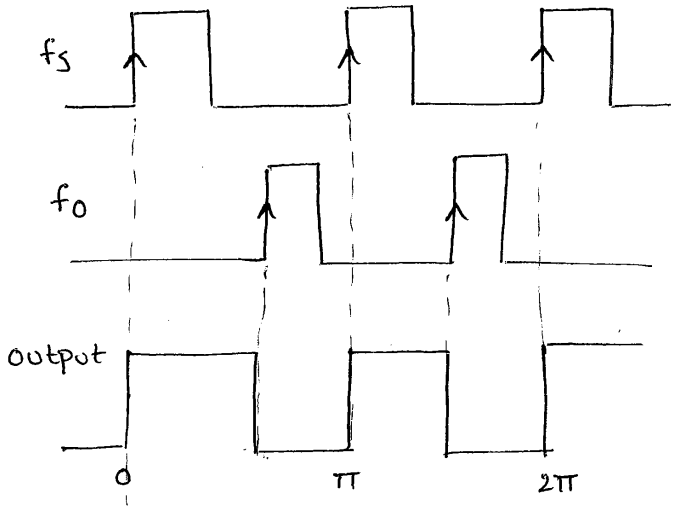


Fig (b) : Inpot and output waveforms

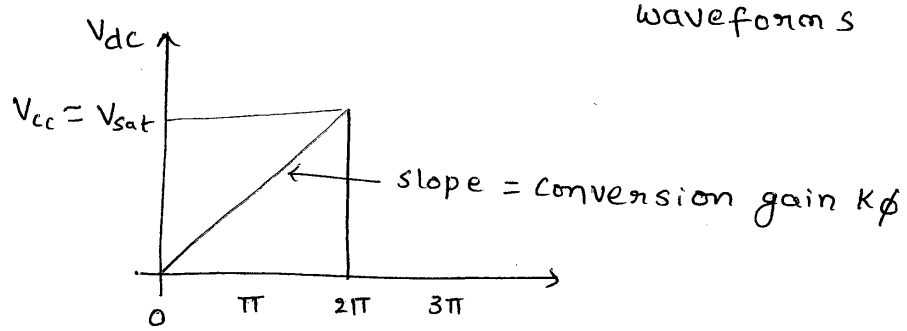


Fig (c) : DC output voltage Vs ϕ

The edge triggered digital phase detector is shown in figure (a). The circuit is an RS flip flop made by NOR gates. This circuit is useful when fs and fo are both pulse waveforms with duty cycle less than 50 %.

The output of the R-S flip flop changes its state on the leading edge of fs and fo as shown in fig (b). The variation of dc output voltage Vs ϕ is shown in fig (c). This type of detector has better capture tracking and locking characteristics as the dc output voltage is linear up to 360° compared to 180° in the case of EX-OR detector.

Voltage controlled oscillator (VCO):

A common type of VCO available in IC form NE/SE 566. The pin configuration and basic block diagram of 566 VCO are shown in figures below.

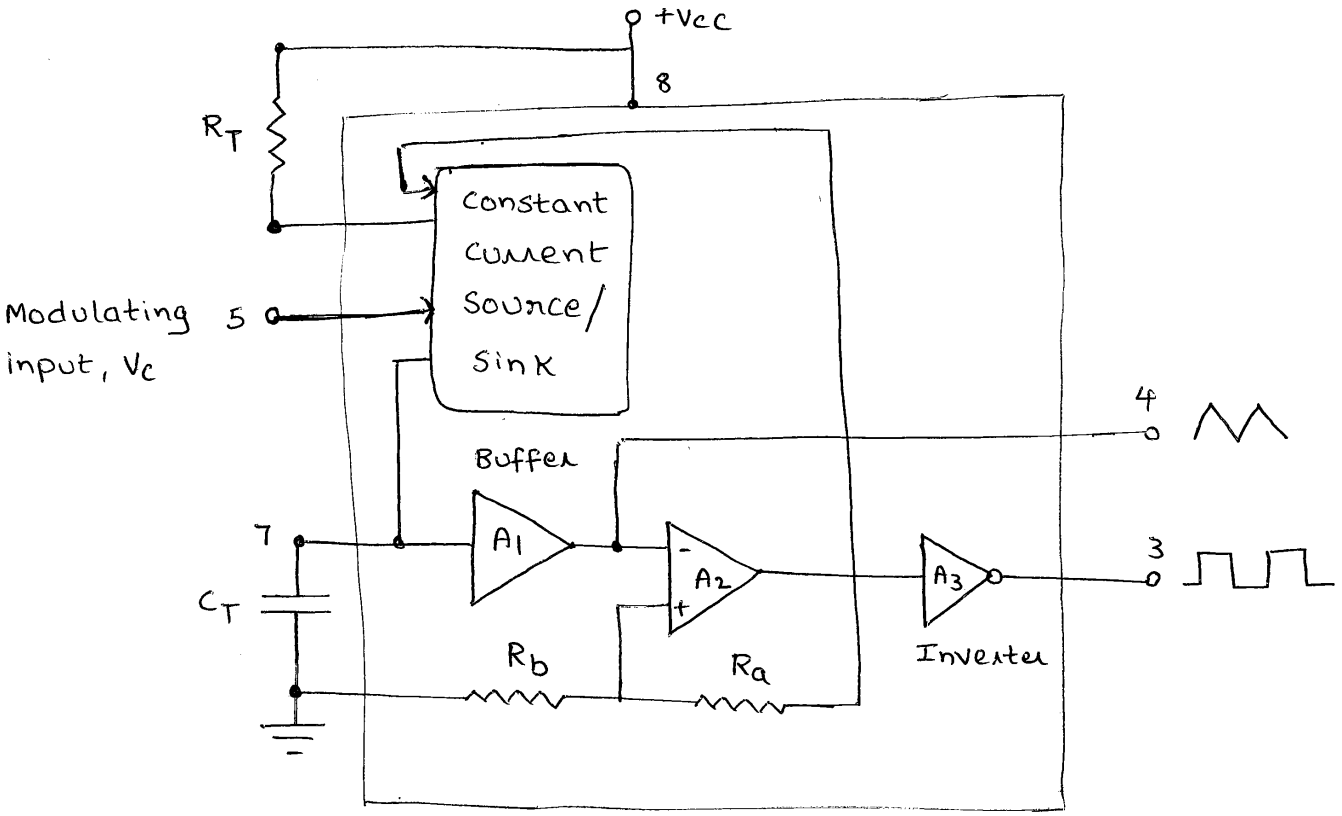


Fig: Voltage controlled oscillator block diagram

A timing capacitor C_T is linearly charged or discharged by a constant current source / sink. The amount of current can be controlled by changing the voltage V_c applied at the modulating input (Pin 5) or by changing the timing resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage at pin 5.

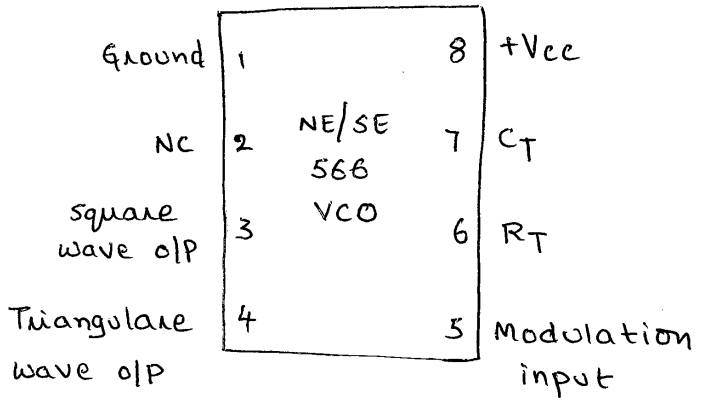


Fig: Pin Configuration.

Thus if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

A small capacitor of 0.001 μF should be connected between pin 5 and 6 to eliminate possible oscillations. A VCO is commonly used in converting low frequency signals.

The voltage across the capacitor C_T is applied to the inverting input terminal of schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the schmitt trigger is designed to Vcc and 0.5 Vcc. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 Vcc to 0.25 Vcc.

In fig(c), when the voltage on the capacitor C_T exceeds 0.5 Vcc during the charging, the output of the schmitt trigger goes low (0.5 Vcc) the capacitor now discharges and when it is at 0.25 Vcc, the output of schmitt trigger goes High(Vcc).

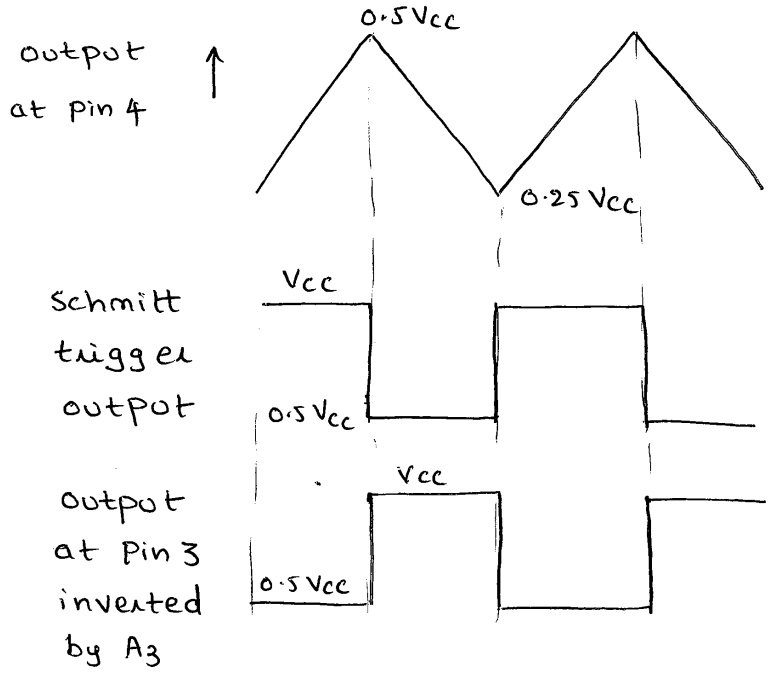


Fig c: output waveform.

since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular waveform across C_T which is also available at pin 4.

The square wave output of the schmitt trigger is inverted by inverter A_3 and is available at pin 3.

The output waveforms are shown in fig (c)

The output frequency of the VCO can be calculated as follows.

The total voltage on the capacitor charges from 0.25 V_{cc} to 0.5 V_{cc}. Thus $\Delta V = 0.25\ V_{cc}$

The capacitor charges with a constant current source. So

$$i = C_T \frac{\Delta V}{\Delta t} \Rightarrow \frac{0.25\ V_{cc}}{\Delta t} = \frac{i}{C_T}$$

$$\Delta t = \frac{0.25\ V_{cc}\ C_T}{i} \quad (or)$$

The time period T of the triangular waveform $= 2\Delta t$

The frequency of oscillator f_o is

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5\ V_{cc}\ C_T}$$

$$i = \frac{V_{cc} - V_c}{R_T}$$

where V_c is the voltage at pin 5. Therefore

$$f_o = \frac{2\ (V_{cc} - V_c)}{R_T\ C_T\ V_{cc}} \longrightarrow (1)$$

the output frequency of the VCO can be changed either by (i) R_T (ii) C_T (iii) the voltage V_c at the modulating input terminal Pin 5.

With no modulating input signal, if the voltage at Pin 5 is biased at $\frac{7}{8}V_{CC}$, Eq ① gives the VCO output frequency as

$$f_o = \frac{2\left(V_{CC} - \frac{7}{8}V_{CC}\right)}{R_T C_T V_{CC}} = \frac{0.25}{R_T C_T} \longrightarrow (2)$$

Voltage to frequency conversion factor:

A parameter of importance for VCO is voltage to frequency conversion factor K_V and is defined as

$$K_V = \frac{\Delta f_o}{\Delta V_c}$$

Here ΔV_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO. If we assume that the original frequency is f_o and the new frequency is f_1, then

$$\Delta f_o = f_1 - f_o = \frac{2\left(V_{CC} - V_c + \Delta V_c\right)}{R_T C_T V_{CC}} - \frac{2\left(V_{CC} - V_c\right)}{R_T C_T V_{CC}}$$

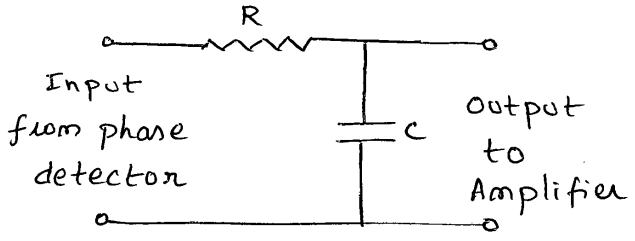
$$\Delta f_o = \frac{2\Delta V_c}{R_T C_T V_{CC}} \qquad (\text{or}) \quad \Delta V_c = \frac{\Delta f_o R_T C_T V_{CC}}{2}$$

putting the value of $R_T C_T$ from Eq (2)

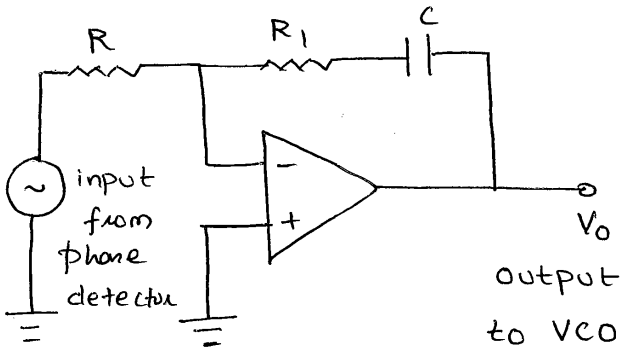
$$\Delta V_c = \frac{\Delta f_o V_{CC}}{8 f_o} \Rightarrow K_V = \frac{\Delta f_o}{\Delta V_c} = \frac{8 f_o}{V_{CC}}$$

Low pass filter:

The filter used in a PLL may be either passive type or active type as shown in figures below.



Fig(a): Passive filter



Fig(b): Active filter

The low pass filter not only removes the high frequency components and noise, but also controls the dynamic characteristics of the PLL. These characteristics include capture, lock range, band width and transient response. If filter band width is reduced, the response time increases. However reducing the band width of the filter also reduces the capture range of the PLL.

The charge on the filter capacitor gives a short time memory to the PLL. Thus even if the signal becomes less than the noise for a few cycles, the dc voltage on the capacitor continues to shift the frequency of the VCO till it picks up signal again. This produces a high noise immunity and locking stability.

Monolithic phase - locked loop :

All the different building blocks of PLL are available as independent IC packages and can be externally interconnected to make a PLL. However a number of manufacturers introduced monolithic PLL's too. Important Monolithic PLL is IC 565 :

IC 565 PLL :

565 is available as 14-pin DIP package and as 10-pin metal can package. the pin configuration and the block diagram are shown in fig (a) and (b)

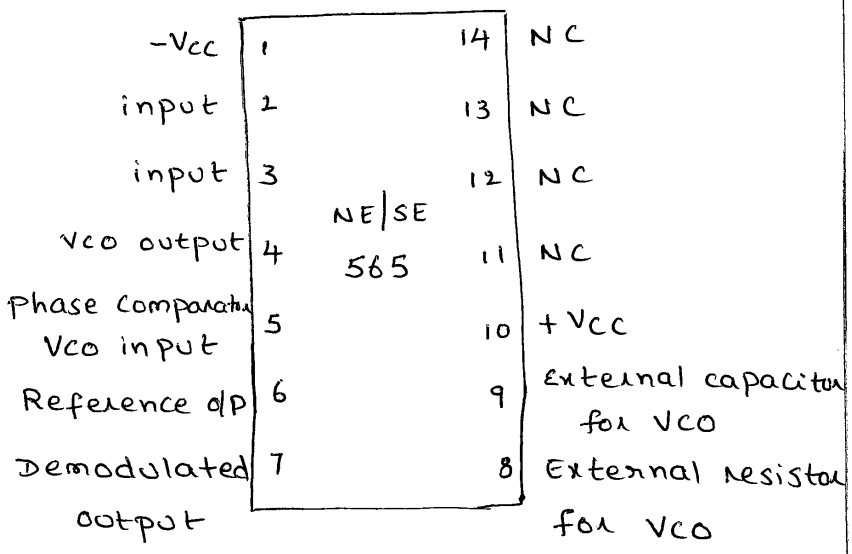


Fig a : Pin Diagram

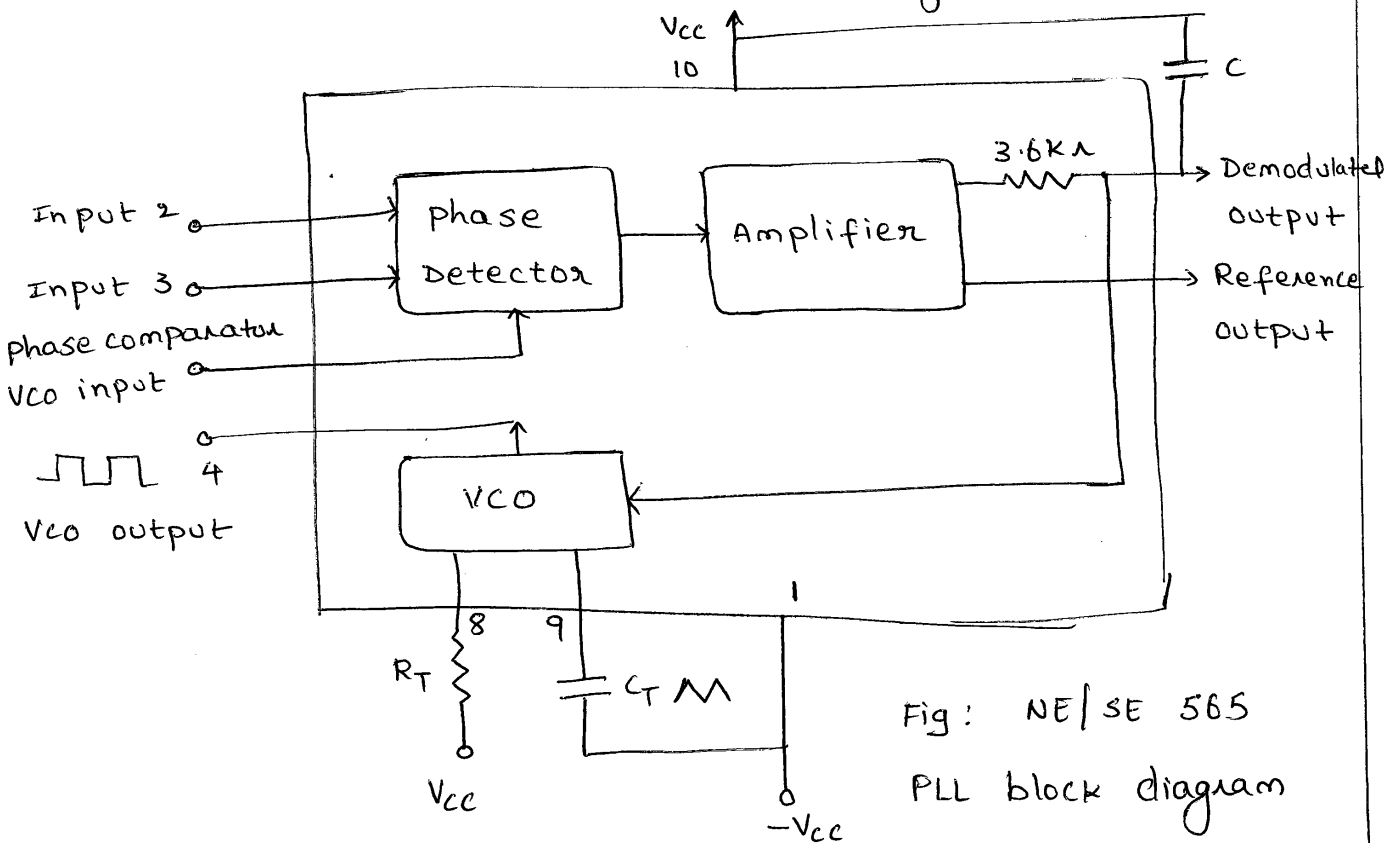


Fig : NE/SE 565 PLL block diagram

the output frequency of the VCO (both inputs 2,3 grounded) can be given as

$$f_o = \frac{0.25}{R_T C_T}$$

where R_T and C_T are the external resistor and capacitor connected to pin 8 and 9.

the VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range. It may be seen that PLL is internally broken b/n the VCO output and the phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_o with input signal f_s. A capacitor C is connected between Pin 7 and Pin 10 to make a low pass filter with the internal resistance of 3.6KΩ.

Derivation of Lock-in Range:

If ϕ radians is the phase difference between the signal and the VCO voltage, then the output voltage of the analog phase detector is given by

$$V_e = K_\phi \left(\phi - \frac{\pi}{2}\right) \longrightarrow (1)$$

where K_ϕ is the phase angle to voltage transfer co-efficient of the phase detector. the control voltage to VCO is

$$V_c = A K_\phi \left(\phi - \frac{\pi}{2}\right) \longrightarrow (2)$$

where A → Voltage gain of the Amplifier

This V_c shifts VCO frequency from its free running frequency f_0 to a frequency f given by

$$f = f_0 + K_V V_c \longrightarrow (3)$$

where K_V → voltage to frequency transfer co-efficient of the VCO.

when PLL is locked in to signal frequency f_s, then we have

$$f = f_s = f_0 + K_V V_c$$

since $V_c = \frac{f_s - f_0}{K_V} = A K_\phi \left(\phi - \frac{\pi}{2}\right)$ [∵ from 2] → (4)

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian and $V_{c(max)} = \pm K_\phi \frac{\pi}{2}$. The corresponding value of the maximum control voltage available to drive the VCO will be

$$V_{c(max)} = \pm \left(\frac{\pi}{2}\right) K_\phi A \longrightarrow (5)$$

The maximum VCO frequency swing that can be obtained is given by

$$f_s = f_0 \pm (f - f_0)_{max} = f_0 \pm K_V K_\phi \left(\frac{\pi}{2}\right) A = f_0 + \Delta f_L$$

Here $\Delta f_L = \pm K_V K_\phi A \frac{\pi}{2} \longrightarrow (6)$

Total lock range $2\Delta f_L = \pm K_V K_\phi A \pi \longrightarrow (7)$

The lock-in range is symmetrically located with respect to VCO free running frequency f_0

For IC 565 PLL

$$K_V = \frac{8 f_0}{V} \rightarrow (8) \text{ where } V = +V_{cc} - (-V_{cc})$$

Again $K_\phi = \frac{1.4}{\pi}$ and $A = 1.4$

Hence the lock-in range becomes

$$\boxed{\Delta f_L = \frac{\pm 7.8 f_o}{V}} \longrightarrow (9)$$

Derivation of capture Range :

When PLL is not initially locked to the signal, the frequency of the VCO will be free running frequency f_o. The phase angle difference between the signal and the VCO output voltage will be

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o)t + \Delta\theta \longrightarrow (1)$$

thus the phase angle difference doesn't remain constant but will change with time at a rate given by

$$\frac{d\phi}{dt} = \omega_s - \omega_o \longrightarrow (2)$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\phi \frac{\pi}{2}$ and a fundamental frequency $f_s - f_o = \Delta f$

the low pass filter is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j\left(\frac{f}{f_1}\right)} \quad \text{where} \quad f_1 = \frac{1}{2\pi RC}$$

$$|T(jf)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_1}\right)^2}} \longrightarrow (3)$$

As $(f/f_1)^2 >> 1$ then $T(f) = \frac{f_1}{f} \longrightarrow (4)$

the fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $\Delta f = f_s - f_0$. then

$$T(\Delta f) = \frac{f_1}{\Delta f} = \frac{f_1}{f_s - f_0} \longrightarrow (5)$$

The voltage V_c to drive the VCO is

$$V_c = V_e \times T(f) \times A$$

$$V_{c(max)} = V_{e(max)} \times T(f) \times A$$

$$V_{c(max)} = \pm K_\phi \left(\frac{\pi}{2}\right) A \frac{f_1}{\Delta f} \longrightarrow (6)$$

then the corresponding value of the maximum VCO frequency shift is

$$(f - f_0)_{max} = K_V V_{c(max)} = \pm K_V K_\phi \left(\frac{\pi}{2}\right) A \frac{f_1}{\Delta f} \rightarrow (7)$$

For the acquisition of the signal frequency we should put $f = f_s$, so that the maximum signal frequency range that can be acquired by PLL is

$$(f_s - f_0)_{max} = \pm K_V K_\phi \left(\frac{\pi}{2}\right) A \frac{f_1}{\Delta f_c}$$

Now $\Delta f_c = (f_s - f_0)_{max}$

So $(\Delta f_c)^2 = \pm K_V K_\phi \left(\frac{\pi}{2}\right) A f_1$

Since $\Delta f_L = \pm K_V K_\phi \left(\frac{\pi}{2}\right) A$

then $\Delta f_c = \pm \sqrt{f_1 \Delta f_L}$

Therefore the total capture range is $2\Delta f_c = \pm 2\sqrt{f_1 \Delta f_L}$

In case of IC PLL 565, $R = 3.6\,k\Omega$ so the capture range is

$$\Delta f_C = \pm \left[\frac{\Delta f_L}{2\pi (3.6 \times 10^3) C} \right]^{1/2}$$

The capture range is symmetrically located with respect to VCO free running frequency f_0 as shown in figure below. The PLL cannot acquire a signal outside the capture range, but once captured, it will hold on till the signal frequency goes beyond the lock-in range. In order to increase the ability of lock-in range, large capture range is required. However a large capture range will make the PLL more susceptible to noise and undesirable signal. Hence a suitable compromise is often reached between these two opposing requirements of the capture range.

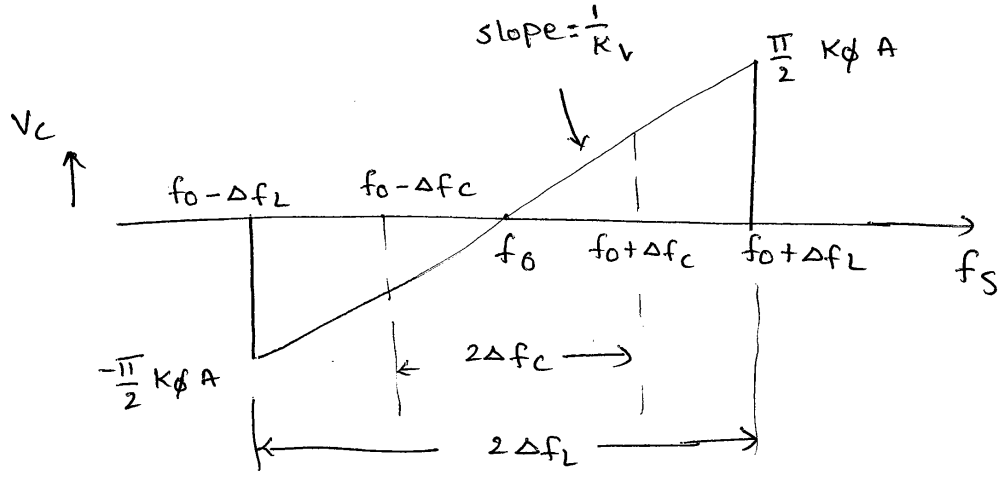


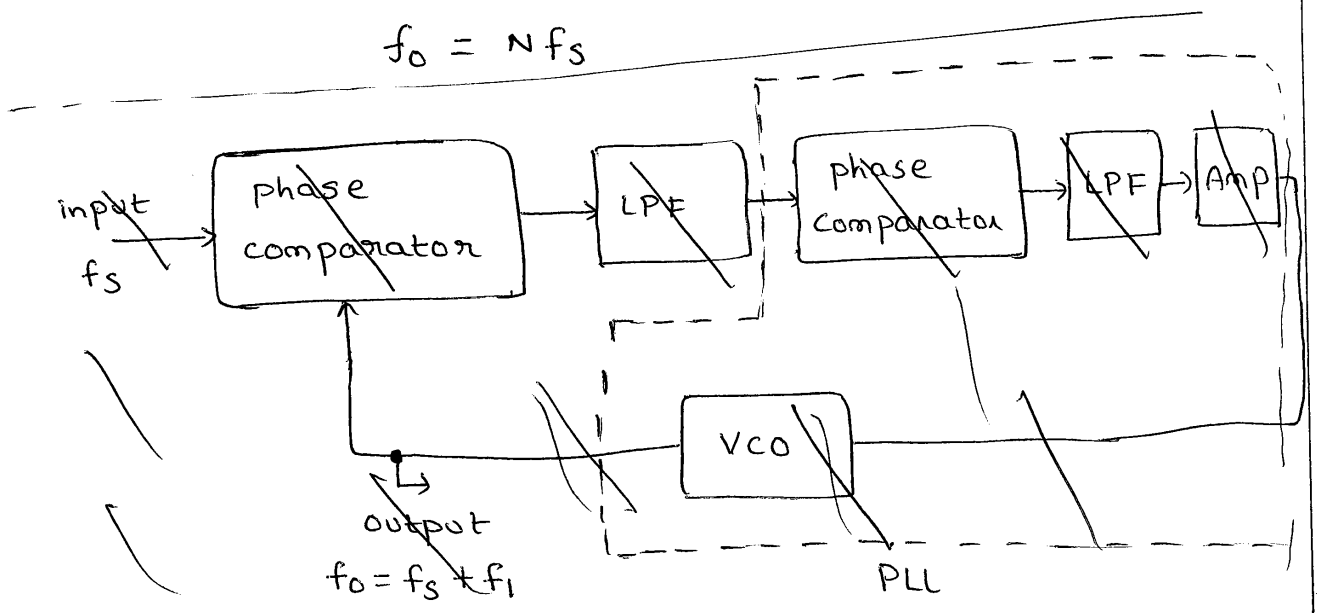
Fig: PLL lock-in range and capture range

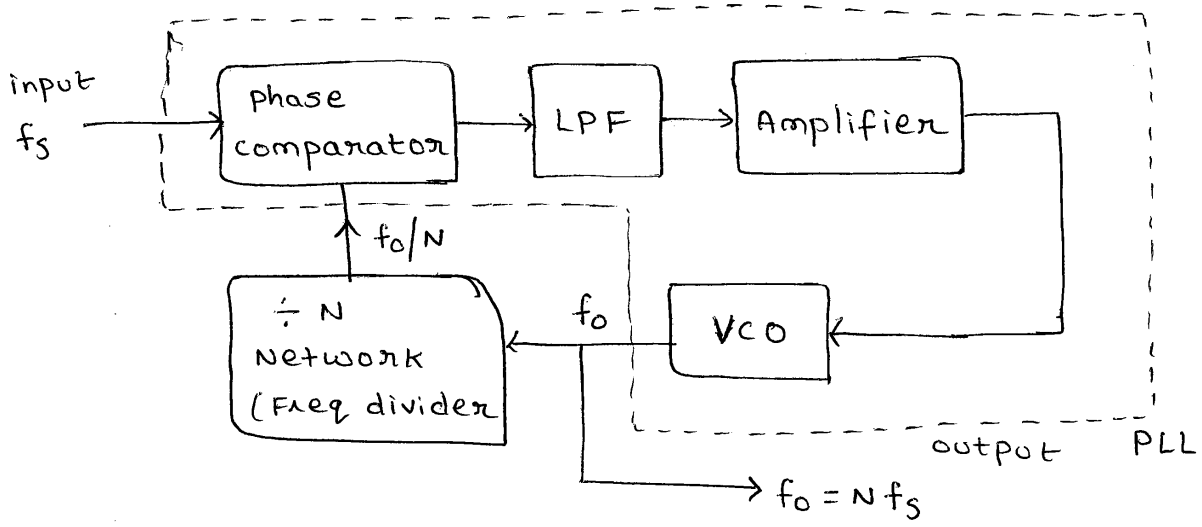
Applications of PLL :

The output from a PLL system can be obtained either as the voltage signal $V_c(t)$ corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator application where as the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

1. Frequency Multiplication / Division :

Figure below gives the block diagram of a frequency multiplier using PLL. A divide by N network is inserted between the VCO output and the phase comparator input. In the locked state, the VCO output frequency f_o is given by





The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

Frequency multiplication can also be obtained by using PLL in its harmonic locking mode.

The above circuit can also be used for frequency division. Since the VCO output (a square wave) is rich in harmonics. it is possible to lock the m-th harmonic of the VCO output with the input signal f_s. The output f_o of VCO is now given by

$$f_o = \frac{f_s}{m}$$

2) Frequency Translation :

A schematic for shifting the frequency of an oscillator by a small factor is shown in figure below. It can be seen that a multiplier and a low-pass filter are connected externally to the PLL.

The signal f_s which has to be shifted and the output frequency f_o of the VCO are applied as

inputs to the multiplier. The output of the multiplier contains the sum and difference of f_s and f_o. However, the output of LPF contains only the difference signal $(f_o - f_s)$. The translation or offset frequency f_1 $(f_1 << f_s)$ is applied to the phase comparator.

When PLL is in locked state

$$f_o - f_s = f_1$$

$$f_o = f_s + f_1 \quad (\text{or})$$

Thus it is possible to shift the incoming frequency f_s by f_1

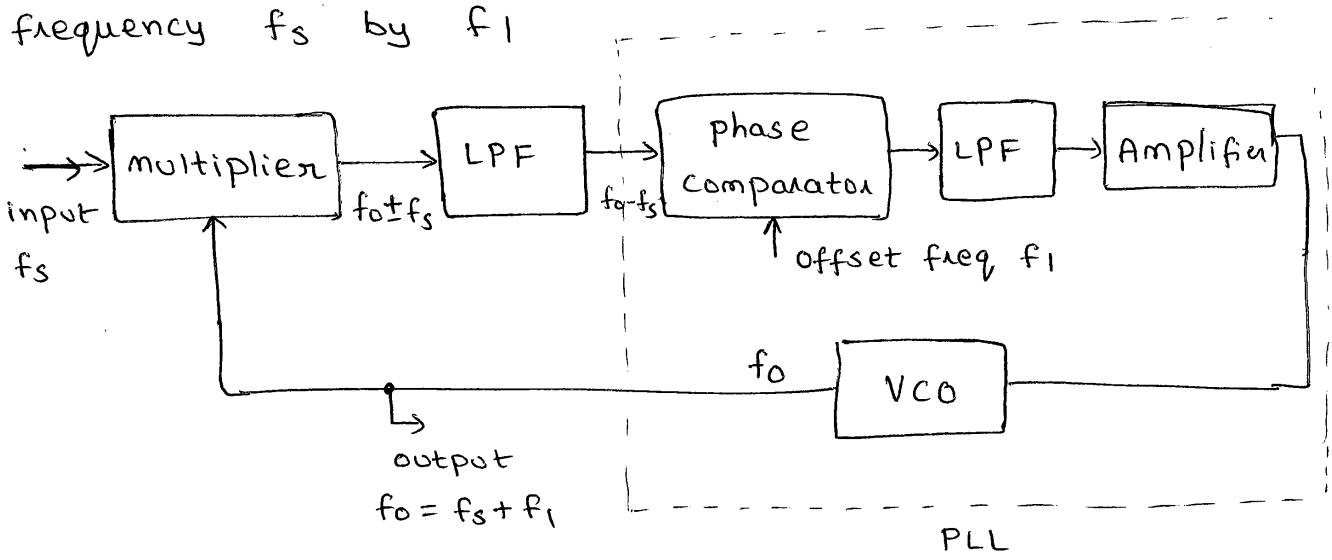


Fig: PLL used as a frequency translator.

3) AM Detection:

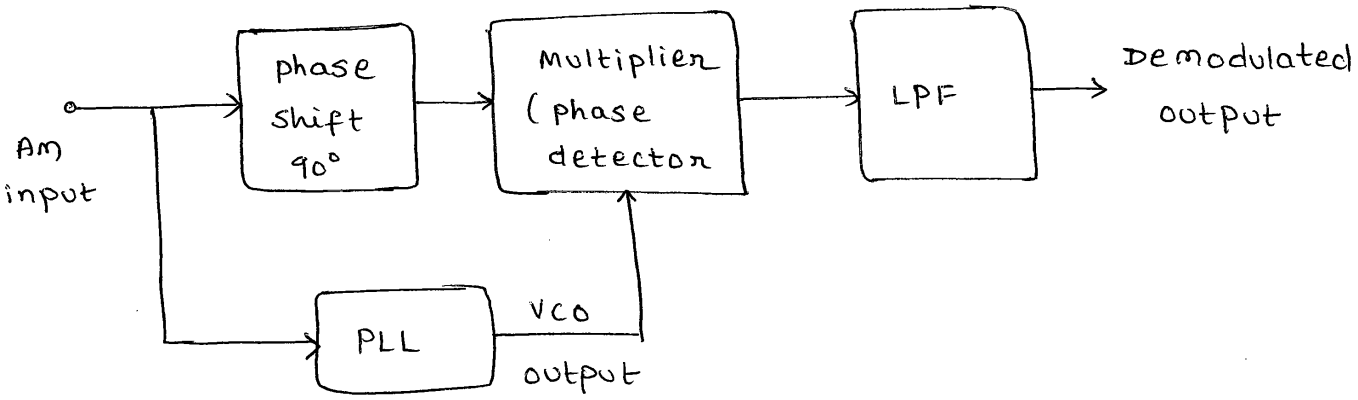


Fig: PLL Used as AM Demodulator.

A PLL may be used to demodulate Am signals as shown in figure above. The PLL is locked to the carrier frequency of the incoming Am signal. The output of the VCO which has the same frequency as the carrier, but unmodulated is fed to the Amplifier.

since VCO output is always 90° out of phase with the incoming Am signal under the locked Condition, the AM input signal is also shifted in phase by 90° before being fed to the amplifier. This makes both the signals applied to the multiplier in same phase.

The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL Am detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

UNIT - IV

Voltage Regulator

Introduction:

The function of a voltage regulator is to provide a stable dc voltage for powering other electronic circuits. A voltage regulator should be capable of providing substantial output current. Voltage regulators are classified as

1. Series Regulator
2. Switching Regulator.

Series regulator use a power transistor connected in series between the unregulated dc input and the load. The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor. Since the transistor conducts in the active or linear region, these regulators are also called linear regulators. Linear regulators may have fixed or variable output voltage and could be positive or negative.

Switching regulator operate the power transistor as a high frequency ON/OFF switch, so that the power transistor doesn't conduct current continuously. This gives improved efficiency over series regulator.

Series op-Amp Regulator :

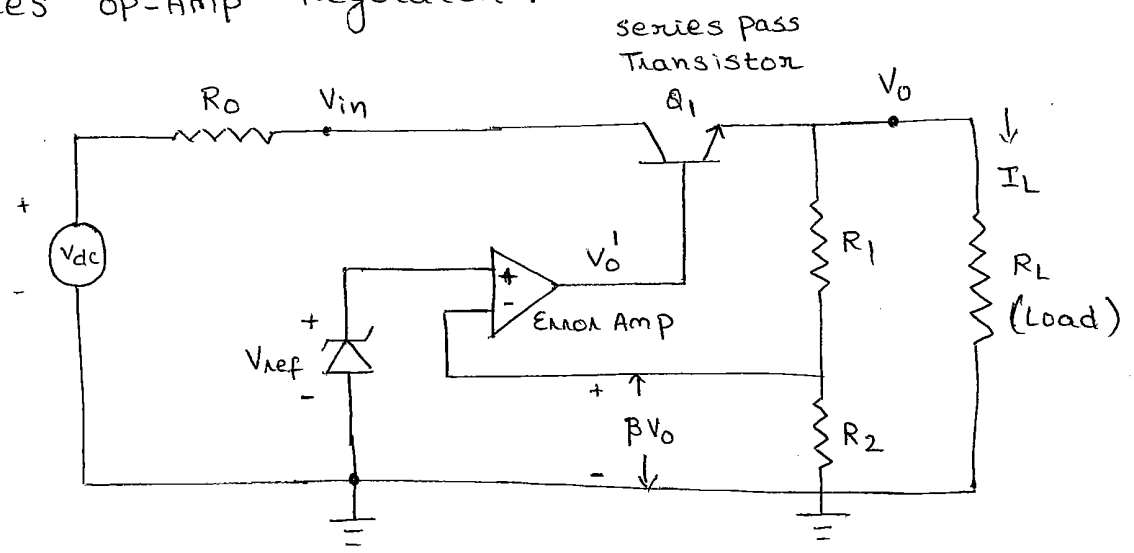


Fig : A Regulated power supply.

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations. Figure above shows a regulated power supply using discrete components. the circuit consists of following four parts.

1. Reference voltage circuit
2. Error Amplifier
3. series pass transistor
4. Feedback Network.

the power transistor Q_1 is in series with the unregulated dc voltage V_{in} and the regulated output voltage V_0. so it must absorb the difference between these voltages whenever any fluctuation in output voltage V_0 occurs.

The transistor Q_1 is also connected as an emitter follower and therefore provides sufficient current gain to drive the load. The output voltage is sampled by the R_1-R_2 divider and fed back to the negative input terminal of the op-Amp error Amplifier. This sampled voltage is compared with the reference voltage V_{ref} (usually obtained by a zener diode). The output V_o' of the error amplifier drives the series transistor Q_1.

If the output voltage increases, due to variation in load current, the sampled voltage βV_o also increases where $\beta = \frac{R_2}{R_1 + R_2}$.

This inturn reduces the output voltage V_o' of the diff Amp due to 180° phase difference provided by the op-Amp amplifier. V_o' is applied to the base of Q_1, which is used as an emitter follower. So V_o follows V_o', that is V_o also reduces. Hence the increase in V_o is nullified. Similarly, reduction in output voltage also gets regulated.

IC voltage Regulators :

With the advent of micro electronics, it is possible to incorporate the complete ckt of voltage regulator on a monolithic Si chip. This gives low cost, high reliability, reduction in size and excellent performance.

Fixed Voltage series Regulator:

78XX series are three terminal, positive fixed voltage regulators. There are seven output voltage options available such as 5, 6, 8, 12, 15, 18 and 24 V.

In 78XX, the last two numbers (XX) indicate the output voltage.

Thus 7815 represents a 15V regulator.

Fig below shows the standard representation of monolithic voltage regulator. A capacitor C1 (0.33μF) is usually connected between input terminal and ground to cancel the inductive effects due to long distribution leads. The output capacitor Co(1μF) improves the transient response.

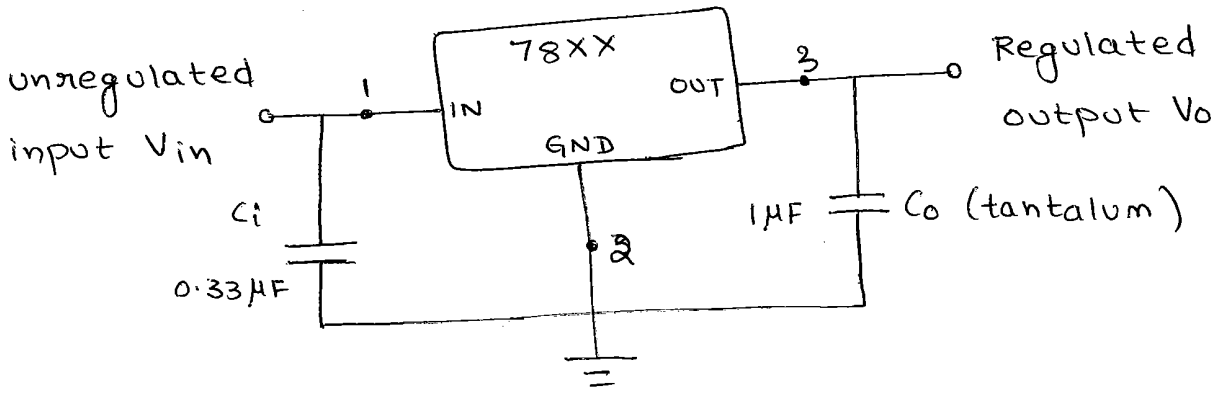


Fig: standard representation of a three terminal positive monolithic regulator.

→ 79XX series are three terminal, Negative fixed voltage regulators. these are complements to the 78XX series. There are two extra voltage options of -2V and -5.2 available in 79XX series.

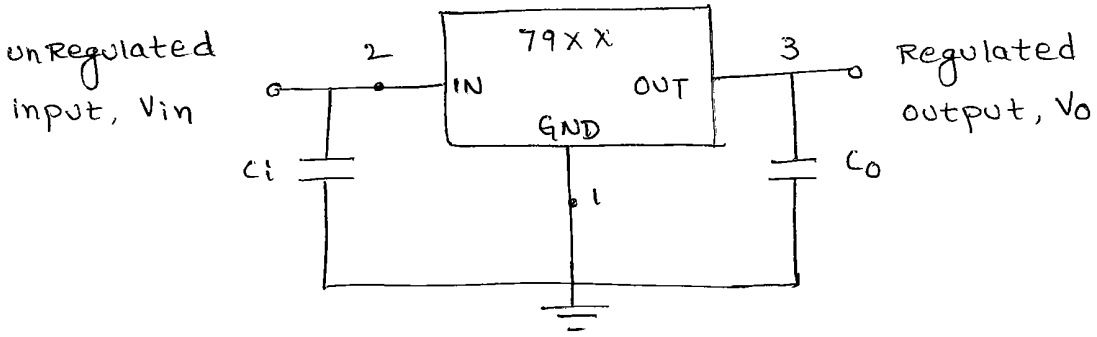


Fig: standard representation of a three terminal Negative monolithic regulator.

National Semi Conductor also produces three terminal voltage regulators in LM series. There are three series available for different operating temperature ranges.

LM 100	Series	$-55^{\circ}C$	to	$+125^{\circ}C$
LM 200	Series	$-25^{\circ}C$	to	$+85^{\circ}C$
LM 300	Series	$0^{\circ}C$	to	$+70^{\circ}C$

Characteristics:

1. V_o : The regulated output voltage is fixed at a value as specified by the manufacturer.
2. $|V_{in}| \geq |V_o| + 2$ Volts : The un regulated input voltage must be atleast 2V more than the regulated output voltage. For example, if $V_o = 5V$, then $V_{in} = 7V$
3. $I_{o(max)}$: the load current may vary from 0 to rated maximum output current. The IC is usually provided with a heat sink, otherwise it may not provide the rated maximum output current.

4. Thermal shut down : The IC has a temperature sensor (built-in) which turns off the IC when it becomes too hot (usually 125°C to 150°C). The output current will drop and remains there until the IC has cooled significantly.

5. Line / Input Regulation :

It is defined as the percentage change in the output voltage for a change in the input voltage. It is usually expressed in millivolts or as a percentage of the output voltage. Typical value of line regulation of 7805 is 3mV [from data sheet]

6. Load Regulation :

The load regulation is the change in the regulated output voltage when the load current is changed from minimum (no load) to maximum (full load). It is also expressed in millivolts or as a percentage of V_o.

$$\text{Load Regulation} = V_{NL} - V_{FL}$$

$$\% \text{ Load Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

V_{NL} = Load voltage with no load current

V_{FL} = Load voltage with full load current.

7. Ripple Rejection:

The output of rectifier and filter circuit consists of ripples. The ripple is equivalent to periodic changes in input voltage. Due to the negative feedback, the ripple voltage gets attenuated by large amount. the factor by which it gets reduced is $1+A\beta$. mathematically the output ripple of a voltage regulator is given by

$$V_{R(out)} = \frac{V_{R(in)}}{1+A\beta}, \quad \text{Ripple Rejection} = \frac{V_{R(out)}}{V_{R(in)}}$$

In data sheet Ripple Rejection is expressed in decibels (dB)

$$\text{Ripple Rejection in dB} = 20 \log \frac{V_{R(out)}}{V_{R(in)}}$$

Applications of Fixed Voltage Regulators:

the three terminal fixed voltage regulator can be used as a current source. Figure below shows the circuit where 7805 has been wired to supply a current of 1 ampere to a 10Ω, 10 watt load.

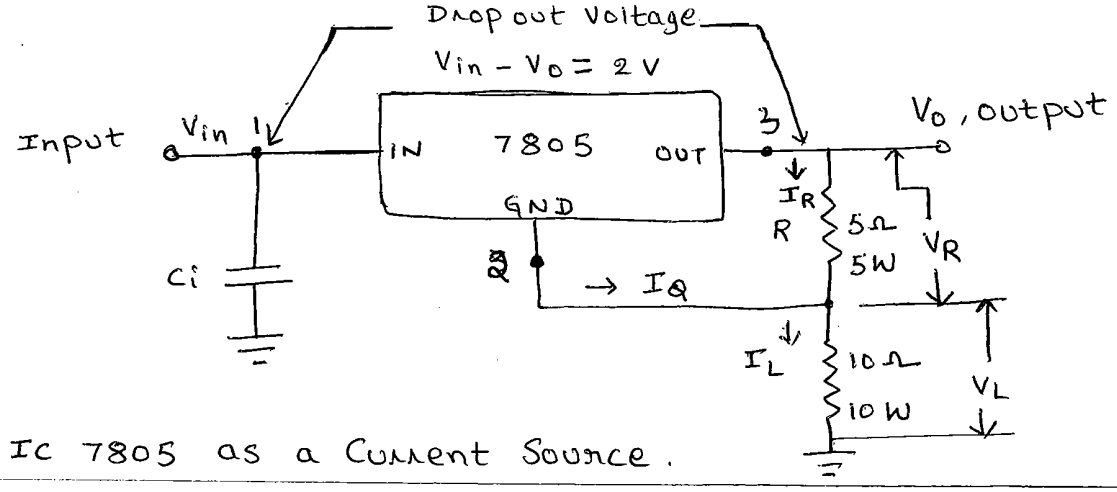


Fig: Ic 7805 as a Current Source.

Here $I_L = I_R + I_Q$

where I_Q → quiescent current and is about 4.2 mA for 7805.

$$I_L = \frac{V_R}{R} + I_Q$$

since $I_L = 1A$, $\frac{V_R}{R} = 1A$ ($\because I_Q$ is neglected)

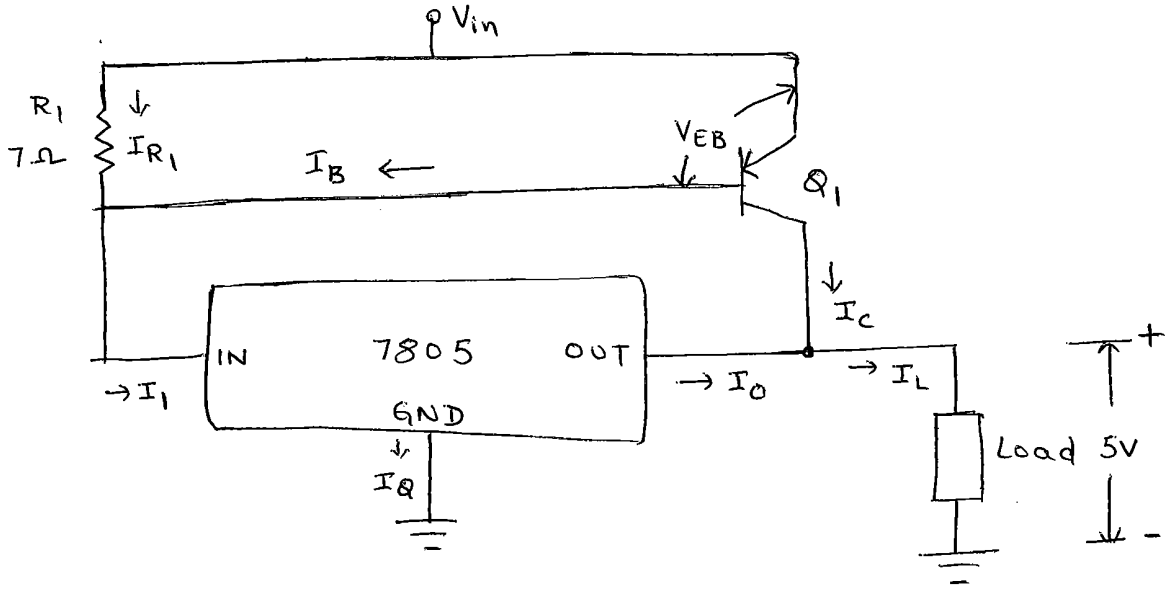
Also $V_R = 5V$ (Voltage between terminal 3 and 2)

So the value of R required is

$$R = \frac{5V}{1A} = 5\Omega.$$

thus choose $R = 5\Omega$ to deliver 1A current to a load of ~~KA~~. 10Ω.

2) Boosting IC Regulator output current;



It is possible to boost the output current of a three terminal regulator simply by connecting an external pass transistor in parallel with the regulator as shown in figure above.

For low load currents, the voltage drop across R_1 is insufficient ($< 0.7V$) to turn on transistor Q_1 and the regulator itself is able to supply the load current.

However as I_L increases, the voltage drop across R_1 increases. When this voltage drop is approximately 0.7V, the transistor Q_1 turns ON. It can be easily seen that if $I_L = 100mA$, the voltage drop across R_1 is equal to $7\Omega \times 100mA = 0.7V$. Thus if I_L increases more than 100mA, the transistor Q_1 turns ON and supplies the extra current required. Since $V_{EB(on)}$ remains constant, the excess current comes from Q_1's base after amplification by β. The regulator adjusts I_B so that

$$I_L = I_C + I_O \rightarrow (1) \quad \text{and} \quad I_C = \beta I_B \rightarrow (2)$$

For the regulator $I_O = I_i - I_Q \simeq I_i$ ($I_Q \rightarrow$ neglect) $\rightarrow (3)$

$$I_B = I_i - I_{R_1}$$

$$I_B = I_O - \frac{V_{EB(ON)}}{R_1} \quad \left[\because I_O = I_i\right] \rightarrow (4)$$

Now Eq (1) $\Rightarrow$ $I_L = \beta I_B + I_O$

$$I_L = \beta\left[I_O - \frac{V_{EB(ON)}}{R_1}\right] + I_O$$

$$I_L = (\beta+1) I_O - \beta \frac{V_{EB(ON)}}{R_1} \rightarrow (5)$$

The maximum current $I_{O(max)}$ for a 7805 regulator is 1A from the data sheet. Assuming $V_{EB(ON)} = 0.7V$ and $\beta = 15$, we get

$$I_L = (16 \times 1) - \left(15 \times \frac{0.7}{7}\right)$$

$$I_L = 14.5 \text{ A}$$

(3) Fixed Regulator used as Adjustable Regulator :

In the laboratory, we may need variable regulated voltages or a voltage that is not available as standard fixed voltage regulator. This can be achieved by using a fixed three terminal regulator as shown in figure. Here ground terminal of fixed three terminal regulator is floating.

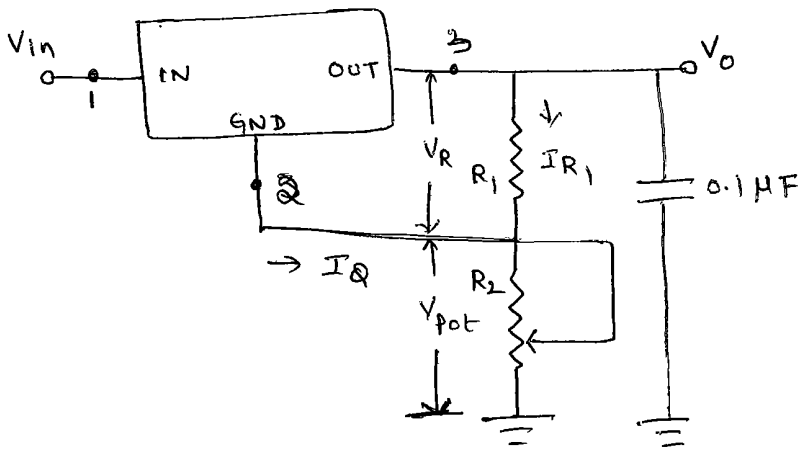


Fig: Adjustable Regulator

Here the output voltage

$$V_o = V_R + V_{pot} = V_R + (I_Q + I_{R_1}) R_2$$

$$V_o = V_R + I_Q R_2 + \frac{V_R}{R_1} R_2 .$$

$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_R + I_Q R_2 .$$

where V_R is the regulated voltage difference b/n OUT and GND terminals. The effect of I_Q is minimized by choosing R_2 small enough to minimize the term $I_Q R_2$. The minimum output voltage is the value of the fixed voltage available from the regulator.

The LM117, 217, 317 positive regulators, LM137, 237, 337 negative regulators have been specially designed to be used for obtaining adjustable output voltages.

It is possible to adjust output voltage from 1.2V to 40V and current up to 1.5A.

723 General purpose Regulator :

For 723, output voltage is adjustable from 2V to 37V.

Limitations of three terminal Regulators :

1. No short circuit protection
2. output voltage (positive or Negative) is fixed.

These limitations have been overcome in the 723 general purpose regulator, which can be adjusted over a wide range of both positive or negative regulated voltage. This Ic is inherently low current device, but can be boosted to provide 5 amps or more current by connecting external components.

The limitation of 723 is that it has no in-built thermal protection. It also has no short circuit current limits.

Functional block diagram of a 723 regulator IC :

Figure below shows the functional block diagram of a 723 regulator. It has two separate sections. The zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7 volts at the terminal V_{ref}. The constant current sources forces the zener to operate a fixed point so that the zener outputs a fixed voltage.

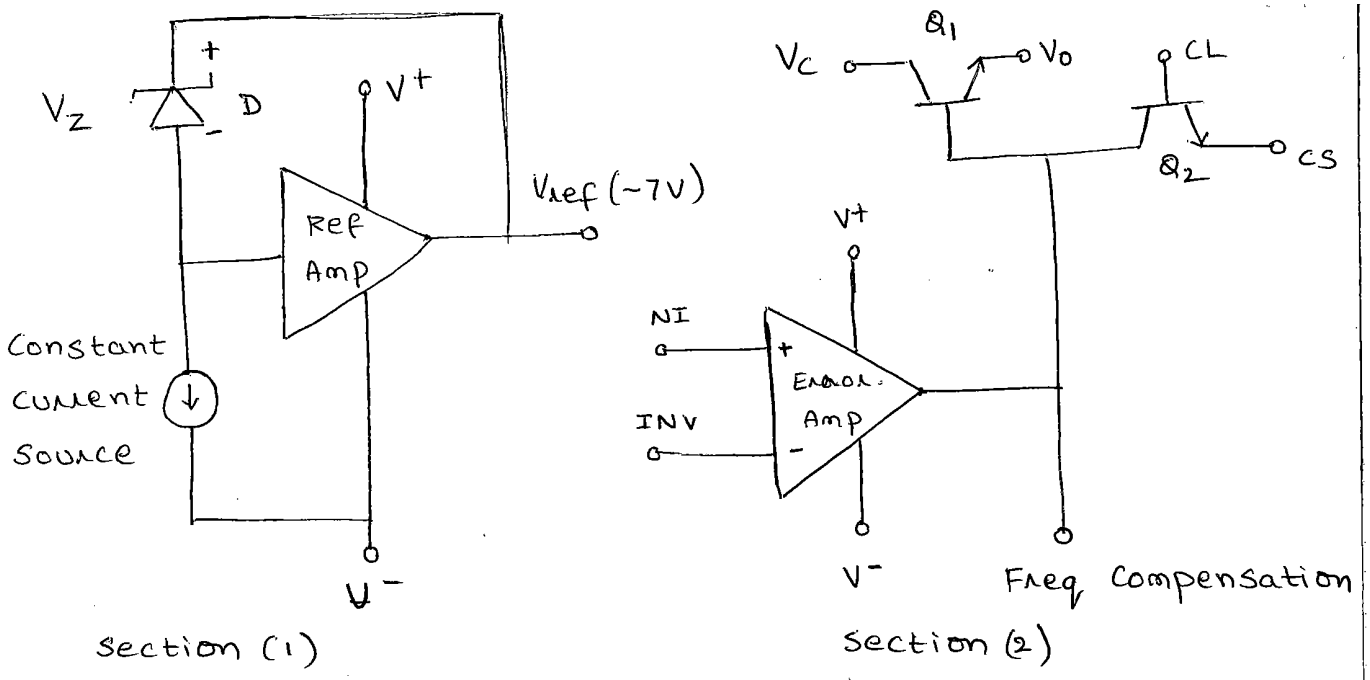


Fig: Function Block diagram of 723 regulator.

The other section of the IC consists of an error Amplifier, a series pass transistor Q_1 and a current limit transistor Q_2. The error amplifier compares a sample of the output voltage applied at the INV terminal to the reference voltage at the NI terminal. The error signal controls the conduction of Q_1.

Pin Configuration of 723 IC:

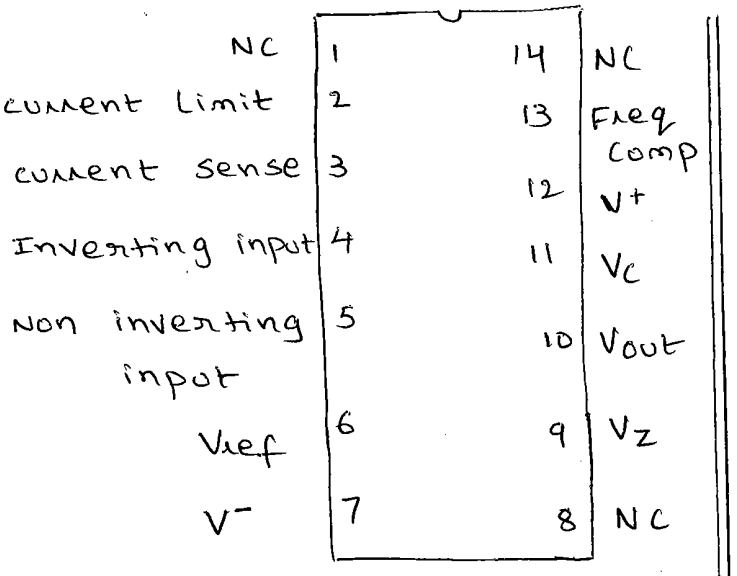


Fig: 14 pin DIP

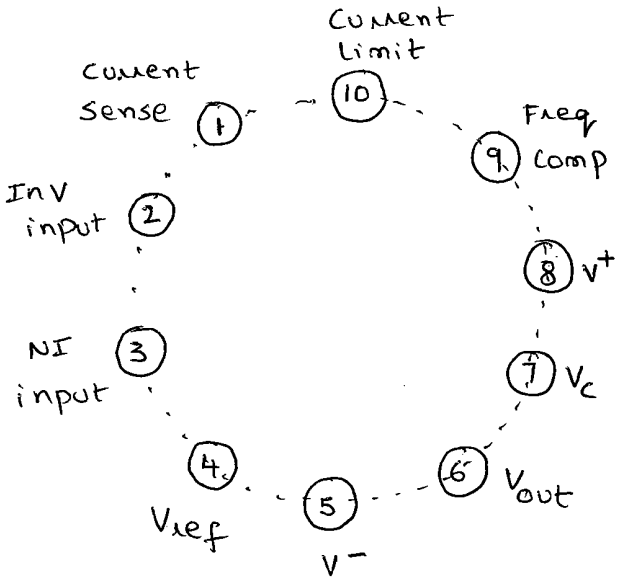
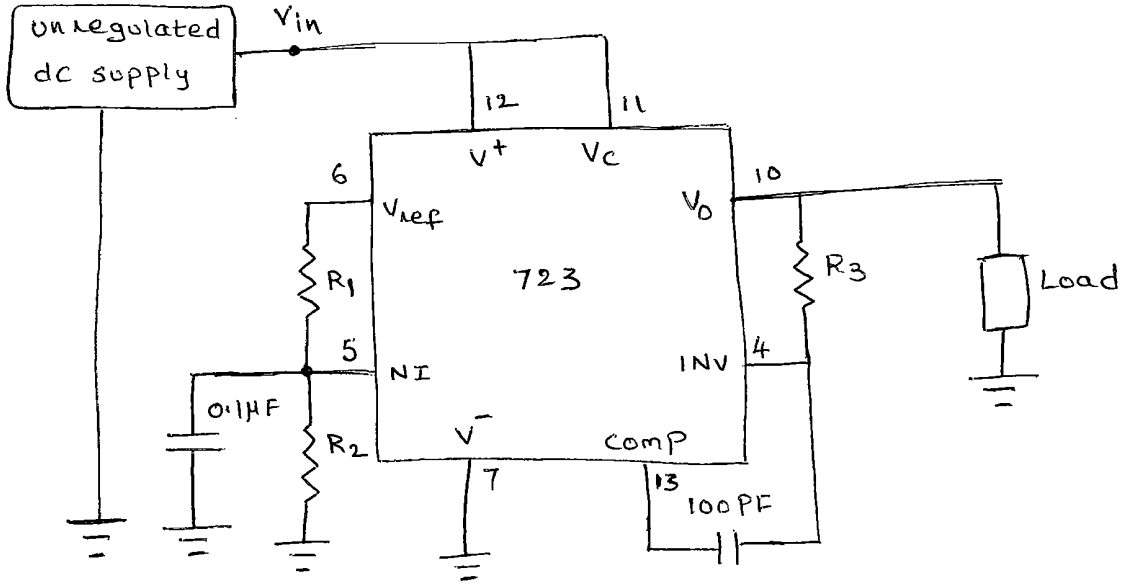
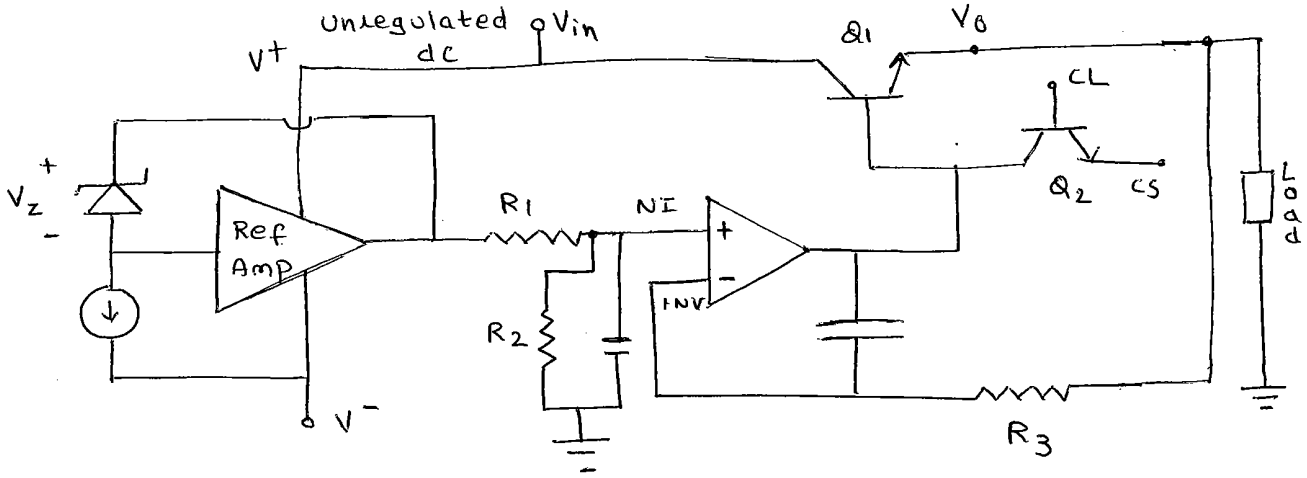


Fig: 10 pin metal-can

Low voltage Regulator Using IC 723



Fig(a); Low voltage Regulator using 723 IC



Fig(b) Functional diagram for a Low voltage Regulator

A simple positive low voltage (2V to 7V) regulator can be made using as shown in schematic of fig(a). In order to understand the voltage at the NI terminal of the error Amplifier due to R_1R_2 divider is

$$V_{NI} = V_{ref} \frac{R_2}{R_1 + R_2} \longrightarrow (1)$$

The difference between V_{NI} and the output voltage V_o which is directly fed back to the INV terminal is amplified by the error Amplifier. The output of the

error Amplifier drives the pass transistor Q_1 so as to minimize the difference between the NI and INV inputs of error Amplifier. since Q_1 is operating as an emitter follower.

$$V_o = V_{ref} \frac{R_2}{R_1 + R_2} \longrightarrow (2)$$

If the output voltage becomes low, the voltage at the INV terminal of error Amplifier also goes down. This makes the output of the error amp to become more positive, thereby driving transistor Q_1 more in to Conduction This reduces the voltage across Q_1 and drives more current in to the load causing voltage across load to increase. so the initial drop in the load voltage has been compensated. similarly, any increase in load voltage, or changes in the input voltage get regulated.

the reference voltage is typically 7V. so the o/p voltage V_o is

$$V_o = 7 \times \frac{R_2}{R_1 + R_2}$$

which will always be less than 7V. so the circuit shown in fig(a) is used as low voltage (< 7) 723 regulator.

<u>High voltage Regulator using IC 723 regulator</u>:

If it is desired to produce regulated output voltage greater than 7V, then the below circuit can be used. The NI terminal is connected directly to V_{ref} through R_3. so the voltage at the NI terminal is V_{ref}. The error Amplifier operates as a non-inverting Amplifier

with a voltage gain of

$$A_V = 1 + \frac{R_1}{R_2}$$

So the output voltage for the circuit is

$$V_o = 7\left(1 + \frac{R_1}{R_2}\right)$$

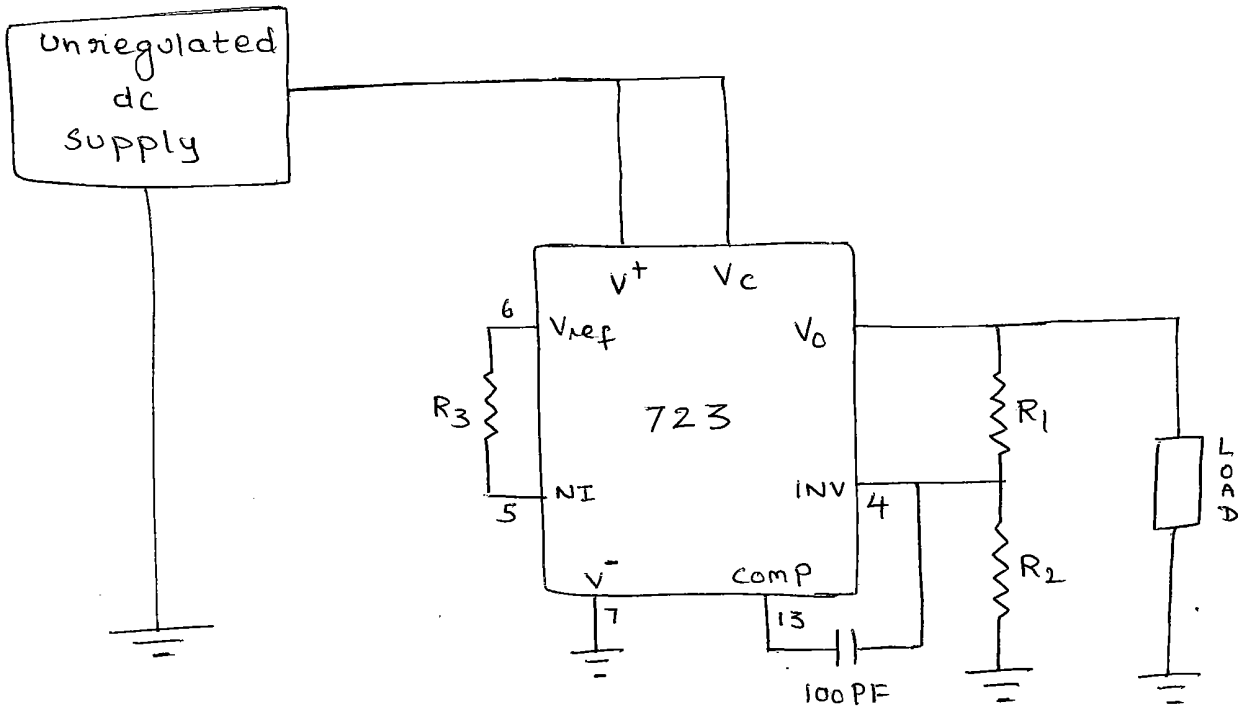


Fig: Basic High voltage 723 Regulator

Current Limit protection:

The circuits of low voltage and high voltage regulator using 723 IC have no protection. If the load demands more current (Eg: under short circuit conditions), the IC tries to provide it at a constant output voltage getting hotter all the time. This may ultimately burn the IC.

The IC is, therefore, provided with a current limit facility. Current limiting refers to the ability of a regulator to prevent the load current from increasing

above a present value. The characteristic curve of a current limited power supply is shown in figure(a) below. The output voltage remains constant for a load current below I_{Limit}. As current approaches to the limit, the output voltage drops. The current limit I_{limit} is set by connecting an external resistor Rsc between the terminals CL and CS terminals as shown in fig(b) below. The CL terminal is also connected to the output terminal V_o and CS terminal to the load.

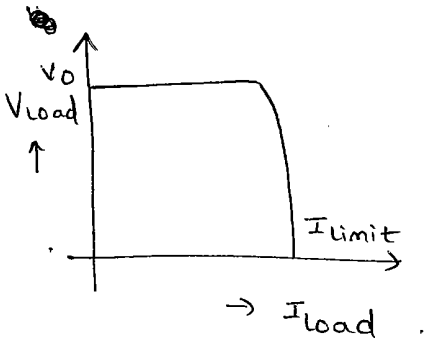
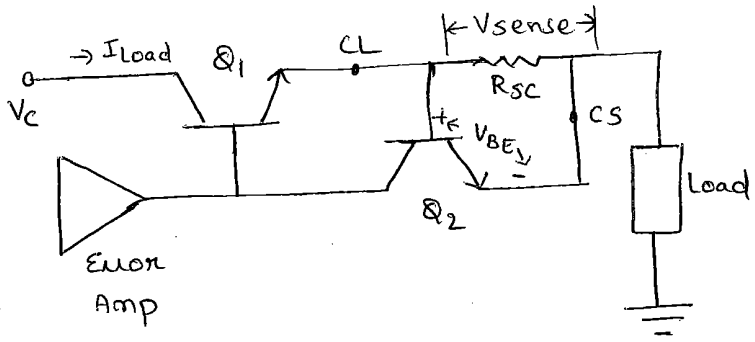


Fig (a): characteristic curve for a current limited regulator.



Fig(b): current limit protection circuit.

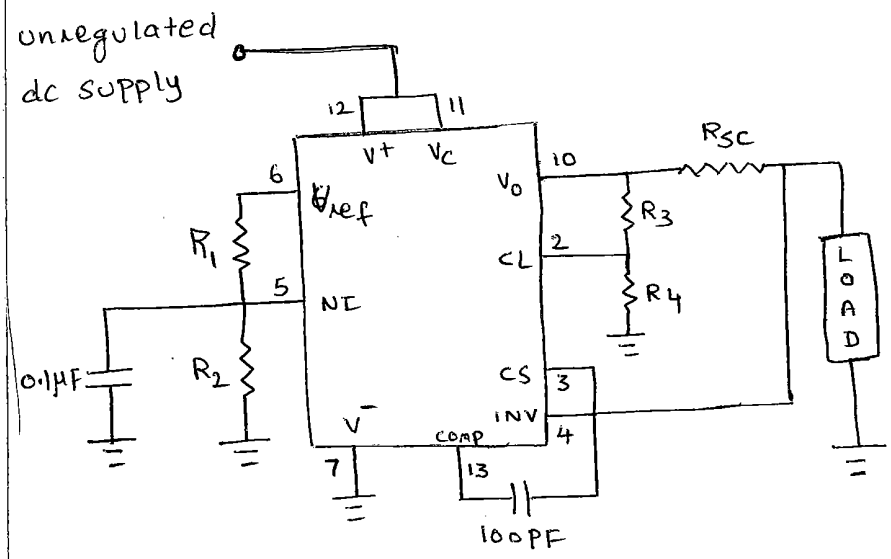
The load current produces a small voltage drop Vsense across Rsc. This voltage Vsense is applied directly across the base emitter junction of Q_2. when this voltage is approximately 0.5 volt, transistor Q_2 begins to turn ON. Now a part of the current from error Amplifier goes to the collector of Q_2, there by decreasing the base current of Q_1. This inturn, reduces the emitter current of Q_1. So any increase in the load current will get nullified.

Similarly if the load current decreases, V_{BE} of Q_2 drops, repeating the cycle in such a manner that the load current is held constant to produce a voltage across R_{SC} sufficient to turn ON Q_2. This voltage is typically 0.5 V

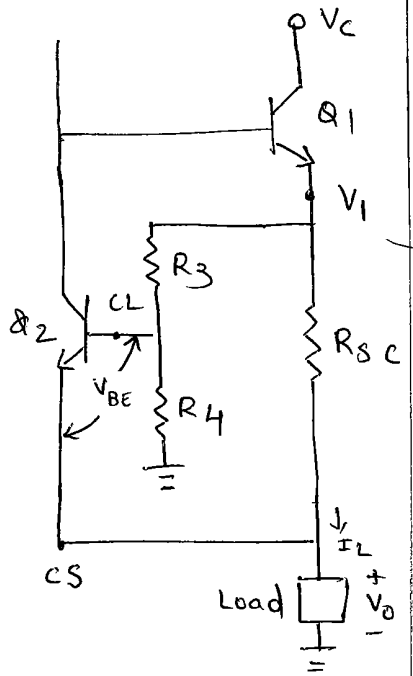
$$\text{So} \quad I_{Limit} = \frac{V_{sense}}{R_{SC}} = \frac{0.5\,V}{R_{SC}}$$

This method of current limiting is also referred to as current sensing technique.

Current ~~Fold~~ Foldback :



Fig(a): A low voltage regulator using current fold back



Fig(b): Current fold back (partial schematic)

In current limiting technique, the load current is maintained at a present value and when over load condition occurs, the output voltage V_o drops to zero. However, if the load is short circuited, maximum current doesn't flow through the regulator. A method which is used

to protect the regulator which will limit the short circuit current and allow higher currents to the load.

The circuit of figure (a) shows the method of applying current fold back. In order to understand the operation of the circuit, consider the circuit of figure (b). the voltage at terminal CL is divided by $R_3 - R_4$ network. The current limit transistor Q_2 conducts only when the drop across the resistance R_{sc} is large enough to produce a base emitter voltage of Q_2 to be atleast 0.5V.

As Q_2 starts conducting transistor Q_1 begins to turn off and the current I_L decreases. This reduces the voltage V_1 at the emitter of Q_1 and also the output voltage V_o.

the voltage at the base of Q_2 (CL) will be $V_1 \frac{R4}{R_3 + R_4}$. Thus the voltage at the CL terminal drops by a smaller amount compared to the drop in voltage at cs terminal. This increase V_{BE} of Q_2 thereby increasing the conduction of Q_2, which inturn reduces the conduction of Q_1. That is the current I_L further reduces. this process continues till $V_o = 0V$ and V_1 is just large enough to keep 0.5V between CL and cs terminal. this point I_{sc} and has been reduced by lowering both I_L and V_o.

Current Boosting:

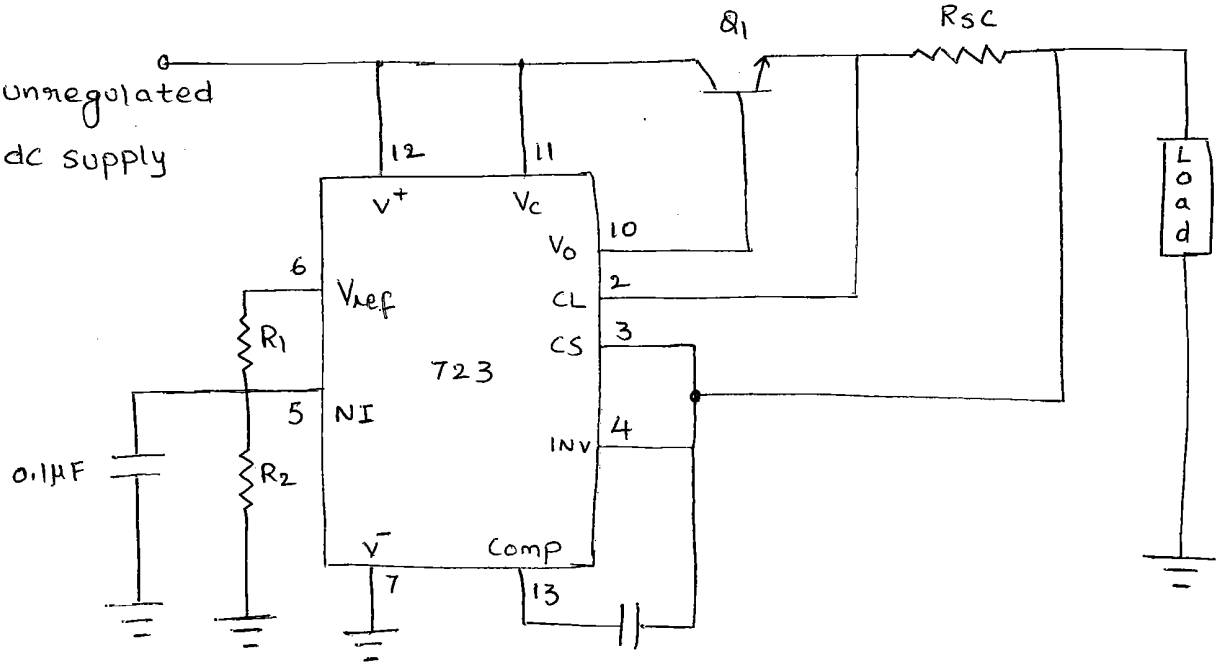


Fig: Current boosted low voltage regulator.

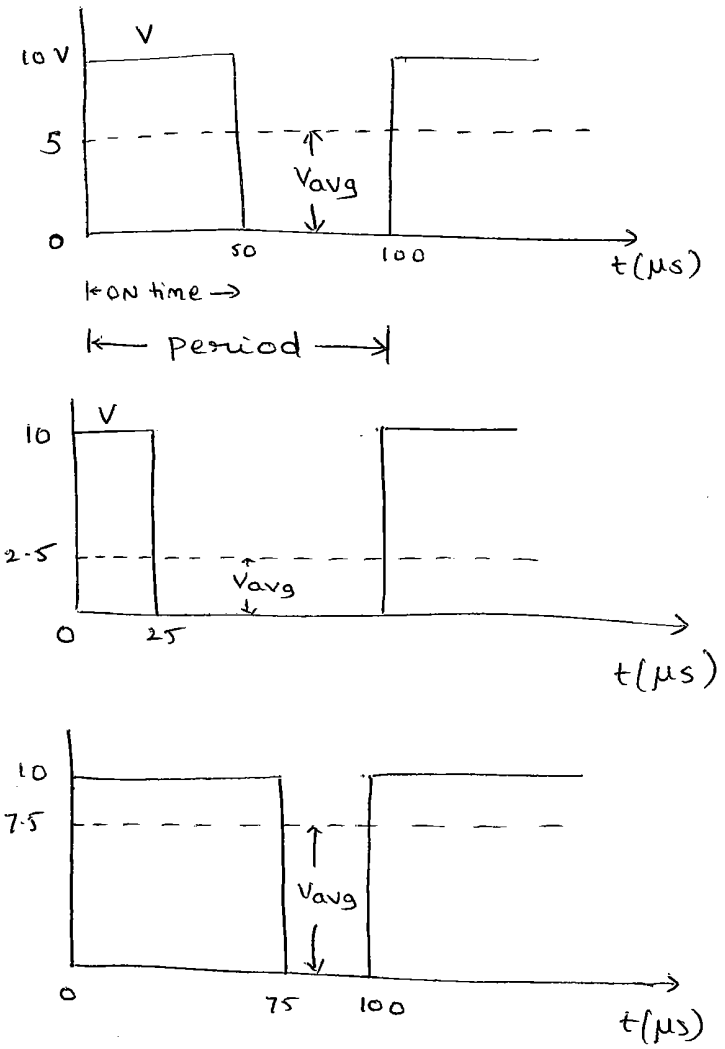
The maximum current that 723 IC regulator can provide is 140 mA. For many applications that is not sufficient. It is possible to boost the current level simply by adding a boost transistor Q_1 to the voltage regulator as shown in figure above. The collector current of the pass transistor Q_1 comes from the unregulated dc supply. The output current from V_o terminal drives the base of the pass transistor Q_1. This base current gets multiplied by the beta of the pass transistor, so that 723 has to provide only the base current

So $$I_{Load} = \beta_{pass\ transistor} \times I_{O(723)}$$

Switching Regulator:

Limitations of series Regulator:

1) The input step down transformer is bulky
2) large values of filter capacitors are required to decrease the ripple
3) The Efficiency of series Regulator is very low.



Fig(a): Pulse width modulation and average value.

Switced mode power supplies overcome these difficulties ① The switching regulator, also called switched mode regulator operates as "Controlled switch". It operates in two modes a) saturation mode b) cut-off mode.

2) the power transmitted across the pass device is in discrete pulses rather than as a steady current flow. So it dissipates no power. Hence Efficiency is high.

switching mode regulators rely on pulse width modulation to control the average value of the output voltage. the average value of the repetitive pulse

waveform depends on the area under the waveform. If the duty cycle is varied as shown in fig(a), the average value of the voltage changes proportionally.

A switching power supply is shown in fig(b). the bridge rectifier and capacitor filters are connected directly to the ac line to give unregulated dc input. the thermistor R_t limits the high initial capacitor charge current. the reference regulator is a series pass regulator. its output is a regulated reference voltage V_{ref} which serves as a power supply voltage for all other circuits.

Transistors Q_1 and Q_2 are alternately switched off an on at 20 KHz. these transistors are either fully on or cut-off, so they dissipate very little power these transistors drive the primary of the main transformer. the secondary is centre tapped and full wave rectification is achieved by diodes D_1 and D_2. this unidirectional square wave is next filtered through a two stage LC filter to produce output voltage V_o.

The regulation of V_o is achieved by the feedback circuit consisting of a pulse width modulation and and steering logic circuit. the output voltage V_o is sampled by a R_1R_2 divider and a fraction $\frac{R_1}{R_1+R_2}$ is

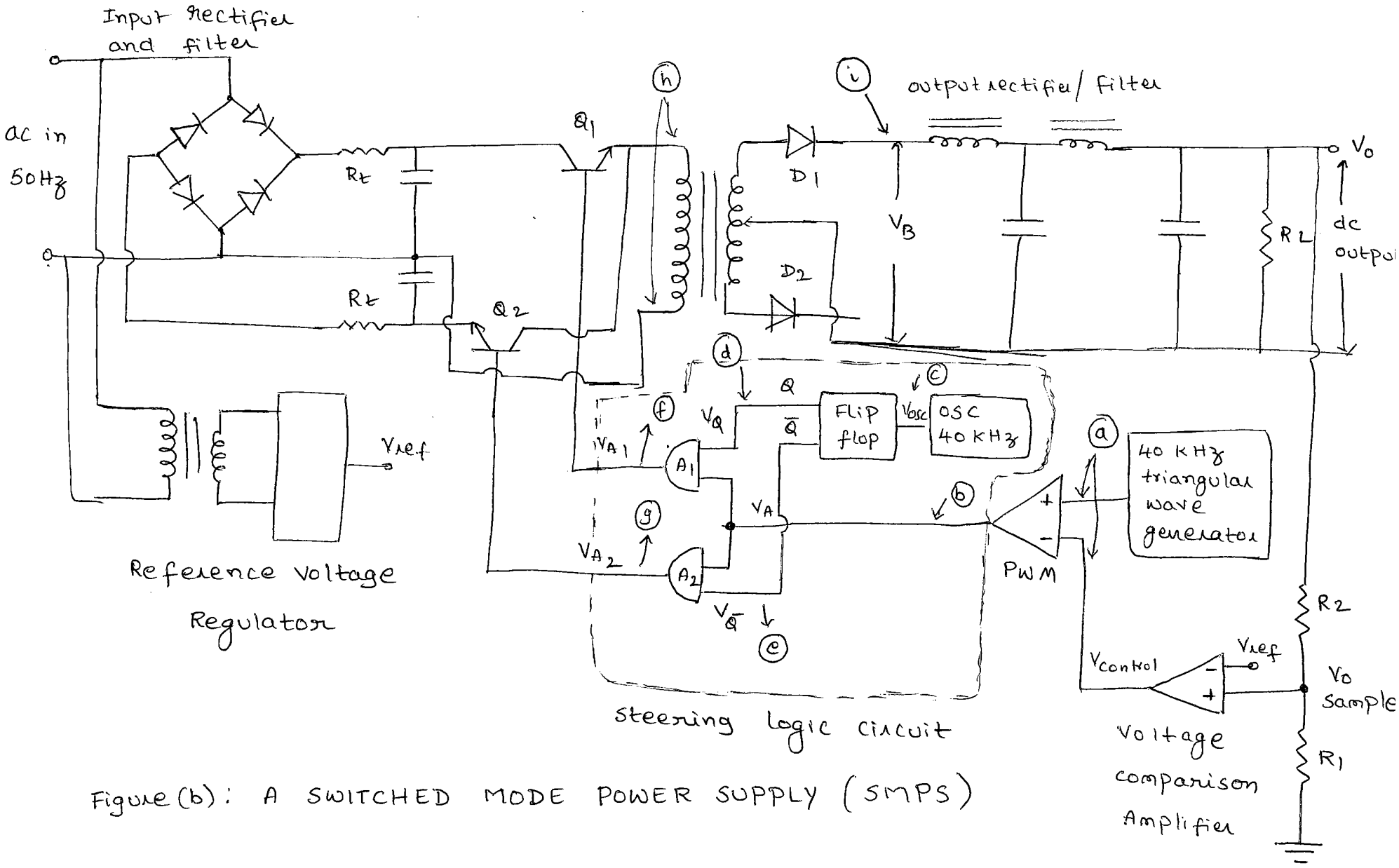
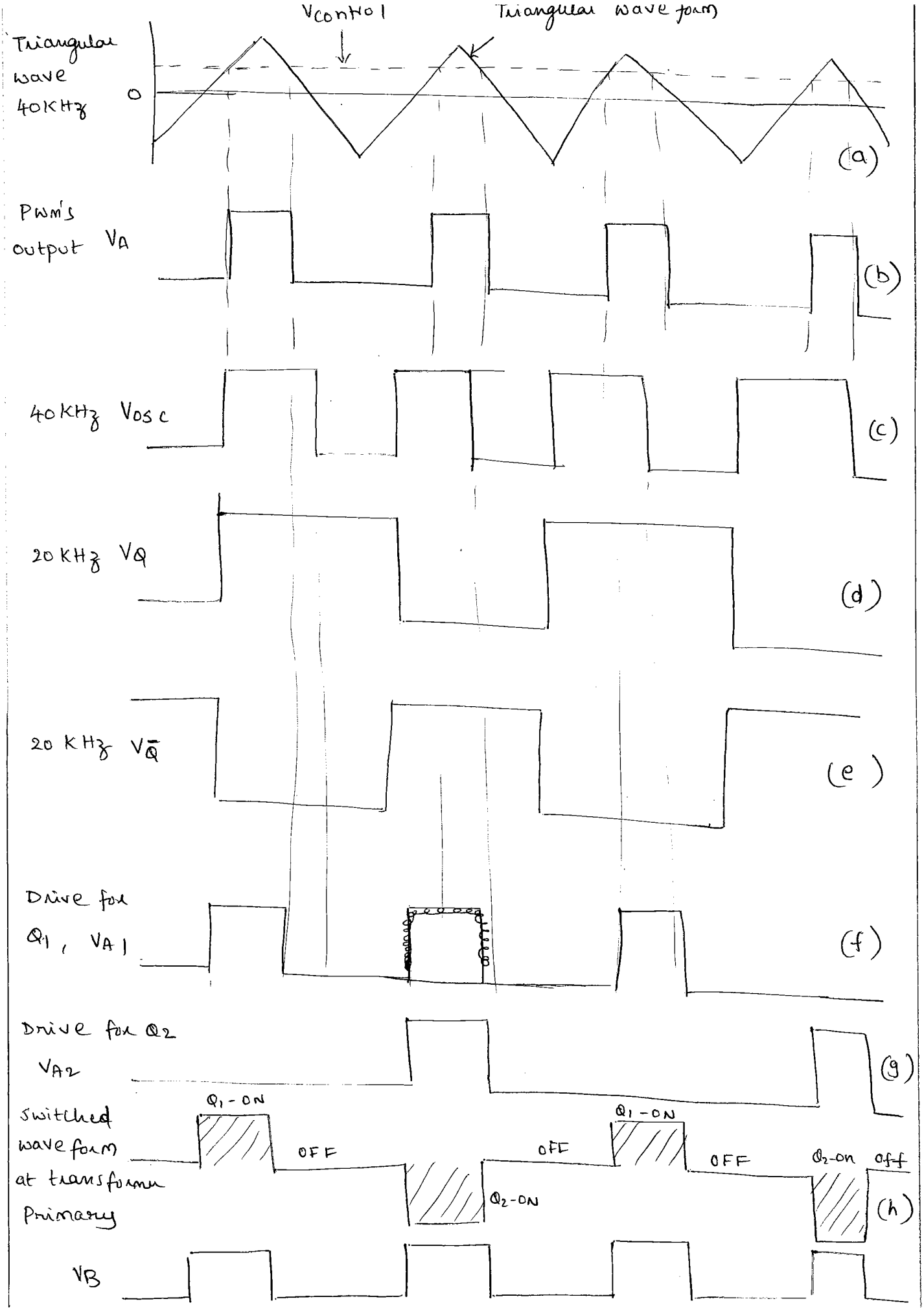


Figure (b): A SWITCHED MODE POWER SUPPLY (SMPS)


Vcontrol
Triangular wave form
Triangular wave 40KHz
0
(a)
PWM's output VA
(b)
40KHz Vosc
(c)
20KHz VQ
(d)
20KHz VQ̄
(e)
Drive for Q1, VA1
(f)
Drive for Q2
VA2
(g)
Switched wave form at transformer Primary
Q1 - ON
OFF
Q2-ON
Q1 - ON
OFF
Q2-on
off
(h)
VB

compared with a fixed reference voltage V_{ref} in comparator 1. The output of this voltage comparison amplifier is called $V_{control}$ and is as shown in fig(b) $V_{control}$ is applied to the (-) input terminal of comp2 and a triangular waveform of frequency 40KHz is applied at the (+) input terminal. It may be noted that high frequency triangular waveform is being used to reduce the ripple.

The comparator 2 functions as a pulse width modulator and its output is a square wave V_A. The duty cycle of the square wave is $T_1/(T_1+T_2)$ and varies with $V_{control}$ which inturn varies with the variation of V_o

The output V_A drives a steering logic circuit It consists of a 40KHz oscillator cascaded with a flipflop to produce two complementary outputs V_Q and $V_{\bar{Q}}$ shown in fig (d) and (e). The output V_{A_1} and V_{A_2} of AND gates A_1 and A_2 are shown fig (f) and (g). These waveforms are applied at the base of transistor Q_1 and Q_2. Depending upon whether transistor Q_1 or Q_2 is on, the waveform at the inpot of the ~~transistor~~ transformer will be a square wave as shown in fig(h) The rectified output is shown in fig(i).

If there is a rise in dc output voltage V_o, the $V_{control}$ of the comparator 1 also rises. This changes the

intersection of the $V_{control}$ with the triangular wave form and in this case decreases the time period T_1 in the waveform of fig(b). This in turn decreases the pulse width of the waveform driving the main power transformer. Reduction in pulse width lowers the average value of the dc output V_o. Thus initial rise in the dc output voltage has been nullified.

555 Timer

Introduction:

In most of the industries, operations are scheduled according to specific time requirements. In process industry, raw material is processed in different stages. In each stage raw material is processed for a particular time period. For example process may be the heating process and the heat may be required for say, 5 minutes. There are number of applications where event must be delayed for specific delay periods. For example, one can snap by setting proper time period in automatic cameras.

To achieve these requirements, an electronic circuitary which is used to generate time delays. the 555 timer is a highly stable device for generating accurate time delay or oscillation.

Features:

* A single 555 timer can provide time delay ranging from microseconds to hours where as counter timer can have a maximum timing range of days.
* the 555 timer can be used with supply voltage in the range of +5V to +18V and can drive

load up to 200mA.

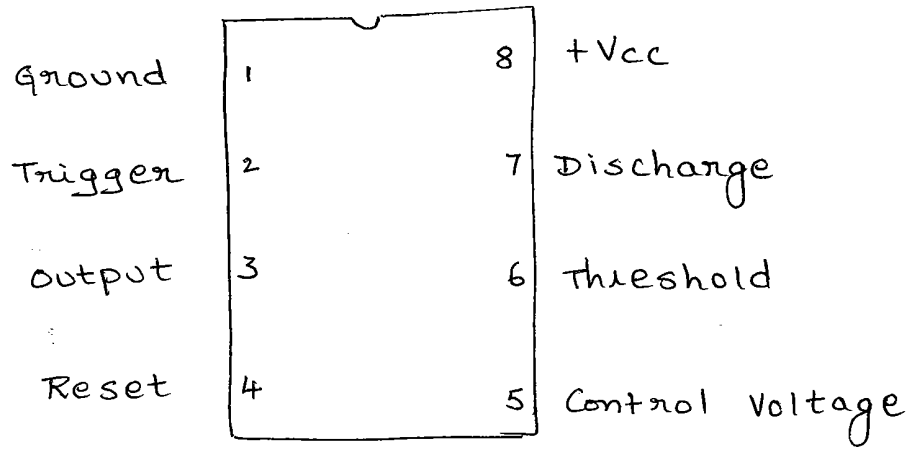
* It is compatible with both TTL and CMOS logic circuits.
* Because of the wide range of supply voltage, the 555 timer is versatile and easy to use in various applications.

Applications:

1. oscillator 2. pulse Generator
3. Ramp and square wave Generator
4. mono shot multivibrator 5. Burglar Alarm
6. Traffic light Control 7. Voltage Monitor.

Functional Block diagram of IC 555:

The figure below shows the pin diagram and the block diagram of the IC NE 555 timer. This is 8 pin IC timer.



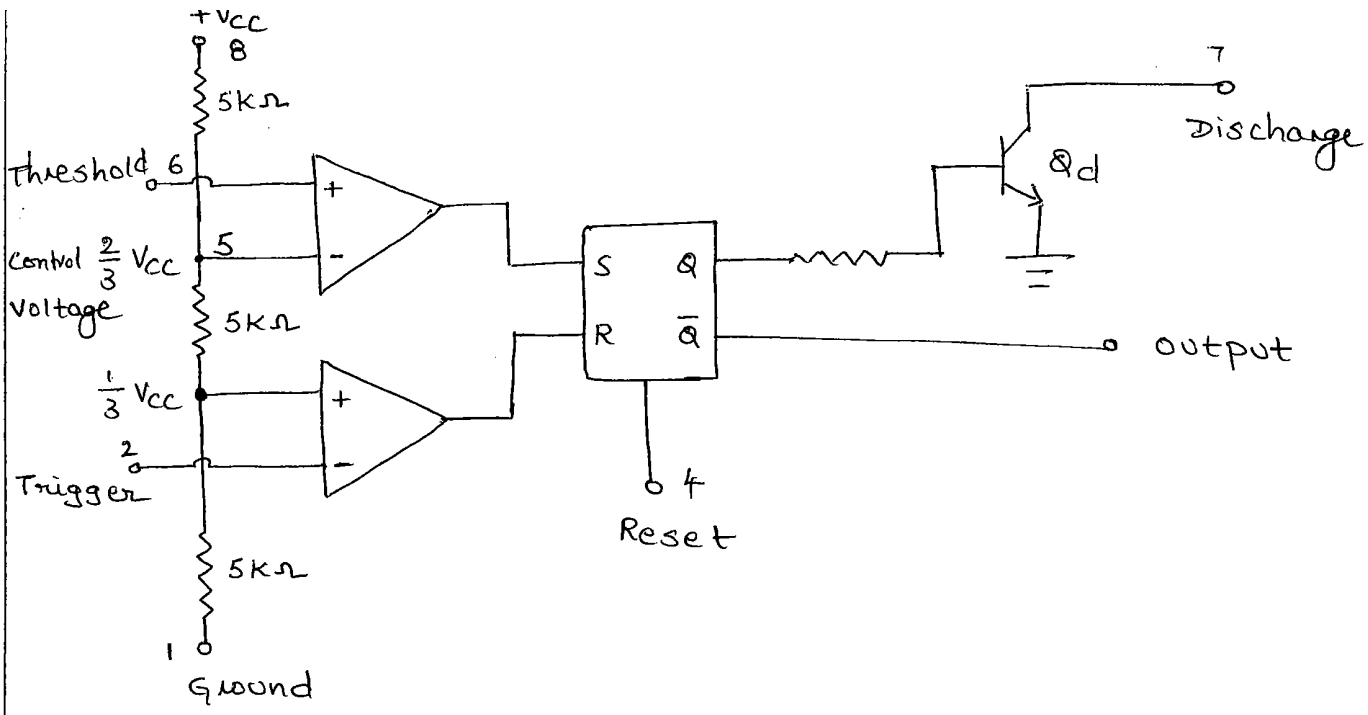
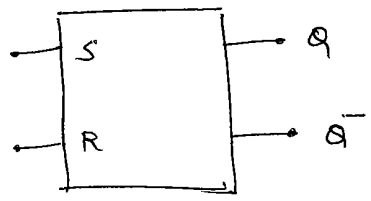


Fig: Block diagram IC 555 timer

Functions of Pins

Pin 1 : Ground : All the voltages are measured with respect to this terminal.

Pin 2 : Trigger : the IC 555 uses two comparators the voltage divider consists of three equal resistances. Due to voltage divider, the voltage of non inverting terminal of comparator 2 is fixed at $\frac{Vcc}{3}$. the inverting input of comparator 2 which is compared with $\frac{Vcc}{3}$. when the trigger input is slightly less than $Vcc/3$, the comparator 2 output goes high. This output is given to reset input of R-S flip flop. So high output of comparator 2 resets the flip flop.



S	R	output (Q)	Remark
0	0	NC	No change in output state
0	1	0 (low)	flip flop resets
1	0	1 (High)	Flip flop sets
1	1	*	Not used.

Pin 3 : output : The complementary signal output ($\bar{Q}$) of the flip flop goes to pin 3 which is the output. The load can be connected in two ways. one between 3 and ground while other between 3 and pin 8.

Pin 4 : Reset : This is an interrupt to the timing device. when pin 4 is grounded, it stops the working of device and makes it off. Thus pin 4 provides on/off feature to the IC 555.

Pin 5 : Control Voltage input : This pin is nothing but the inverting input terminal of Comparator 1. The voltage divider holds the voltage of this input at $\frac{2}{3}$ Vcc. This is reference level for Comparator 1 with which threshold is compared.

Pin 6 : Threshold : This is the non-inverting input terminal of Comparator 1.

For threshold $> \frac{2}{3} V_{cc}$, flip flop → set, Q →: high, output at pin 3 → low

For trigger $< \frac{1}{3} V_{cc}$, flip flop → reset, Q → low, output at pin 3 → high.

Pin 7 : Discharge : This pin is connected to the collector of the discharge transistor Q_d. When the output is high, the Q is low and transistor Q_d is off. It acts as an open circuit to the external capacitor C to be connected across it, so capacitor C can charge.

When output is low, Q is high which drives the base of Q_d high, driving transistor Q_d in saturation. It acts as short circuit, shorting the external capacitor C to be connected across it.

Pin 8 : Supply $+V_{cc}$: the IC 555 timer can work with any supply voltage between 4.5 V and 18V

Monostable Multivibrator using IC 555

The IC 555 timer can be operated as a monostable multivibrator by connecting an external resistor and a capacitor as shown in figure below.

The circuit has only one stable state. When trigger is applied, it produces a pulse at the

output and return back to its stable state. the duration of the pulse depends on the values of R and C. As it has only one stable state, it is called one shot multivibrator.

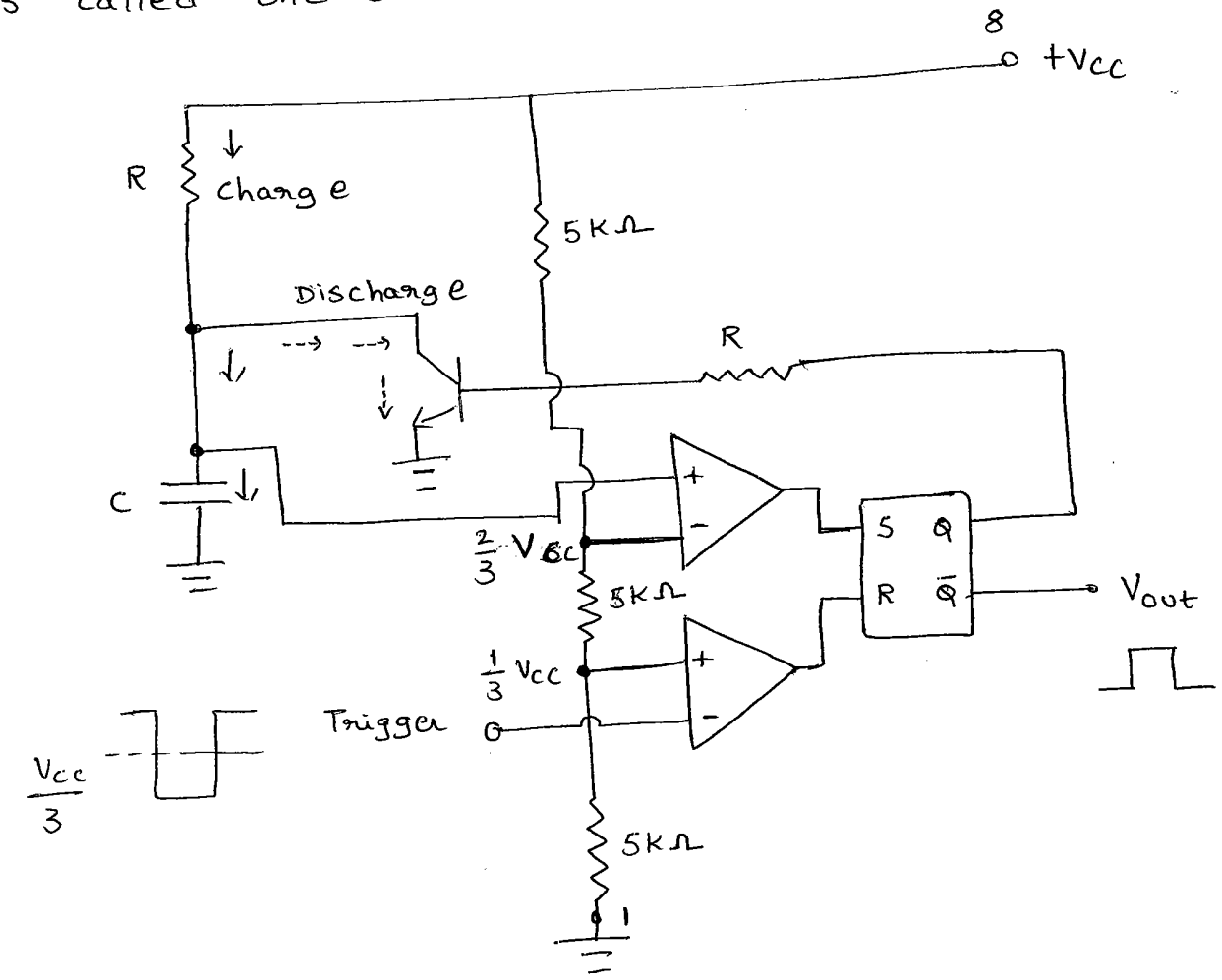


Fig: monostable operation of 555

operation:

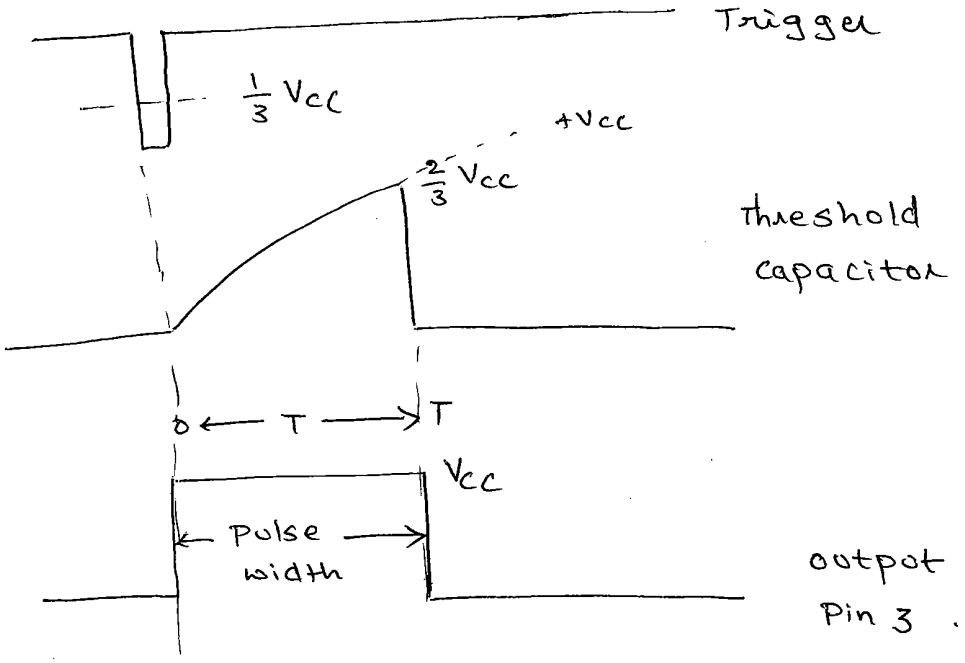
The flip flop is initially set ie Q is high. The drives the transistor Qd in saturation. The capacitor discharges completely and voltage across it is nearly zero. the output at pin 3 is low.

when a trigger input, a low going pulse is applied, the circuit state remains unchanged till trigger voltage is greater than $\frac{1}{3}$ Vcc. when it

less than $\frac{1}{3}V_{cc}$, then comparator 2 output goes high. this resets the flip flop so Q goes low and $\bar{Q}$ goes high. low Q makes the transistor Qd off. Hence capacitor starts charging through resistance R as shown by dark arrows.

the voltage across capacitor increases exponentially this voltage is nothing but the threshold voltage at pin 6. when this voltage becomes more than $\frac{2}{3}V_{cc}$, then comparator 1 output goes high. This sets the flip flop ie. Q becomes high and $\bar{Q}$ low. this high Q drives the transistor Qd in saturation. Thus capacitor C quickly discharges through Qd as shown by dotted arrows.

so it can be noted that V_{out} at pin 3 is low at start, when trigger is less than $\frac{1}{3}V_{cc}$ it becomes high and when threshold is greater than $\frac{2}{3}V_{cc}$ again becomes low, till next trigger pulse occurs so a rectangular wave is produced at the output. the pulse width of this rectangular pulse is controlled by the charging time of capacitor. this depends on the time constant RC. Thus RC controls the pulse width. The waveforms are shown in the figure below.



Derivation of pulse width:

The voltage across capacitor increases exponentially and is given by

$$V_c = V_f - (V_f - V_{ini})\, e^{-t/RC}$$

Here $V_{ini} = 0$, $V_f = V_{cc}$

$$\therefore \quad V_{c} = V_{cc}\left(1 - e^{-t/RC}\right)$$

At $t = T$, $V_c = \frac{2}{3} V_{cc}$

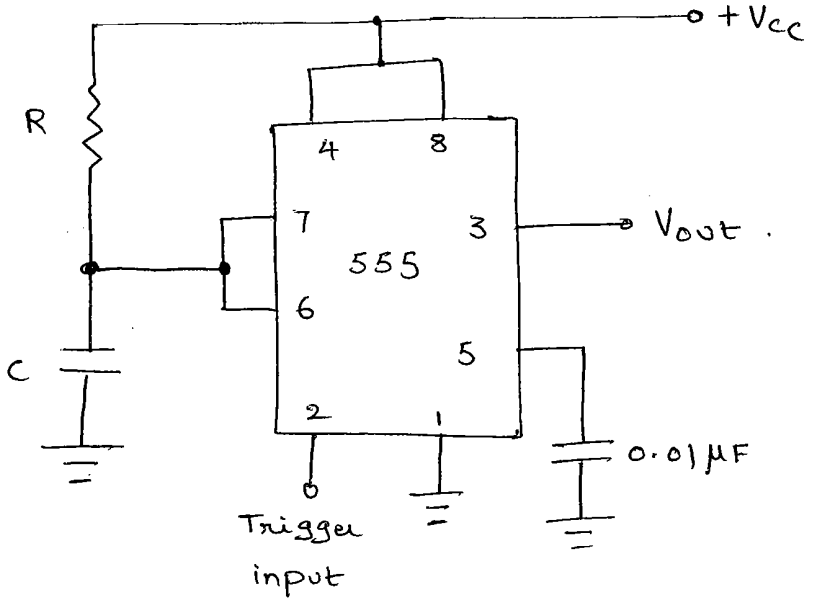
$$\therefore \quad \frac{2}{3} V_{cc} = V_{cc}\left(1 - e^{-T/RC}\right)$$

$$T = 1.1\, RC$$

thus the pulse width T is given by

$$\boxed{T = 1.1\, RC}$$

Schematic Diagram:



Applications of IC 555 timer in Monostable Mode:

1. Frequency Divider:

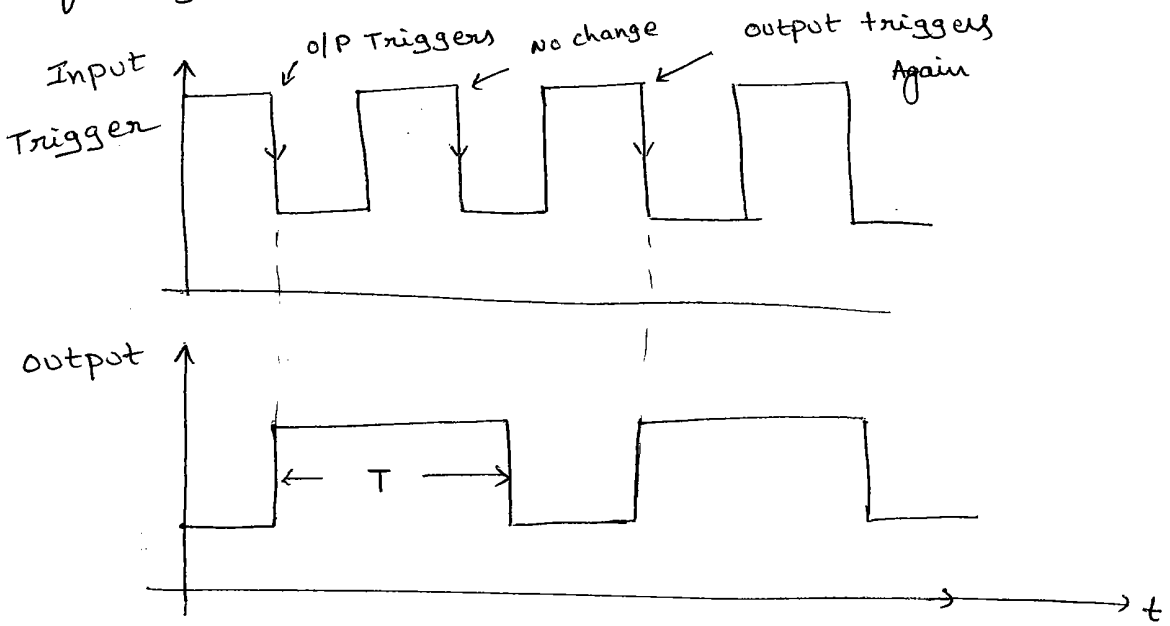


Fig: Frequency divider circuit.

A continuosly triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal. The monostable multivibrator will be

triggered by the first negative going edge of the square wave input signal. but the output will remain high for next negative going edge of the input square wave as shown in figure above. The monoshot will however be triggered on the third negative going input depending on the choice of time delay. In this way the output can be made integral fractions of the frequency of the input triggering square wave.

2. Missing pulse detector:

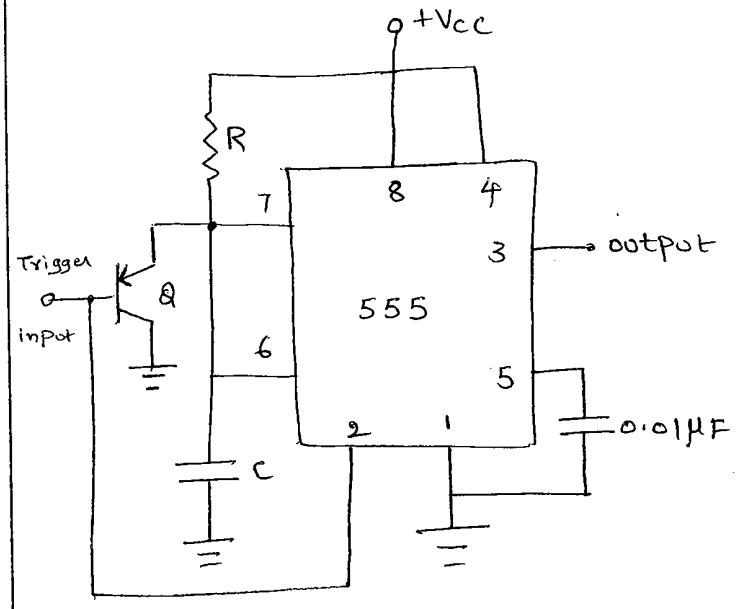


Fig: A missing pulse detector monostable circuit.

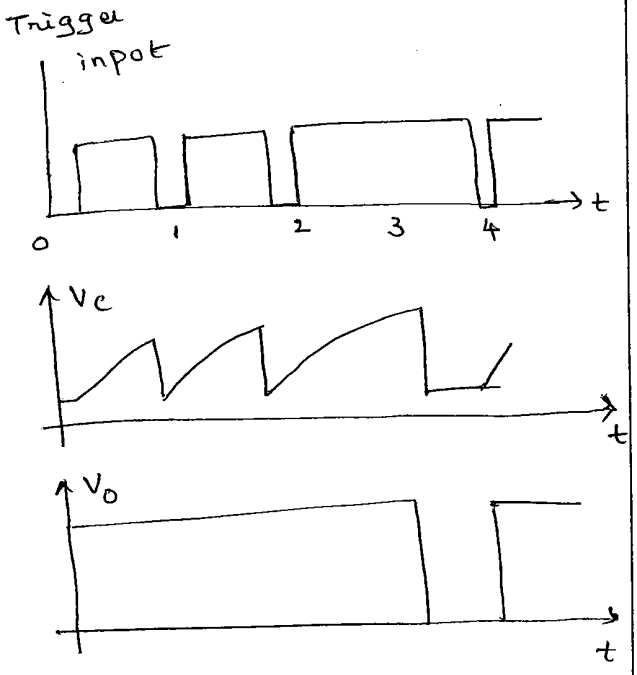


Fig: Output of Missing pulse detector.

Missing pulse detector circuit using 555 timer is shown in figure above. whenever, input trigger is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (~0.7V). The output of the timer goes high.

The circuit is designed so that the time period

of the monostable circuit is slightly greater ($\frac{1}{3}$ longer) than that of the triggering pulses. So long the trigger pulse train keeps coming at pin 2, the output remains High. However, if a pulse misses, the trigger input is high and transistor Q is cut-off. The 555 timer enters in to normal state of monostable operation.

The output goes low after time T of the mono shot. Thus this type of circuit can be used to detect missing heart beat. It can also be used for speed control and measurement.

3. Linear Ramp Generator :

Linear ramp can be generated by the circuit shown in figure. The resistor R of the monostable circuit is replaced by a constant current source.

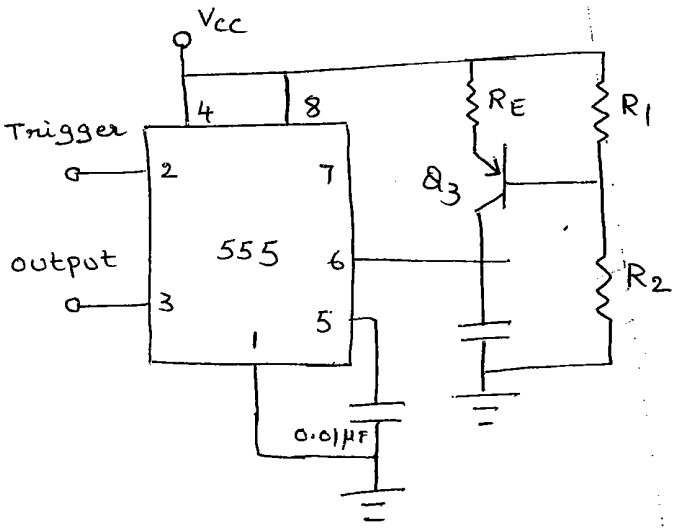


Fig: Linear Ramp Generator.

The capacitor is charged linearly by the constant current source formed by the transistor Q_3. The capacitor voltage V_c can be written as

$$V_c = \frac{1}{C}\int_0^t i\,dt \longrightarrow (1)$$

where i is the current supplied by the constant current source. Further the KVL equation can be written as

$$\frac{R_1}{R_1+R_2} V_{CC} - V_{BE} = (\beta+1) I_B R_E \simeq \beta I_B R_E = I_C R_E = i R_E \longrightarrow (2)$$

where I_B, I_C are the base current and collector current respectively, β is the current amplification factor in CE-mode and is very high. therefore.

$$i = \frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{R_E (R_1+R_2)} \longrightarrow (3)$$

Now putting the value of the current i in eq (1), we get

$$V_C = \frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{C R_E (R_1+R_2)} + t$$

At time $t = T$, the capacitor voltage V_c becomes $\frac{2}{3} V_{CC}$, then we get

$$\frac{2}{3} V_{CC} = \frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{R_E (R_1+R_2) C} \times T$$

$$\text{Now} \quad T = \frac{\left(\frac{2}{3}\right) V_{CC} R_E (R_1+R_2) C}{R_1 V_{CC} - V_{BE}(R_1+R_2)} \longrightarrow (4)$$

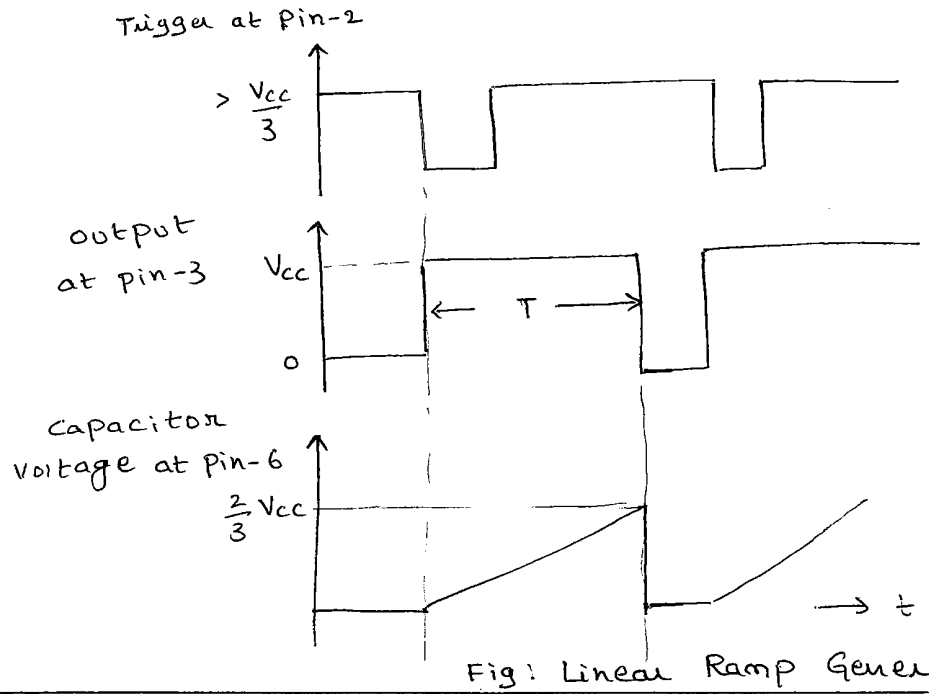
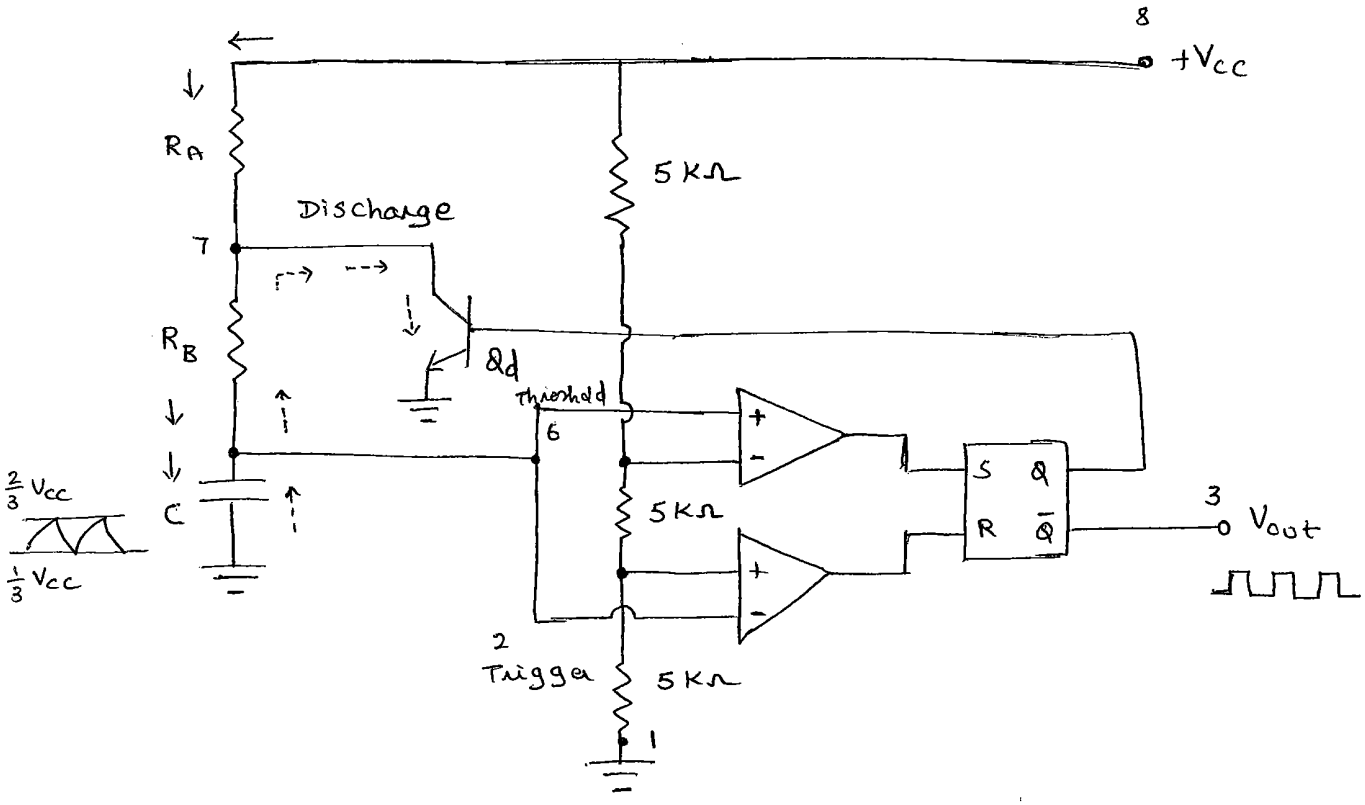


Fig: Linear Ramp Generator output.

the capacitor discharges as soon as its voltage reaches $\frac{2}{3}V_{CC}$ which is the threshold of the upper comparator in the monostable circuit functional diagram. The capacitor voltage remains zero till another trigger is applied. The waveforms are shown in the figure above.

Astable Multivibrator using IC 555 :



The figure above shows the IC 555 connected as an astable multivibrator. The threshold input is connected to the trigger input. Two external resistances R_A, R_B and the capacitor C is used in the circuit.

The circuit has no stable state. The circuit changes its state alternately. Hence the operation is also called free running nonsinusoidal oscillator.

operation: when the flip flop is set, Q is high which drives the transistor Q_d in saturation and the capacitor

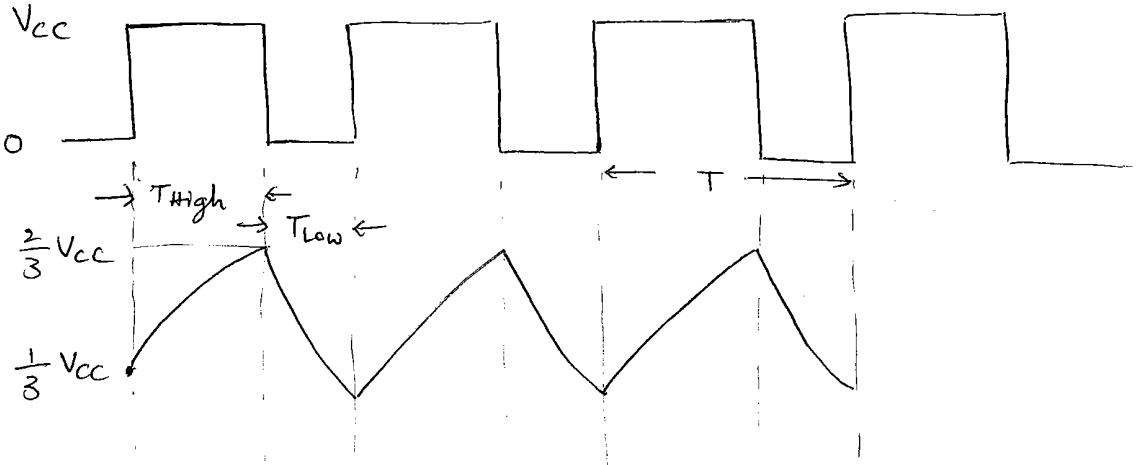
gets discharged. Now the capacitor voltage is nothing but the trigger voltage. So while discharging, when it becomes less than $\frac{1}{3}V_{cc}$, comparator 2 output goes high. This resets the flip-flop hence Q goes low and $\bar{Q}$ goes high.

The low Q makes the transistor off. Thus capacitor starts charging through the resistances R_A, R_B and C. The charging path is shown by thick arrows in above figure. As total resistance in the charging path is $(R_A + R_B)$, the charging time constant is $(R_A + R_B)C$.

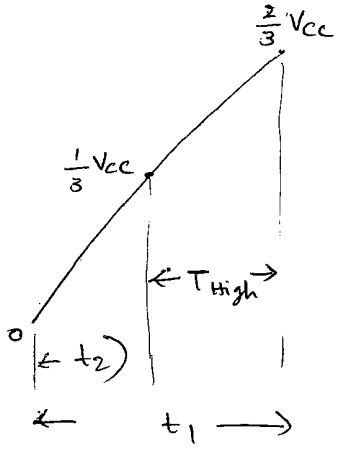
Now the capacitor voltage is also a threshold voltage, while charging, capacitor voltage increases ie the threshold voltage increases. When it exceeds $\frac{2}{3}V_{cc}$, then the comparator 1 output goes high which sets the flip flop. The flip flop output Q becomes high and output at pin 3 ie. $\bar{Q}$ becomes low. High Q drives transistor Qd in saturation and capacitor starts discharging through resistance R_B and transistor Qd. This path is shown by dotted arrows in above figure. Thus the discharging time constant is $R_B C$. When capacitor voltage becomes less than $\frac{1}{3}V_{cc}$, comparator 2 o/p goes high, resetting the flip flop. This cycle repeats.

Thus when capacitor is charging, output is high while when it is discharging the output is low. The output is a rectangular wave. The capacitor voltage is exponentially

rising and falling. The waveforms are shown in figure below.



The time t_1 taken by the circuit to charge from 0 to $\frac{2}{3}V_{cc}$ is



$$V_c = V_f - (V_f - V_{ini})\, e^{-t/RC}$$

$V_f = V_{cc}$, $V_{ini} = 0$

$$V_c = V_{cc} - (V_{cc} - 0)\, e^{-t/RC}$$

$$V_c = V_{cc}\left(1 - e^{-t/RC}\right)$$

when $t = t_1$, $V_c = \frac{2}{3}V_{cc}$

$$\frac{2}{3}V_{cc} = V_{cc}\left(1 - e^{-t_1/RC}\right)$$

$$t_1 = 1.09\ RC$$

Ily when $t = t_2$, $V_c = \frac{1}{3}V_{cc}$

$$\frac{1}{3}V_{cc} = V_{cc}\left(1 - e^{-t_2/RC}\right)$$

$$t_2 = 0.405\ RC$$

$$\therefore \quad T_{High} = t_1 - t_2 = 1.09RC - 0.405\ RC$$

$$T_{High} = 0.69\ RC = 0.69(R_A + R_B)C \quad \rightarrow (1)$$

the output is low while the capacitor discharges from $\frac{2}{3} V_{cc}$ to $\frac{1}{3} V_{cc}$ and the voltage across the capacitor is given by

$$V_c = V_f - (V_f - V_{ini}) e^{-t/RC}$$

$$V_{ini} = \frac{2}{3} V_{cc} \quad , \quad V_f = 0$$

$$V_c = 0 - \left(0 - \frac{2}{3} V_{cc}\right) e^{-t/RC}$$

At $t = T_{Low}$ $\quad V_c = \frac{1}{3} V_{cc}$

$$\frac{1}{3} V_{cc} = \frac{2}{3} V_{cc} \, e^{-T_{Low}/RC}$$

$$T_{Low} = 0.69 RC = 0.69 R_B C$$

$$T = T_{High} + T_{Low}$$

$$T = 0.69 (R_A + 2R_B) C$$

$$f = \frac{1}{T} = \frac{1.45}{0.69 (R_A + 2R_B) C}$$

In the circuit, when the transistor Q_1 is ON, the output goes low. Hence

$$\% \text{ Duty cycle} = \frac{T_{Low}}{T} \times 100$$

$$\% \text{ Duty cycle} = \frac{R_B}{R_A + 2R_B} \times 100$$

$$\% D = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100$$

Applications of 555 timer in Astable Mode

1) FSK Generator:

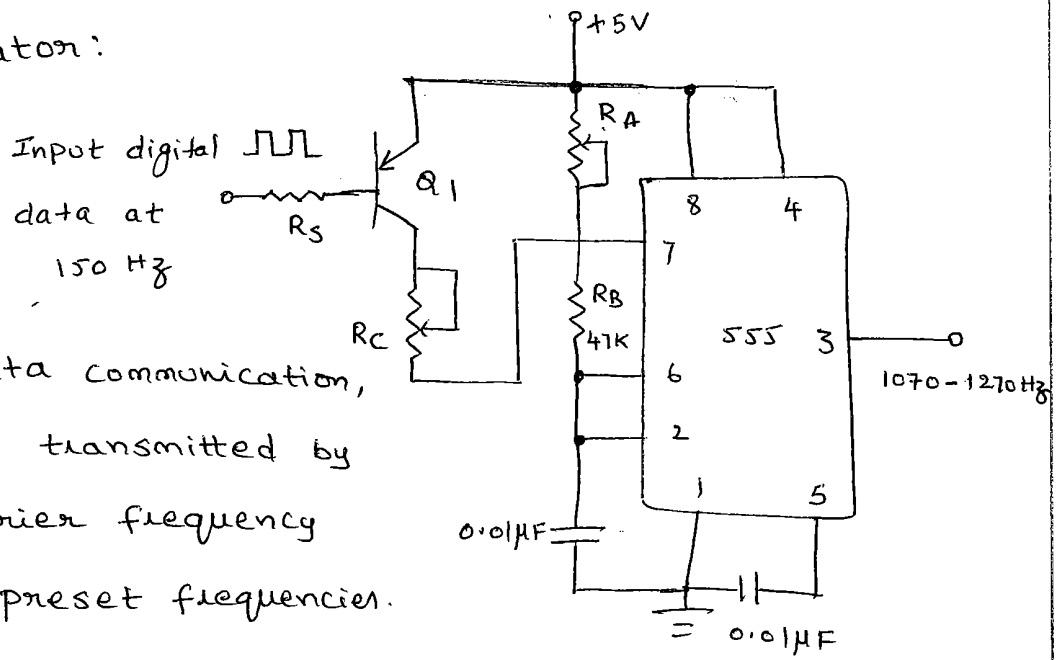


Fig: FSK Generator

In digital data communication, binary code is transmitted by shifting a carrier frequency between two preset frequencies. This type of transmission is called frequency shift keying (FSK) technique.

A 555 timer in astable mode can be used to generate FSK signal. The circuit is shown in figure above. The standard digital data input frequency is 150Hz. when input is high, transistor Q is off and 555 timer works in the normal astable mode of operation. The frequency of the output wave form is given by

$$f_0 = \frac{1.45}{(R_A + 2R_B)C}$$

In a tele-type writer using a modulator-demodulator (MODEM), a frequency between 1070Hz to 1270 Hz is used as one of the standard FSK signals. the components R_A, R_B and the capacitor C can be selected so that f_0 is 1070 Hz

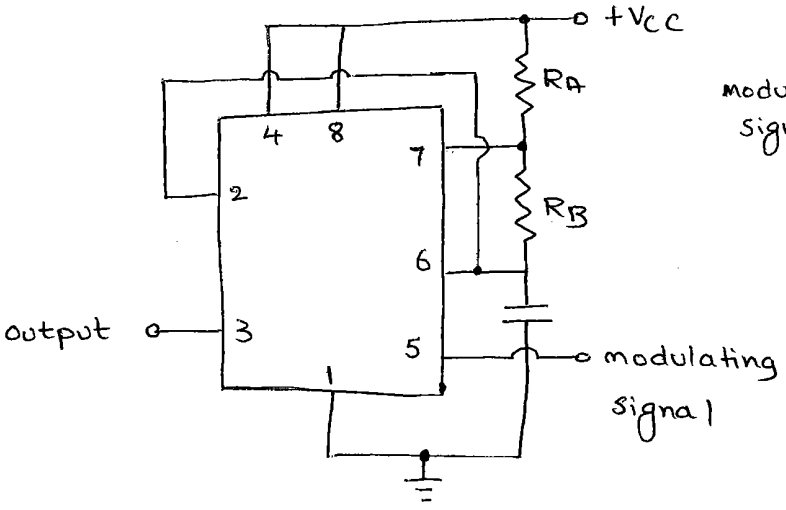
when the input is low, Q goes on and connects the resistance R_C across R_A. The output frequency is now given by

$$f_o = \frac{1.45}{(R_A || R_C) + 2R_B}$$

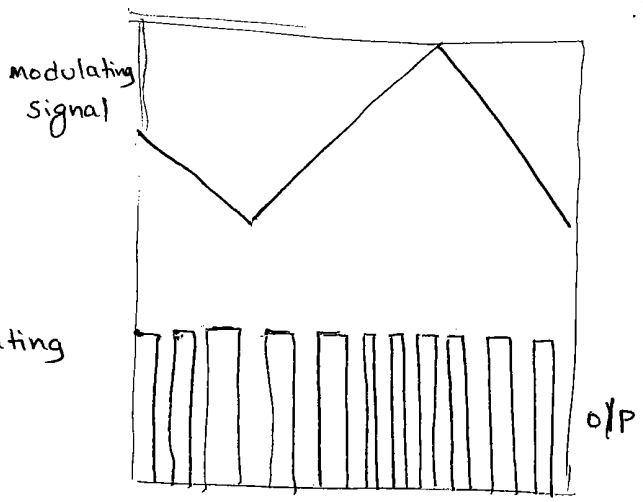
The resistance R_C can be adjusted to get an output frequency 1270 Hz.

d) Pulse position Modulator:

The pulse position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation as shown in figure below. The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.



Fig(a) Pulse position modulator



Fig(b): Pulse position modulator output

Fig(b) shows the output waveform generated for a triangular wave modulation signal. It may be noted that from the output waveform that the frequency is varying leading to Pulse Position Modulation.

Schmitt trigger using 555 timer:

The use of 555 timer as a schmitt trigger is shown in fig. Here the two internal comparators are tied together and externally biased at $\frac{V_{cc}}{2}$ through R_1 and R_2.

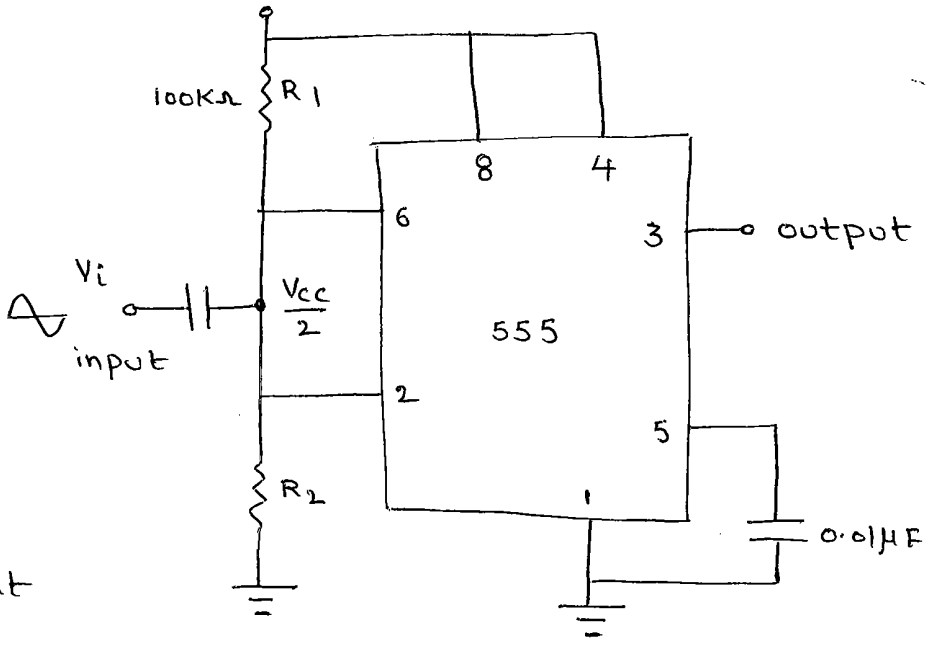
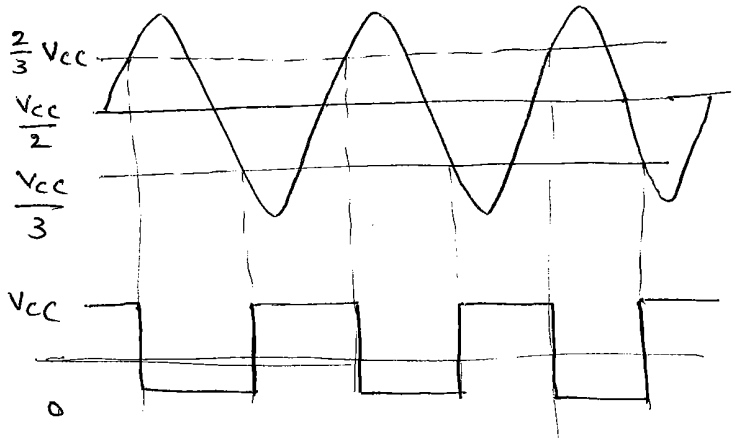


Fig: Timer in schmitt trigger operation.

Since the upper comparator will trip at $\frac{2}{3}V_{cc}$ and lower comparator at $\frac{1}{3}V_{cc}$, the bias provided by R_1 and R_2 is centered with in these two thresholds.

Thus a sine wave of sufficient amplitude $> \frac{V_{cc}}{6}$ $\left(\text{ie } \frac{2}{3}V_{cc} - \frac{V_{cc}}{2}\right)$ to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave output as shown in figure (b).



(Fig b): Input and output waveforms of schmitt trigger.

phase - Locked Loops

Introduction: A phase locked loop is basically a closed loop system designed to lock the output frequency and phase to the frequency and phase of an input signal. It is commonly abbreviated as PLL. Now with the advanced Ic technology, PLL's are available as inexpensive monolithic Ic's. They are used in applications such as frequency synthesis, frequency modulation/ demodulation, AM detection, tracking filters, FSK demodulator, tone detector etc.

Basic principle and operation of PLL:

The basic block schematic of the PLL is shown in figure below.

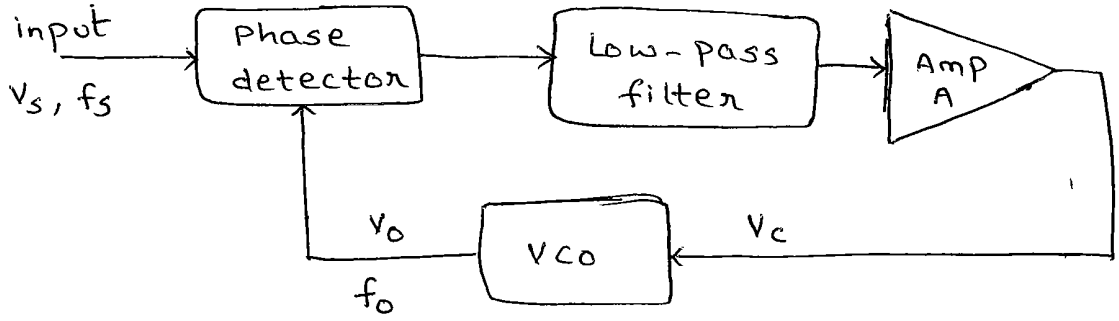


Fig: Block schematic of PLL

This feedback system consists of

1. phase detector/ comparator
2. Low pass filter
3. An Error Amplifier
4. A Voltage controlled Oscillator (VCO)

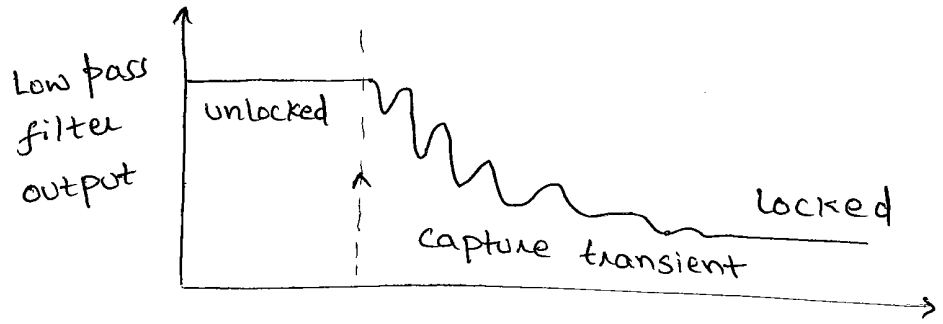
The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency (f_o). This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage V_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called voltage Controlled oscillator or in short VCO.

If an input signal V_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output V_o of the VCO.

If the two signals differ in frequency/phase, an error voltage V_e is generated. The phase detector is basically a multiplier and produces the sum $f_s + f_o$ and difference $f_s - f_o$ components at its output. The high frequency component $f_s + f_o$ is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage V_c to VCO. The signal V_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. Once this action starts, we say that the signal is in the capture range.

The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ. this phase difference ϕ generates a corrective control voltage V_c to shift the VCO frequency from f_o to f_s and thereby maintain the lock. once locked, PLL tracks the frequency changes of the input signal. thus, a PLL goes through three stages. i) free running ii) capture and iii) locked or tracking.

Figure below shows the capture transient.



the capture transient

As capture starts, a small sine wave appears. this is due to the difference frequency between the VCO and the input signal. the dc component of the beat drives the VCO towards lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency.

the difference in frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further. the process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat (f_{diff}) frequency will be too high to pass through the filter and the PLL will not respond. we can say that the signal is out of the capture band.

However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus lock range is always larger than the capture range.

Some important definitions related to PLL.

1) Lock-in range: once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range.

The lock range is usually expressed as a percentage of f_0.

Capture Range: The range of frequencies over which PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of fo.

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the over all loop gain and loop filter characteristics.

PHASE DETECTOR

The phase detection is the most important part of the PLL system. There are two types of phase detectors used ① Analog ② Digital.

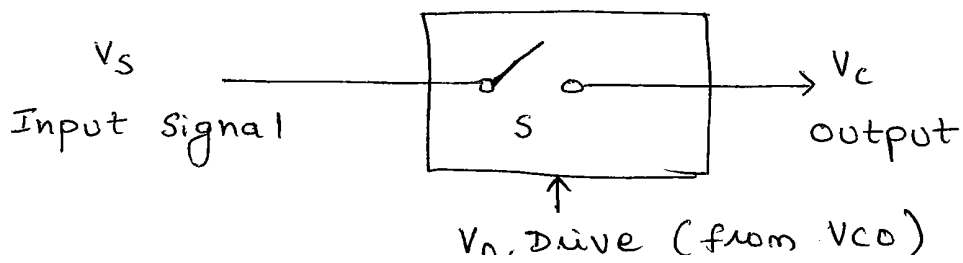
1) Analog phase detector

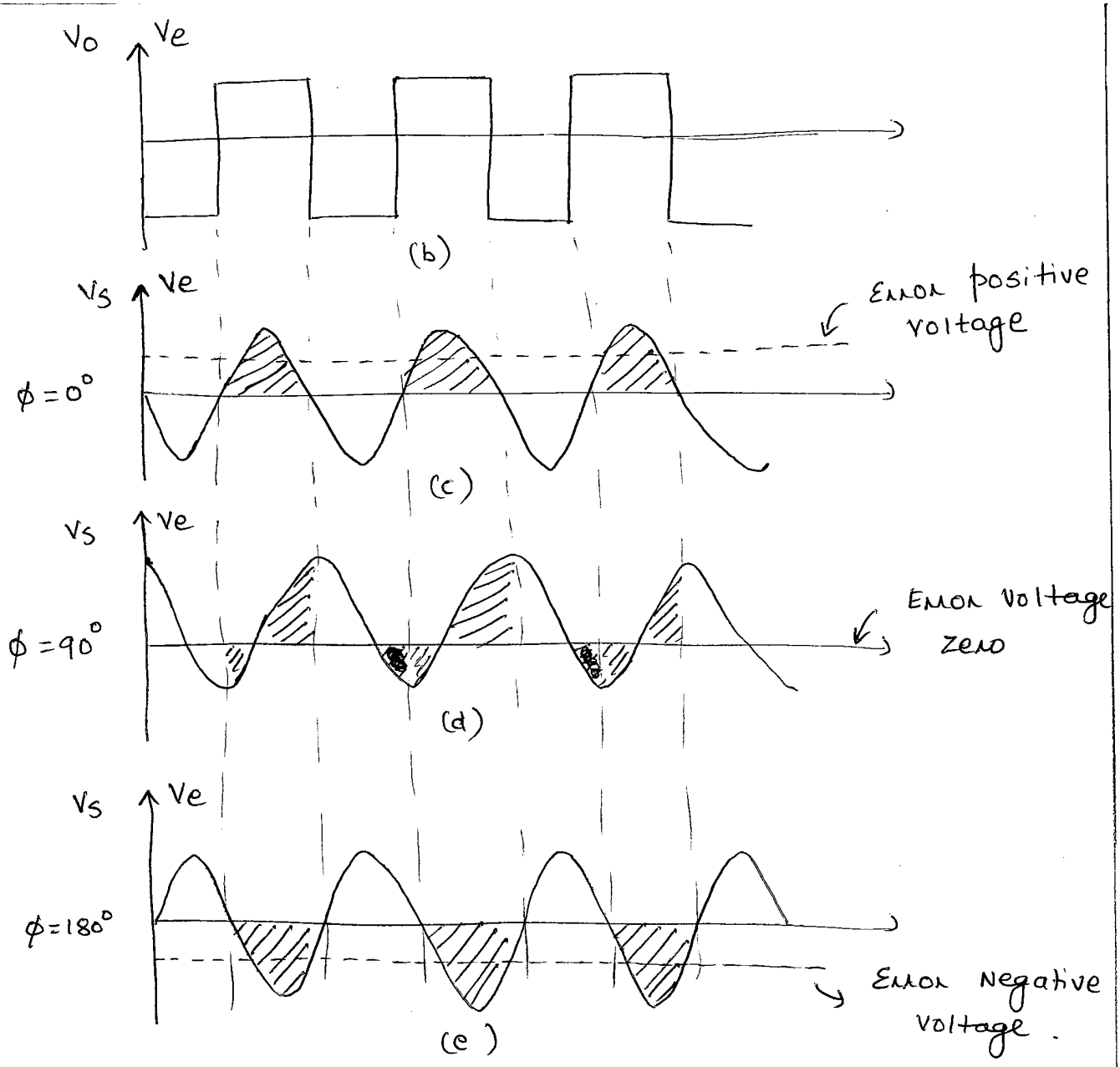
a) Analog phase detector using electronic switch

b) Analog phase detector using balanced modulator

a) Analog phase detector using Electronic switch:

The principle of analog phase detection using switch type phase detector is shown in figure below.





(b) VCO output wave form.

Input and output (Hatched) wave form of phase detector for (c) $\phi = 0$ (d) $\phi = 90^\circ$ (e) $\phi = 180^\circ$.

An electronic switch S is opened and closed by signal coming from VCO (normally a square wave) the input signal is therefore chopped at a repetition rate determined by VCO frequency.

Figure (e) shows the input signal V_s assumed to be in phase ($\phi = 0^\circ$) with VCO output V_o.

Since the switch S is closed only when VCO output is positive, the output wave form V_e will be half sinusoids. similarly, the output wave form for $\phi = 90^\circ$ and $\phi = 180^\circ$ is shown in fig (d) and figle).

This type of phase detector is called a Half wave detector, since the phase information for only one half of the input wave form is detected and averaged.

The output of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output wave form shown by a dotted line.

It may be seen that error voltage is zero when the phase shift between the two inputs is 90°. so for perfect lock, the VCO output should be 90° out of phase with respect to the input signal.

Analysis:

A phase comparator is basically a multiplier which multiplies the input signal by the VCO signal

$$V_s = V_s \sin 2\pi f_s t \quad , \quad V_o = V_o \sin (2\pi f_o t + \phi)$$

Then the phase comparator output is

$$V_e = K V_s V_o \sin 2\pi f_s t \sin (2\pi f_o t + \phi) \longrightarrow (1)$$

where K → phase comparator gain

and ϕ is the phase shift between the input signal and the VCO output. Eq ① can be simplified as

$$V_e = \frac{K V_s V_o}{2}\left[\cos\left(2\pi f_s t - 2\pi f_o t - \phi\right) - \cos\left(2\pi f_s t + 2\pi f_o t + \phi\right)\right]$$

when at lock ie. $f_s = f_o$

$$\text{then } V_e = \frac{K V_s V_o}{2}\left[\cos(-\phi) - \cos\left(2\pi \times 2 f_o t + \phi\right)\right]$$

this shows that the phase comparator output contains a double frequency term and a dc term $(K V_s V_o/2)\cos\phi$ which varies as a function of phase ϕ, ie. $\cos\phi$ between the two signals.

The double frequency term is eliminated by the low pass filter and the dc signal is applied to the modulating input terminal of a VCO. It can be seen that in the perfect locked state ($f_s = f_o$), the phase shift should be 90° ($\cos 90^\circ = 0$), in order to get zero error signal, that is $V_e = 0$

There are two problems associated with the switch type phase detector.

1. the output voltage V_e is proportional to the input signal amplitude V_s. This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude
2. the output is proportional to $\cos\phi$ and not proportional to ϕ making it non-linear.

Both these problems can be eliminated by limiting the amplitude of the input signal, that is converting the input to a constant amplitude square wave. A circuit which performs phase comparison with square wave input is called Balanced modulator.

Analog phase detector using Balanced modulator:

Balanced modulator is used as full-wave switching phase detector. Here the input signals is applied to the differential pair $Q_1 Q_2$.

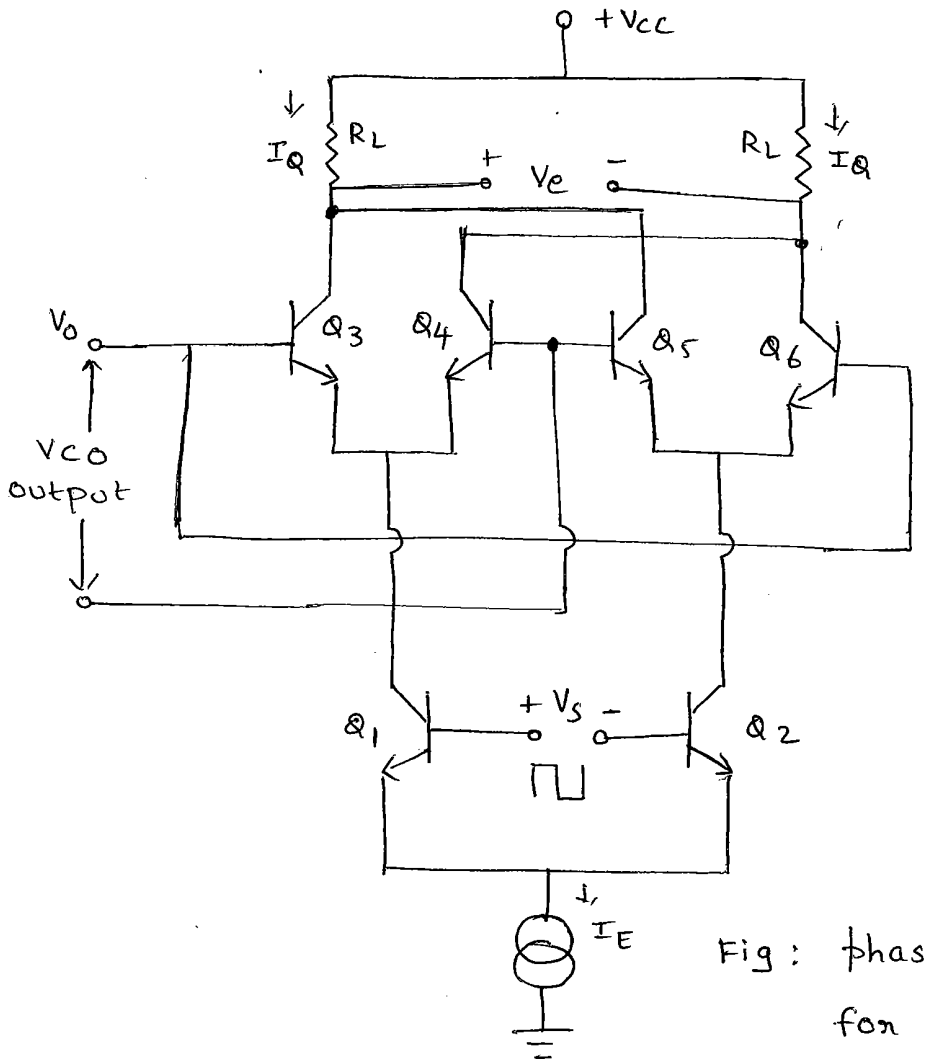
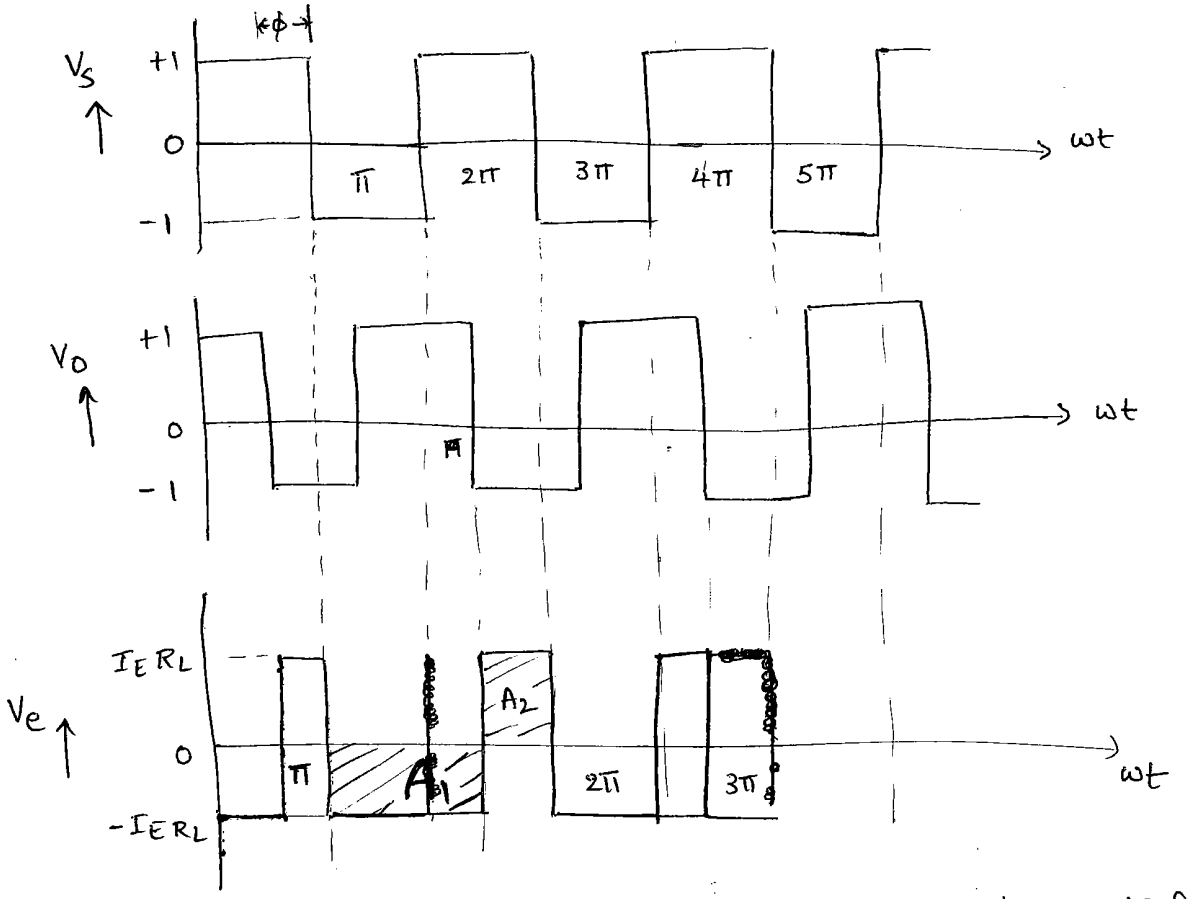


Fig: phase detector for IC PLL

Transistors $Q_3 - Q_4$ and $Q_5 - Q_6$ are two sets of SPDT switches activated by the VCO output.

The input signal V_S and the VCO output V_0 are assumed to be high enough to switch the transistors in figure above fully on or off.



Fig(b): Timing diagram of input and output waveforms for balanced modulator circuit.

In figure (b) when V_S and V_0 both are high during the time 0 to $(\pi - \phi)$, transistors Q_1 and Q_3 are driven on and current I_E flows through Q_1 and Q_3. This gives an output voltage

$$V_e = -I_E R_L$$

Next for the period $(\pi - \theta)$ for π, when V_S is high and V_0 is low, transistors Q_1 and Q_4 are driven on resulting in an output voltage $V_e = I_E R_L$

In this way, the output voltage waveform Ve is obtained

$$V_{e(avg)} = \frac{1}{\pi}\left[(\text{area } A_1) + \text{area}(A_2)\right]$$

$$= \frac{1}{\pi}\left[I_E R_L \phi + (-I_E R_L) \times (\pi - \phi) \right]$$

$$= I_E R_L \left[\frac{2\phi}{\pi} - 1 \right]$$

$$V_{e(avg)} = \frac{2 I_E R_L}{\pi}\left[\phi - \frac{\pi}{2} \right] \quad \text{--- (1)}$$

$$V_{e(avg)} = K_\phi \left(\phi - \frac{\pi}{2} \right)$$

where $K_\phi = \frac{2 I_E R_L}{\pi} = \frac{4 I_Q R_L}{\pi}$ $\left[\because I_E = 2 I_Q \right]$

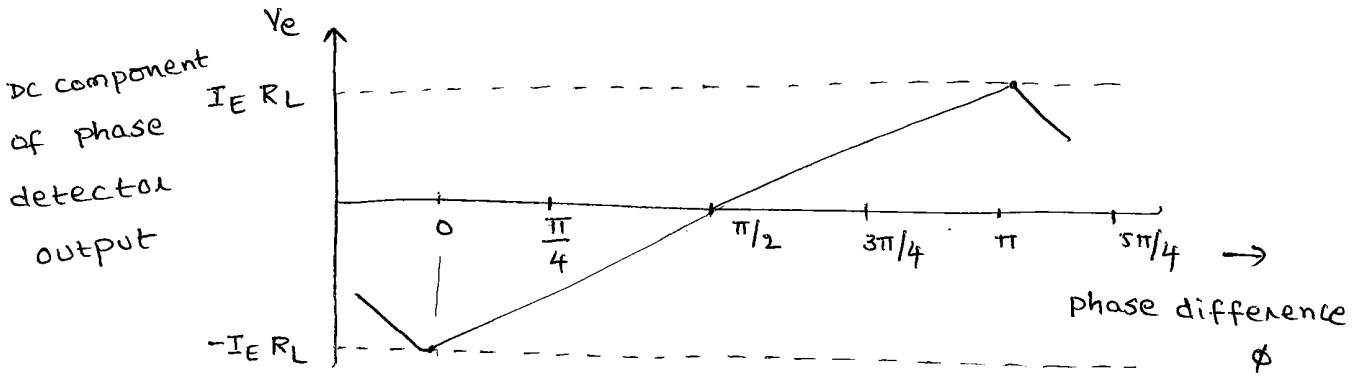


Fig (c)

where K_ϕ is the phase angle to voltage transfer co-efficient or the conversion ratio of the phase detector. This linear relationship between Ve and ϕ is shown in figure (c).

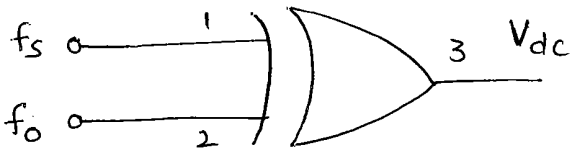
2) ~~Digition~~ Digital phase detector :

There are two types of digital phase detectors available

a) Digital phase detector using EX-OR detector

b) Edge triggered phase detector.

a) EXOR phase detector :



Fig(a): EXOR phase detector

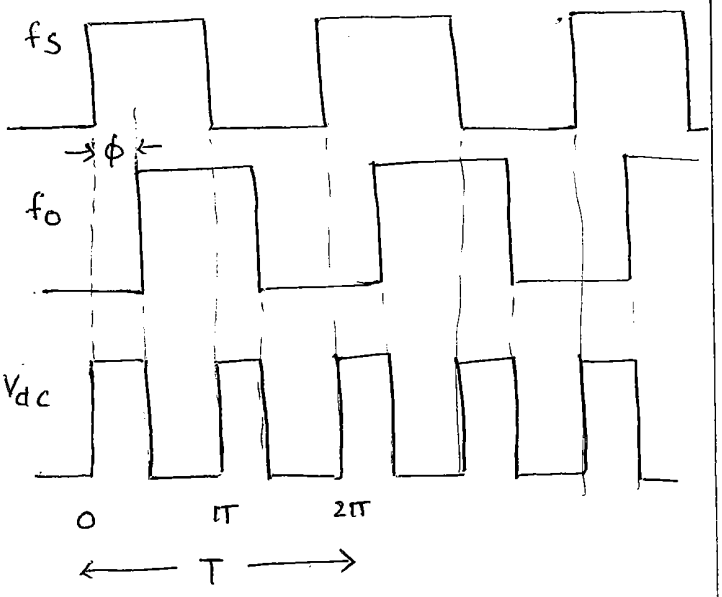


Fig: Input and output waveforms

Figure shows the digital type XOR phase detector. It uses CMOS type 4070 Quad 2-input XOR gate. the output of the XOR Gate is high when only one of the input signals f_s (or) f_o is high. This type of detector is used when both the input signals are square waves. the input and output waveforms for $f_s = f_o$ are shown in fig(b). In this figure f_s is Leading f_o by ϕ degrees. The variation of dc output voltage with phase difference ϕ is shown in fig(c).

It can be seen that the maximum dc output voltage occurs when the phase difference is π because the output of the gate remains high throughout.

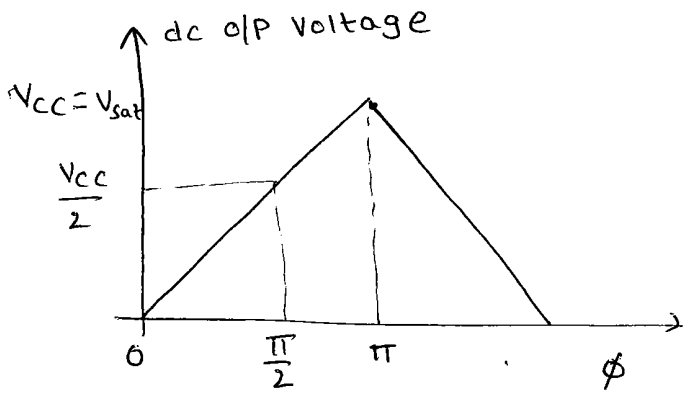


Fig (c): DC output voltage Versus ϕ

the slope of the curve gives the conversion ratio K_ϕ of the phase detector. so the conversion ratio K_ϕ for a supply voltage $V_{CC} = 5V$ is , $K_\phi = \frac{5}{\pi} = 1.59$ V/rad.

b) Edge triggered phase Detector :

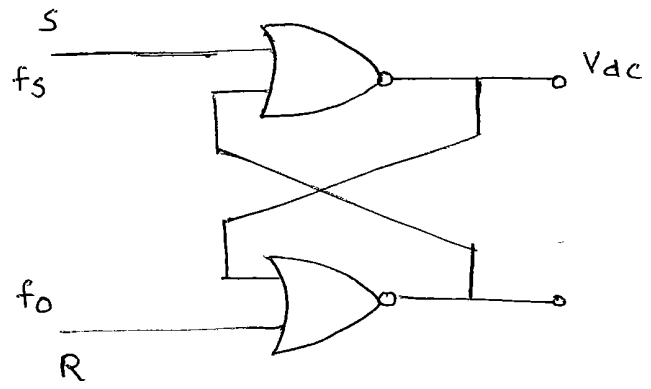


Fig (a) : Edge triggered phase detector

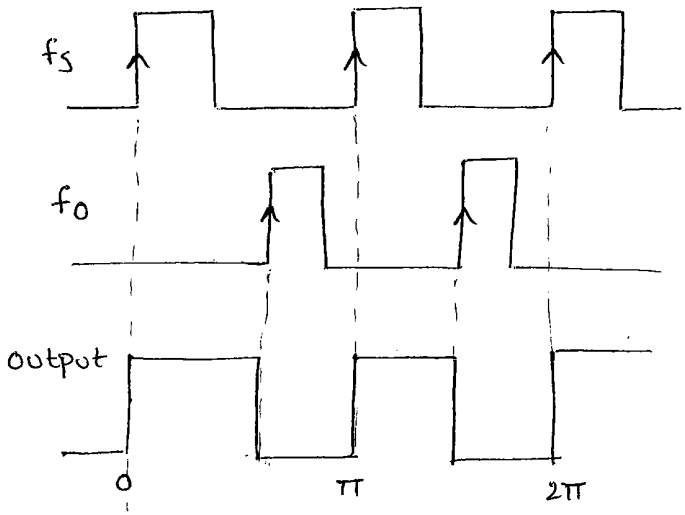


Fig (b) : Input and output waveforms

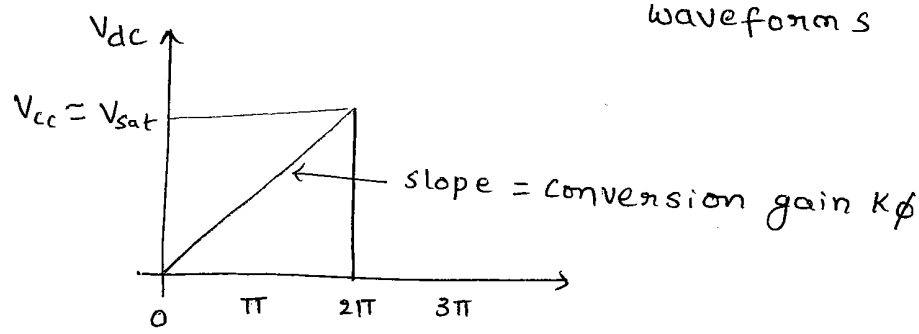


Fig (c) : DC output voltage Vs ϕ

The edge triggered digital phase detector is shown in figure (a). The circuit is an RS flip flop made by NOR gates. This circuit is useful when f_S and f_o are both pulse waveforms with duty cycle less than 50 %.

The output of the R-S flip flop changes its state on the leading edge of f_S and f_o as shown in fig (b). The variation of dc output voltage Vs ϕ is shown in fig (c). This type of detector has better capture tracking and locking characteristics as the dc output voltage is linear up to 360° compared to 180° in the case of EX-OR detector.

Voltage controlled oscillator (VCO):

A common type of VCO available in IC form NE/SE 566. The pin configuration and basic block diagram of 566 VCO are shown in figures below.

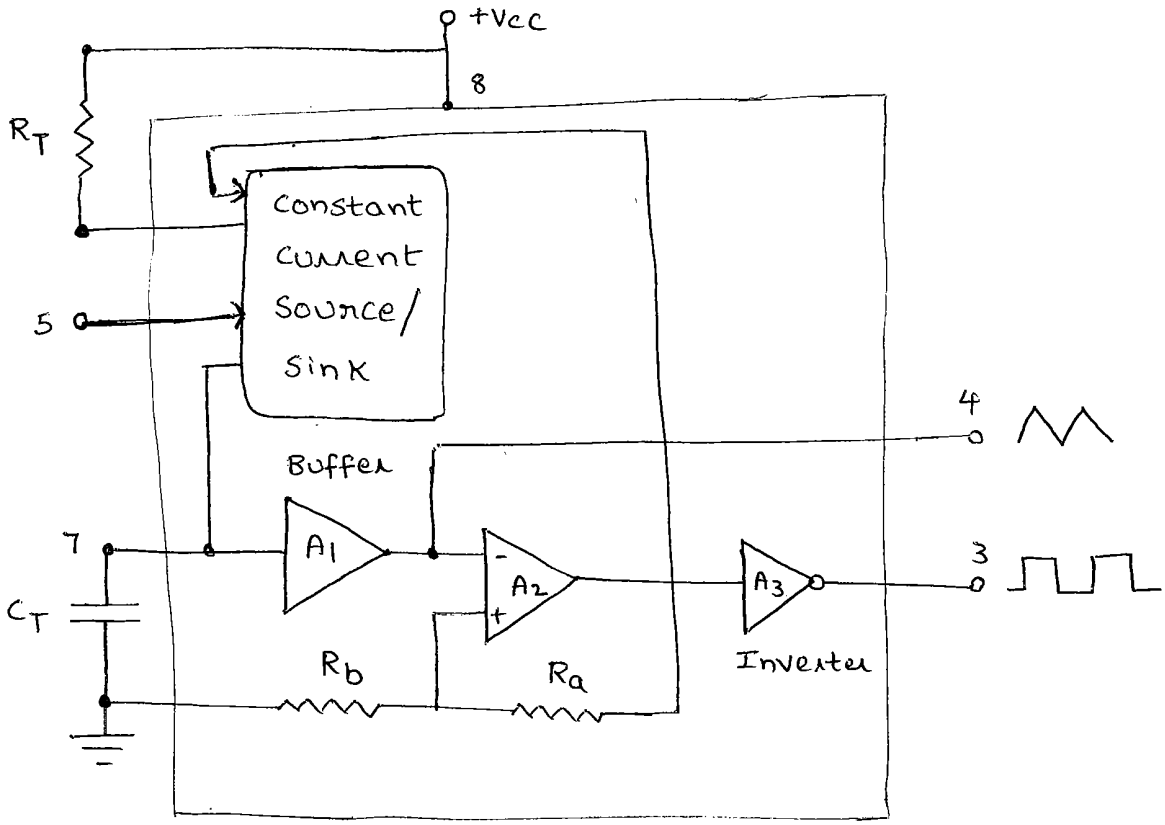


Fig: Voltage controlled oscillator Block diagram

A timing capacitor C_T is linearly charged or discharged by a constant current source / sink. The amount of current can be controlled by changing the voltage Vc applied at the modulating input (Pin 5) or by changing the timing resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage at pin 5.

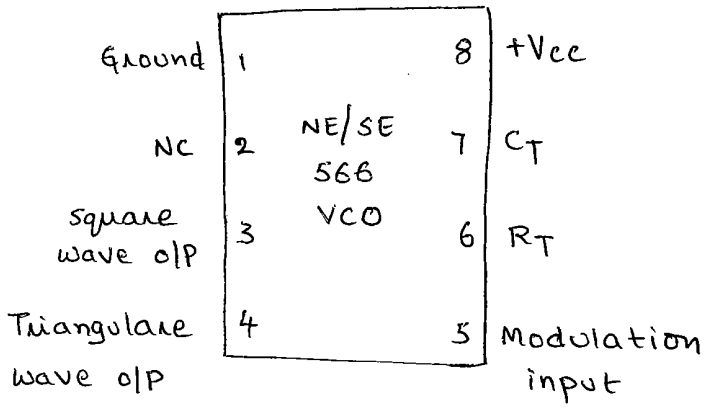


Fig: Pin Configuration.

Thus if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

A small capacitor of 0.001 μF should be connected between pin 5 and 6 to eliminate possible oscillations. A VCO is commonly used in converting low frequency signals.

The voltage across the capacitor C_T is applied to the inverting input terminal of schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the schmitt trigger is designed to Vcc and 0.5 Vcc. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 Vcc to 0.25 Vcc.

In fig(c), when the voltage on the capacitor C_T exceeds 0.5 Vcc during the charging, the output of the schmitt trigger goes low (0.5 Vcc) the capacitor now discharges and when it is at 0.25 Vcc, the output of schmitt trigger goes High(Vcc)

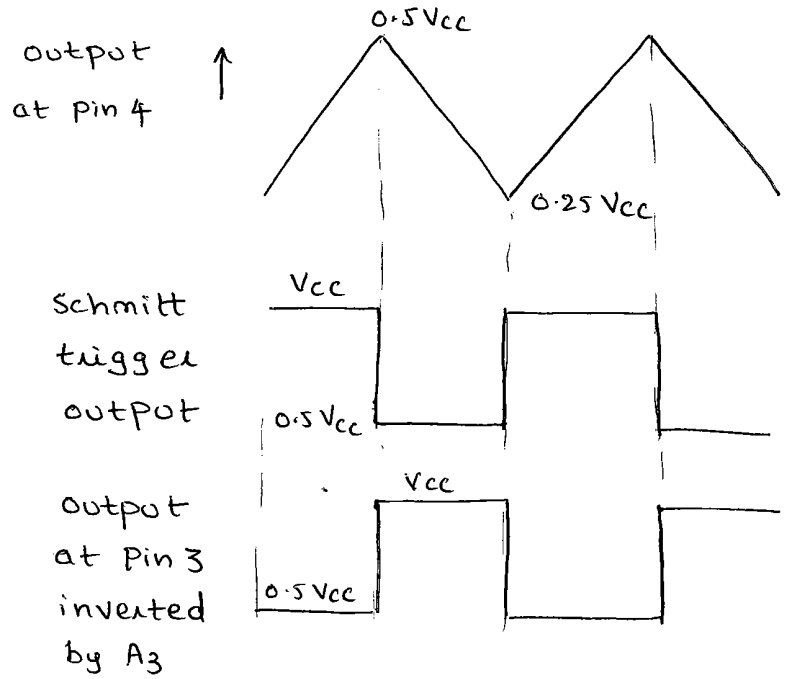


Fig c: output waveform.

since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular waveform across C_T which is also available at pin 4.

The square wave output of the schmitt trigger is inverted by inverter A_3 and is available at pin 3.

The output waveforms are shown in fig (c)

The output frequency of the VCO can be calculated as follows.

The total voltage on the capacitor changes from 0.25 V_{cc} to 0.5 V_{cc}. Thus $\Delta V = 0.25\ V_{cc}$

The capacitor charges with a constant current source. So

$$i = C_T \frac{\Delta V}{\Delta t} \Rightarrow \frac{0.25\ V_{cc}}{\Delta t} = \frac{i}{C_T}$$

$$\Delta t = \frac{0.25\ V_{cc}\ C_T}{i} \quad (or)$$

The time period T of the triangular waveform = $2\Delta t$

The frequency of oscillator f_o is

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5\ V_{cc}\ C_T}$$

$$i = \frac{V_{cc} - V_c}{R_T}$$

where V_c is the voltage at pin 5, therefore

$$f_o = \frac{2\ (V_{cc} - V_c)}{R_T\ C_T\ V_{cc}} \longrightarrow (1)$$

the outpot frequency of the VCO can be changed either by (i) R_T (ii) C_T (iii) the voltage V_c at the modulating input terminal Pin 5.

With no modulating input signal, if the voltage at Pin 5 is biased at $\frac{7}{8}V_{CC}$, Eq ① gives the VCO outpot frequency as

$$f_o = \frac{2\left(V_{CC} - \frac{7}{8}V_{CC}\right)}{R_T C_T V_{CC}} = \frac{0.25}{R_T C_T} \longrightarrow ②$$

Voltage to frequency conversion factor:

A parameter of importance for VCO is voltage to frequency conversion factor K_V and is defined as

$$K_V = \frac{\Delta f_o}{\Delta V_c}$$

Here ΔV_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO. If we assume that the original frequency is f_o and the new frequency is f_1, then

$$\Delta f_o = f_1 - f_o = \frac{2\left(V_{CC} - V_c + \Delta V_c\right)}{R_T C_T V_{CC}} - \frac{2\left(V_{CC} - V_c\right)}{R_T C_T V_{CC}}$$

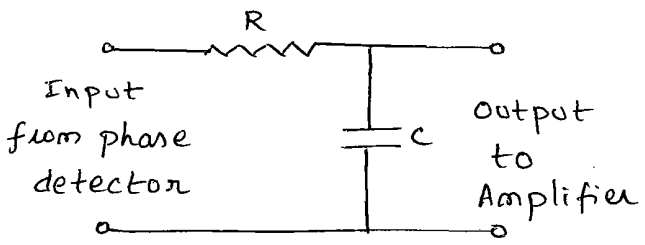
$$\Delta f_o = \frac{2\Delta V_c}{R_T C_T V_{CC}} \qquad \text{or} \qquad \Delta V_c = \frac{\Delta f_o R_T C_T V_{CC}}{2}$$

Putting the value of $R_T C_T$ from Eq ②

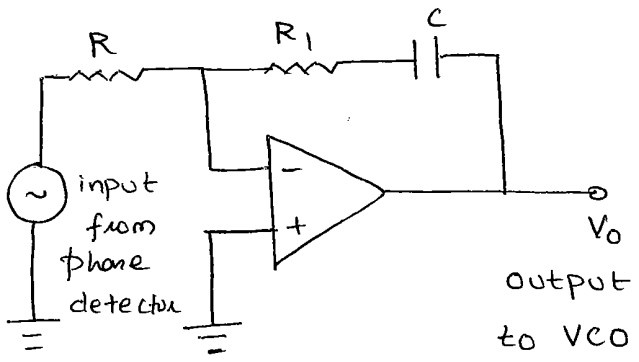
$$\Delta V_c = \frac{\Delta f_o V_{CC}}{8 f_o} \Rightarrow K_V = \frac{\Delta f_o}{\Delta V_c} = \frac{8 f_o}{V_{CC}}$$

Low pass filter:

The filter used in a PLL may be either passive type or active type as shown in figures below.



Fig(a): passive filter



Fig(b): Active filter

The low pass filter not only removes the high frequency components and noise, but also controls the dynamic characteristics of the PLL. these characteristics include capture, lock range, bandwidth and transient response. If filter band width is reduced, the response time increases. However reducing the band width of the filter also reduces the capture range of the PLL.

The charge on the filter capacitor gives a short time memory to the PLL. Thus even if the signal becomes less than the noise for a few cycles, the dc voltage on the capacitor continues to shift the frequency of the VCO till it picks up signal again. This produces a high noise immunity and locking stability.

Monolithic phase - locked loop :

All the different building blocks of PLL are available as independent IC packages and can be externally interconnected to make a PLL. However a number of manufacturers introduced monolithic PLL's too. Important Monolithic PLL is IC 565 :

IC 565 PLL :

565 is available as 14-Pin DIP package and as 10-Pin metal can package. The pin configuration and the block diagram are shown in fig (a) and (b)

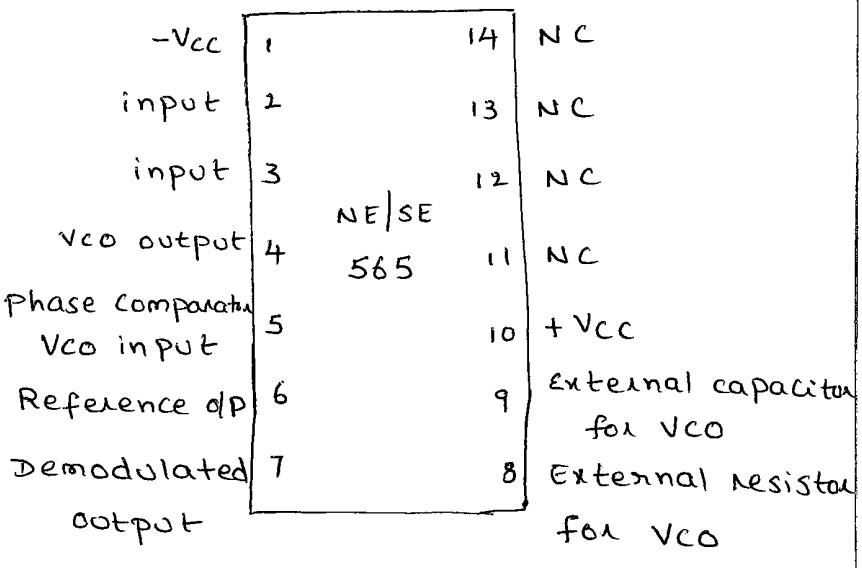


Fig a : Pin Diagram

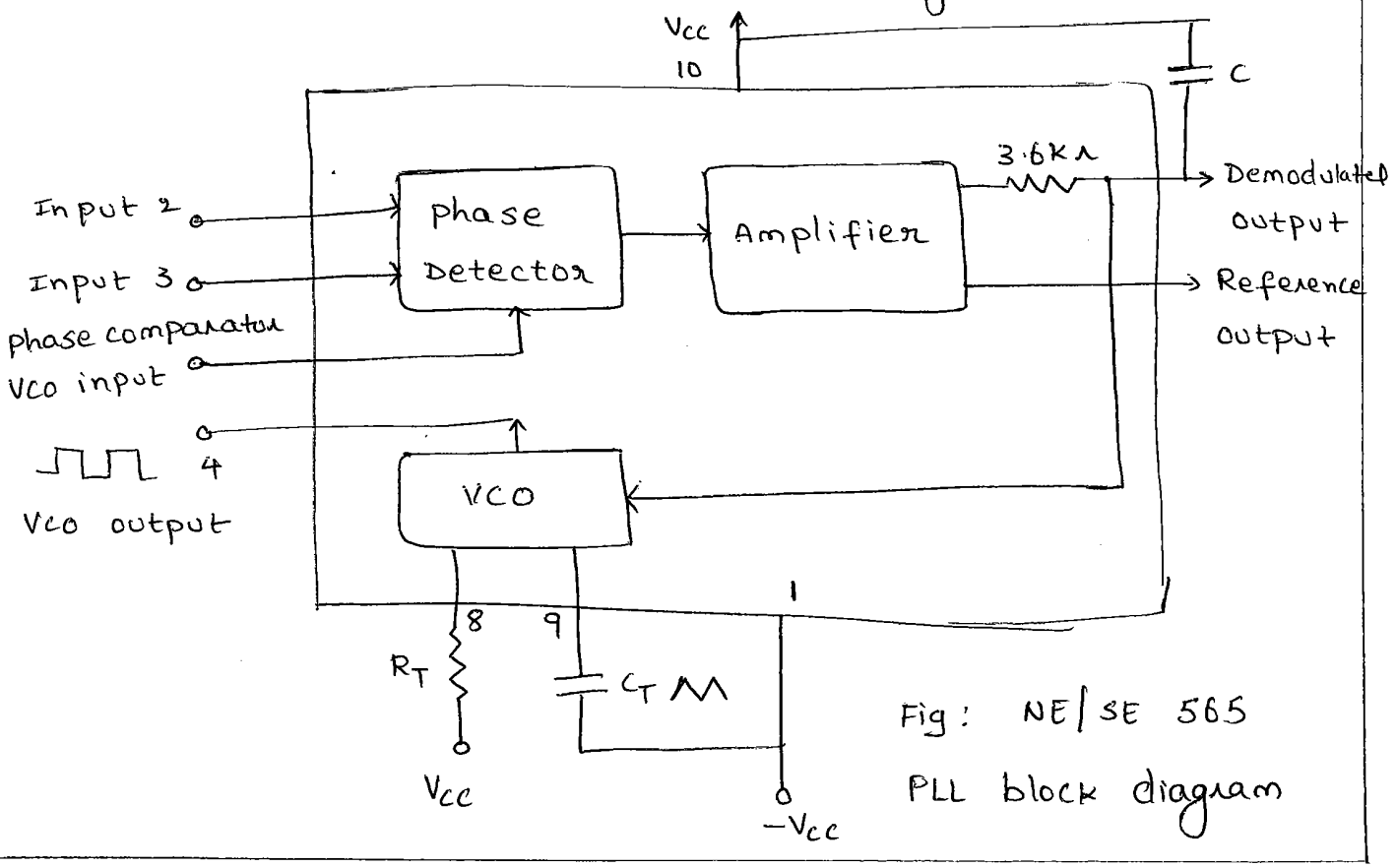


Fig : NE/SE 565 PLL block diagram

the output frequency of the VCO (both inputs 2,3 grounded) can be given as

$$f_o = \frac{0.25}{R_T C_T}$$

where R_T and C_T are the external resistor and capacitor connected to pin 8 and 9.
the VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range. It may be seen that PLL is internally broken b/n the VCO output and the phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_o with input signal f_s. A capacitor C is connected between Pin 7 and Pin 10 to make a low pass filter with the internal resistance of 3.6KΩ.

Derivation of Lock-in Range:

If ϕ radians is the phase difference between the signal and the VCO voltage, then the output voltage of the analog phase detector is given by

$$V_e = K_\phi \left(\phi - \frac{\pi}{2}\right) \longrightarrow (1)$$

where K_ϕ is the phase angle to voltage transfer co-efficient of the phase detector. the control voltage to VCO is

$$V_c = A K_\phi \left(\phi - \frac{\pi}{2}\right) \longrightarrow (2)$$

where A → voltage gain of the Amplifier.

This V_c shifts VCO frequency from its free running frequency f_0 to a frequency f given by

$$f = f_0 + K_V V_c \longrightarrow (3)$$

where K_V → voltage to frequency transfer co-efficient of the VCO.

when PLL is locked in to signal frequency f_s, then we have

$$f = f_s = f_0 + K_V V_c$$

Since $V_c = \frac{f_s - f_0}{K_V} = A K_\phi \left(\phi - \frac{\pi}{2}\right)$ [∵ from 2] → (4)

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian and $V_{c(max)} = \pm K_\phi \frac{\pi}{2}$. The corresponding value of the maximum control voltage available to drive the VCO will be

$$V_{c(max)} = \pm \left(\frac{\pi}{2}\right) K_\phi A \longrightarrow (5)$$

The maximum VCO frequency swing that can be obtained is given by

$$f_s = f_0 \pm (f - f_0)_{max} = f_0 \pm K_V K_\phi \left(\frac{\pi}{2}\right) A = f_0 + \Delta f_L$$

Here $\Delta f_L = \pm K_V K_\phi A \frac{\pi}{2} \longrightarrow (6)$

Total lock range $2\Delta f_L = \pm K_V K_\phi A \pi \longrightarrow (7)$

The lock-in range is symmetrically located with respect to VCO free running frequency f_0

For IC 565 PLL

$$K_V = \frac{8 f_0}{V} \rightarrow (8) \text{ where } V = +V_{cc} - (-V_{cc})$$

Again $K\phi = \frac{1.4}{\pi}$ and $A = 1.4$

Hence the lock-in range becomes

$$\boxed{\Delta f_L = \frac{\pm 7.8 f_o}{V}} \longrightarrow (9)$$

Derivation of capture Range :

When PLL is not initially locked to the signal, the frequency of the VCO will be free running frequency f_o. The phase angle difference between the signal and the VCO output voltage will be

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o)t + \Delta\theta \longrightarrow (1)$$

thus the phase angle difference doesn't remain constant but will change with time at a rate given by

$$\frac{d\phi}{dt} = \omega_s - \omega_o \longrightarrow (2)$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K\phi \frac{\pi}{2}$ and a fundamental frequency $f_s - f_o = \Delta f$

The low pass filter is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j\left(\frac{f}{f_1}\right)} \quad \text{where} \quad f_1 = \frac{1}{2\pi RC}$$

$$|T(jf)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_1}\right)^2}} \longrightarrow (3)$$

As $(f/f_1)^2 >> 1$ then $T(f) = \frac{f_1}{f} \longrightarrow (4)$

the fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $\Delta f = f_s - f_0$. then

$$T(\Delta f) = \frac{f_1}{\Delta f} = \frac{f_1}{f_s - f_0} \longrightarrow (5)$$

The voltage V_c to drive the VCO is

$$V_c = V_e \times T(f) \times A$$

$$V_{c(max)} = V_{e(max)} \times T(f) \times A$$

$$V_{c(max)} = \pm K_\phi \left(\frac{\pi}{2}\right) A \frac{f_1}{\Delta f} \longrightarrow (6)$$

then the corresponding value of the maximum VCO frequency shift is

$$(f - f_0)_{max} = K_V V_{c(max)} = \pm K_V K_\phi \left(\frac{\pi}{2}\right) A \frac{f_1}{\Delta f} \rightarrow (7)$$

For the acquisition of the signal frequency we should put $f = f_s$, so that the maximum signal frequency range that can be acquired by PLL is

$$(f_s - f_0)_{max} = \pm K_V K_\phi \left(\frac{\pi}{2}\right) A \frac{f_1}{\Delta f_c}$$

Now $\Delta f_c = (f_s - f_0)_{max}$

So $(\Delta f_c)^2 = \pm K_V K_\phi \left(\frac{\pi}{2}\right) A f_1$

Since $\Delta f_L = \pm K_V K_\phi \left(\frac{\pi}{2}\right) A$

then $\Delta f_c = \pm \sqrt{f_1 \Delta f_L}$

Therefore the total capture range is $2\Delta f_c = \pm 2\sqrt{f_1 \Delta f_L}$

In case of IC PLL 565, $R = 3.6\,k\Omega$ so the capture range is

$$\Delta f_C = \pm \left[\frac{\Delta f_L}{2\pi (3.6 \times 10^3) C} \right]^{1/2}$$

The capture range is symmetrically located with respect to VCO free running frequency f_0 as shown in figure below. The PLL cannot acquire a signal outside the capture range, but once captured, it will hold on till the signal frequency goes beyond the lock-in range. In order to increase the ability of lock-in range, large capture range is required. However a large capture range will make the PLL more susceptible to noise and undesirable signal. Hence a suitable compromise is often reached between these two opposing requirements of the capture range.

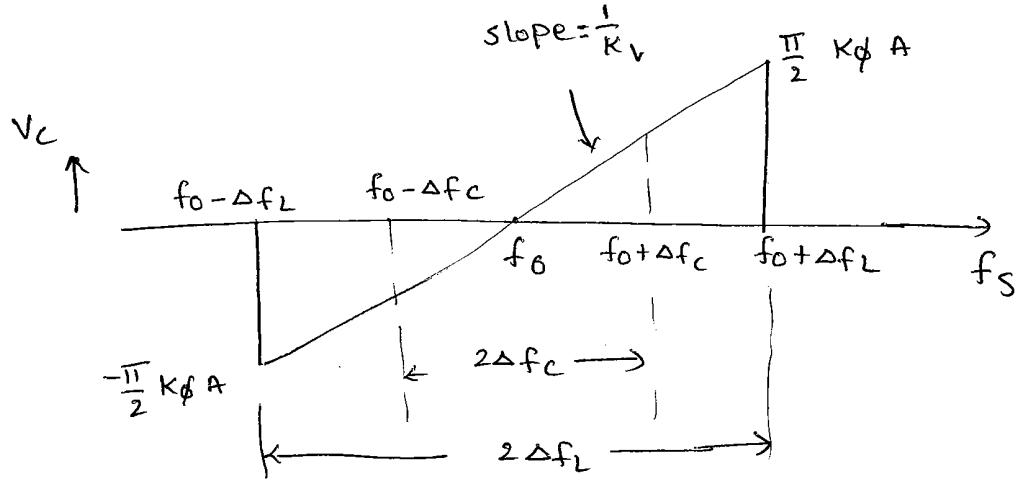


Fig: PLL lock-in range and capture range

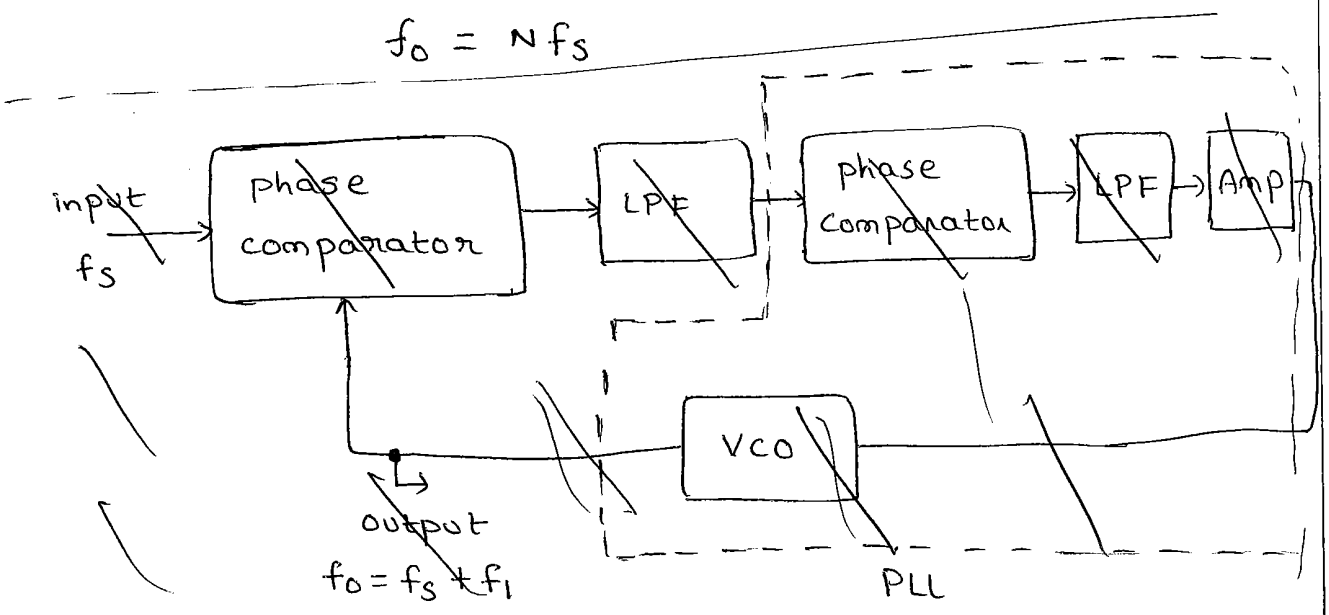
Applications of PLL :

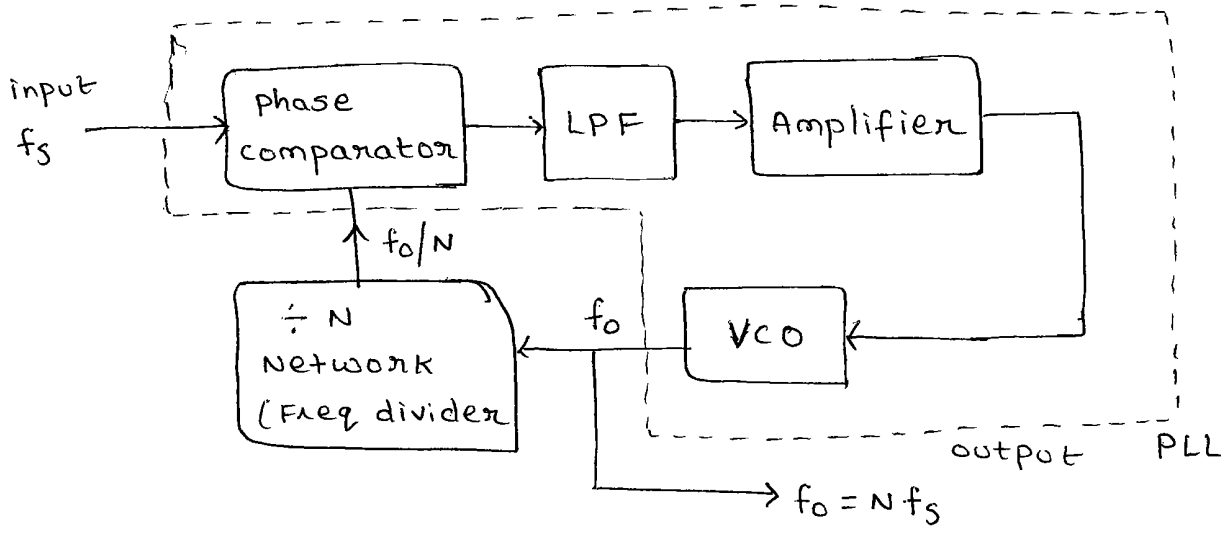
The output from a PLL system can be obtained either as the voltage signal $V_c(t)$ corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator application where as the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

1. Frequency Multiplication / Division :

Figure below gives the block diagram of a frequency multiplier using PLL. A divide by N network is inserted between the VCO output and the phase comparator input. In the locked state, the VCO output frequency f_o is given by

$$f_o = N f_s$$





The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

Frequency multiplication can also be obtained by using PLL in its harmonic locking mode.

The above circuit can also be used for frequency division. Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_s. The output f_o of VCO is now given by

$$f_o = \frac{f_s}{m}$$

2) Frequency Translation:

A schematic for shifting the frequency of an oscillator by a small factor is shown in figure below. It can be seen that a multiplier and a low-pass filter are connected externally to the PLL.

The signal f_s which has to be shifted and the output frequency f_o of the VCO are applied as

A PLL may be used to demodulate Am signals as shown in figure above. The PLL is locked to the carrier frequency of the incoming Am signal. The output of the VCO which has the same frequency as the carrier, but unmodulated is fed to the Amplifier.

since VCO output is always 90° out of phase with the incoming Am signal under the locked Condition, the AM input signal is also shifted in phase by 90° before being fed to the amplifier. This makes both the signals applied to the multiplier in same phase.

The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL Am detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

D/A and A/D Converts

Introduction: most of the real world physical quantities such as voltage, current, temperature, pressure and time etc are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superim-position of noise as in the case of amplitude modulation. Therefore, for processing, transmission and storage purposes, it is often convinient to express these variables in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital and digital to analog conversion.

D to A Converters

Basic DAC techniques:

The schematic of a DAC is shown in fig. The input is a binary word D and is combined with a reference voltage V_R to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

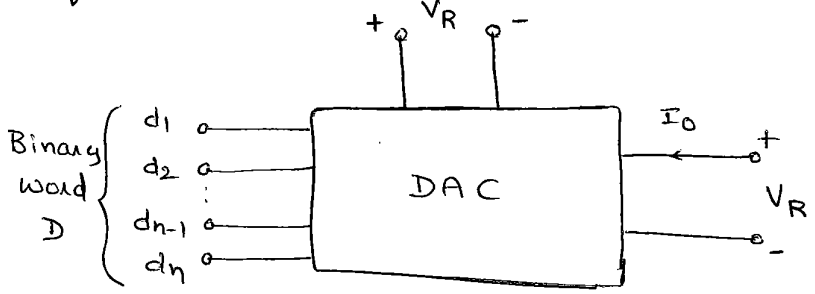


Fig: Schematic of DAC

$$V_o = K V_{FS} \left(d_1 2^{-1} + d_2 2^{-2} + \text{----} + d_n 2^{-n} \right) \longrightarrow (1)$$

where V_o = output voltage

V_{FS} = Full scale output voltage

K = scaling factor usually adjusted to unity

$d_1, d_2 \text{ ---- } d_n$ = n-bit binary fractional word with the decimal point located at the left.

d_1 = MSB with a weight of $V_{FS}/2$

d_n = LSB with a weight of $V_{FS}/2^n$.

1) Weighted Resistor DAC :

One of the simplest circuits shown in figure below uses a summing Amplifier with a binary weighted resistor network.

It has n electronic switches $d_1, d_2 \cdots d_n$ controlled by binary input word. these switches are single pole double throw type. (SPDT).

If the binary input to a particular switch is 1, it connects a reference voltage $(-V_R)$. And if the input bit is 0, the switch connects the resistor to the ground. From the figure, the output current I_o for an ideal op-Amp can be written as

$$I_o = I_1 + I_2 + I_3 + \text{---} + I_n$$

$$I_o = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \text{---} + \frac{V_R}{2^n R} d_n$$

$$V_o = \frac{V_R}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \text{------} + d_n 2^{-n}\right)$$

The output voltage

$$V_o = -I_o R_f = V_R \frac{R_f}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \text{---} + d_n 2^{-n}\right) \rightarrow (2)$$

comparing Eq (2) with Eq (1), it can be seen that if $R_f = R$ then $K = 1$ and $V_{FS} = V_R$.

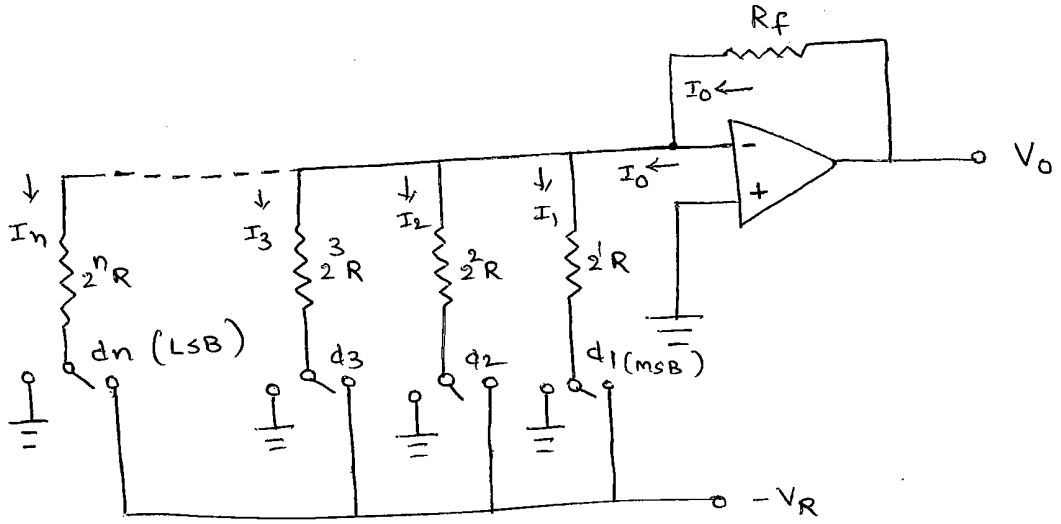
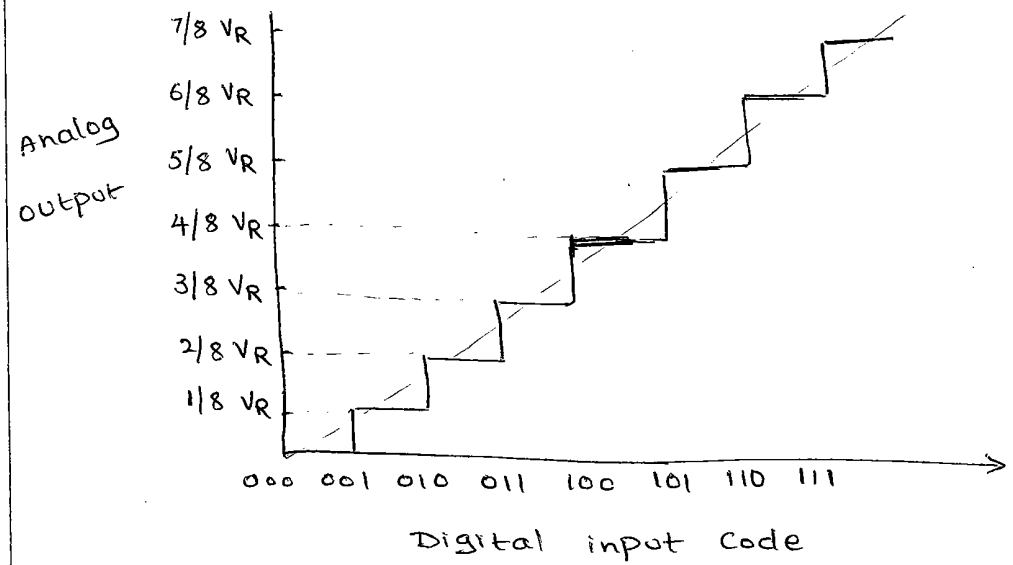


Fig (a): A simple weighted resistor DAC



Fig(b): Transfer characteristics of a 3-bit DAC

If $D = 100$, $V_o = V_R \frac{R_f}{R}\left(1 \times 2^{-1} + 0 \times 2^{-2} + 0 \times 2^{-3}\right)$

$$V_o = \frac{V_R}{2} = \frac{4V_R}{8}$$

the circuit shown in above figure uses a negative reference voltage. the analog output voltage is therefore positive stair case as shown in figure(b). for a 3-bit weighted resistor DAC. It may be noted that

1) Although the op-Amp is connected in inverting mode, it can also be connected in non-inverting mode.
2) The op-Amp is simply working as a current to voltage converter.
3) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be +5V, and the output will be negative.

2) R-2R Ladder DAC

wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 KΩ to 10 KΩ.

For simplicity, consider a 3-bit DAC as shown in figure below, where the switch position $d_1 d_2 d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of fig(b) and finally to fig(c). Then voltage at node c can be easily calculated by the set procedure of network analysis as

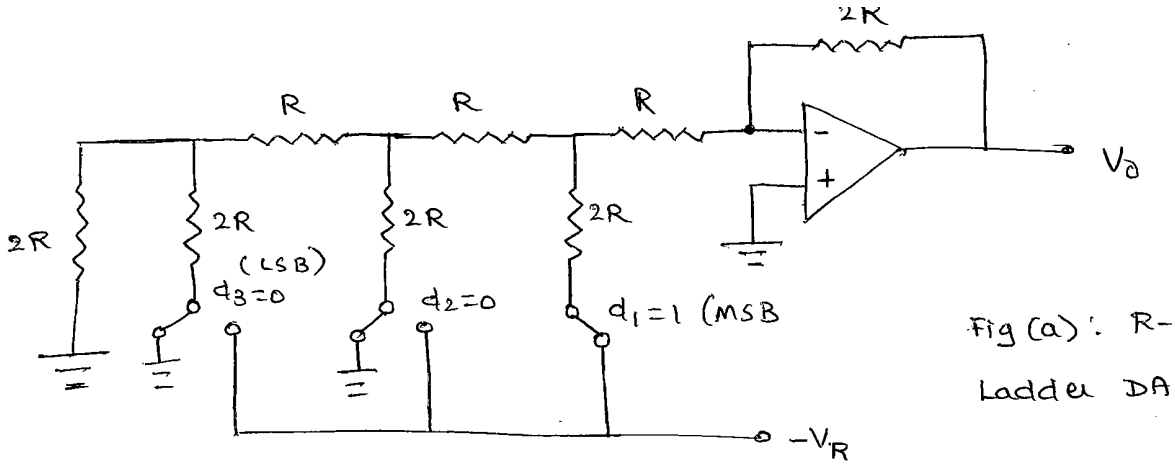


Fig (a): R-2R Ladder DAC

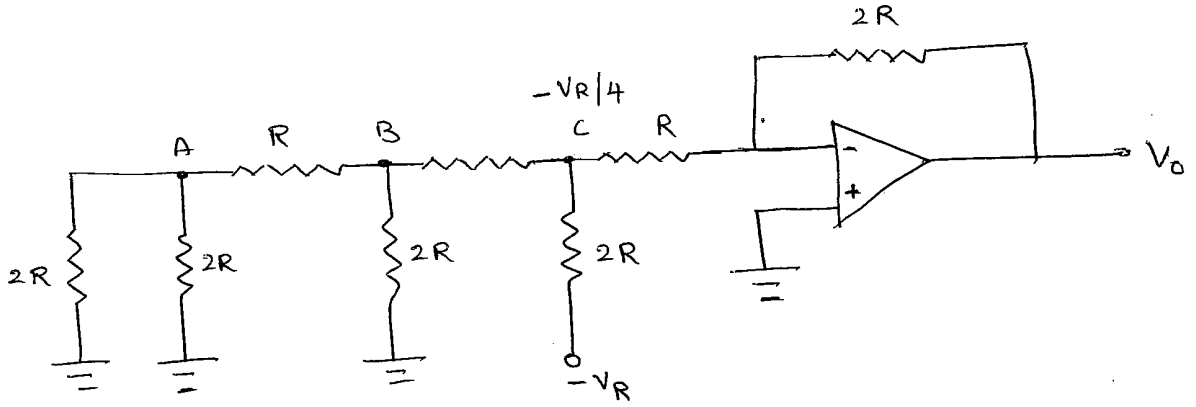


Fig (b): Equivalent circuit of fig (a)

$$V_C = \frac{-V_R\left(\frac{2}{3}R\right)}{2R + \frac{2}{3}R} = \frac{-V_R}{4}$$

the output voltage

$$V_0 = -\frac{2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

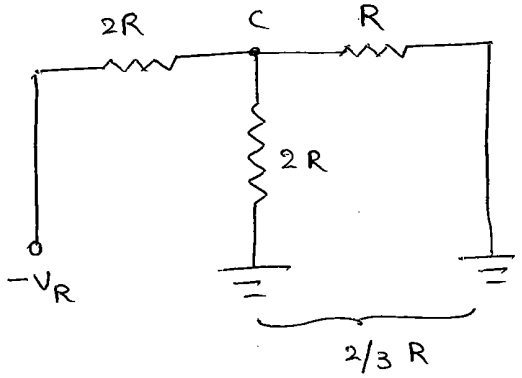


Fig c: Equivalent circuit of fig (b)

Similarly For binary word 001

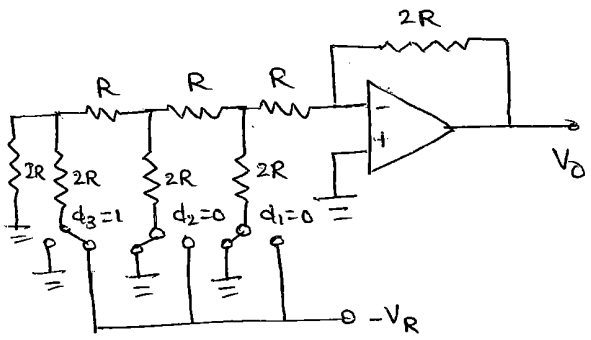


Fig: R-2R ladder DAC for switch positions 001

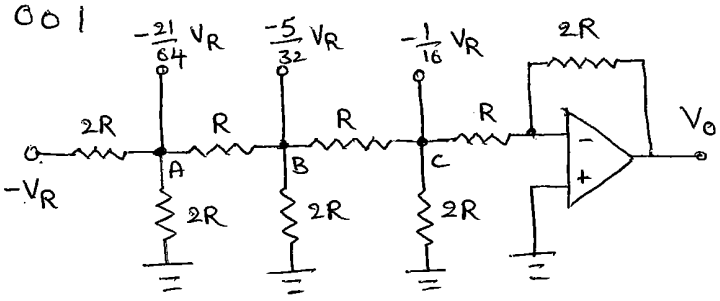
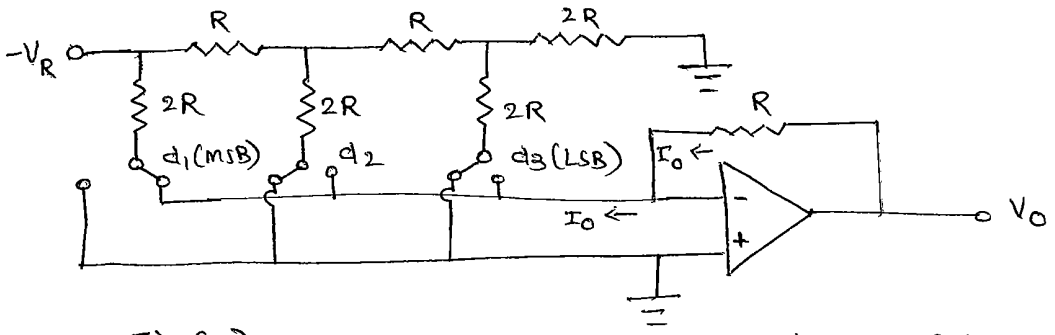


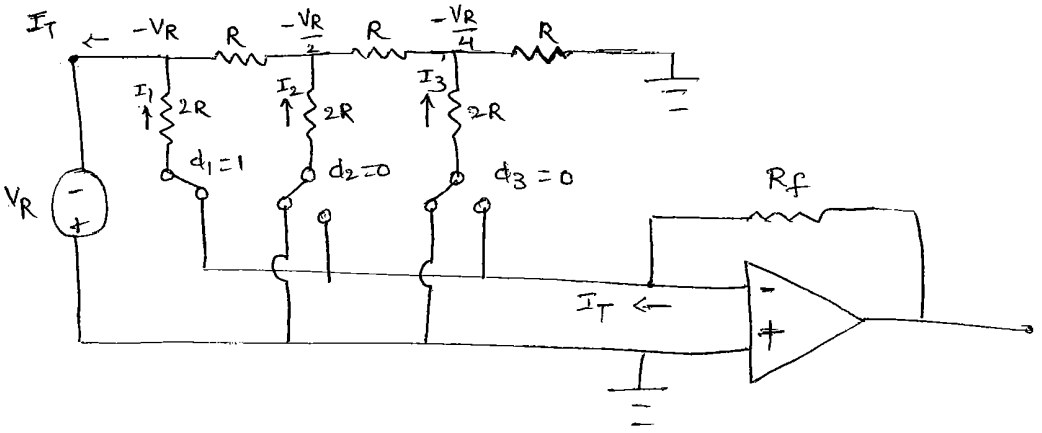
Fig (d): Equivalent circuit

$$V_0 = \left(-\frac{2R}{R}\right)\left(\frac{-V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

3) Inverted R-2R ladder DAC :



Fig(a) : Inverted R-2R Ladder DAC.



$$I_1 = \frac{V_R}{2R} \qquad I_2 = \frac{V_R}{2}\Big/2R = \frac{V_R}{4R} \qquad I_3 = \frac{V_R}{4}\Big/2R = \frac{V_R}{8R}$$

$$I_T = I_1 + I_2 + I_3$$

$$I_T = d_1\frac{V_R}{2R} + d_2\frac{V_R}{4R} + \frac{V_R}{8R}d_3 = \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right]$$

$$I_T = \frac{V_0 - 0}{R_f} \Rightarrow V_0 = I_T R_f$$

$$V_0 = V_R \frac{R_f}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right]$$

For 100 $\qquad V_0 = \frac{V_R}{2} \quad \left[\because R_f = R\right]$

In general

$$V_0 = V_R \frac{R_f}{R}\left[d_1 2^{-1} + d_2 2^{-2} + \cdots d_n 2^{-n}\right]$$

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. more power dissipation causes heating, which inturn creates non-linearity in DAC. This is a serious problem and can be avoided completely in Inverted ladder type DAC.

A 3-bit Inverted ladder type DAC is shown in figure, where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-Amp which is also at Virtual ground. since both the terminals of switches di are at ground potential, current flowing in the resistances is constant and independent of switch position.

Problem 1:

The basic step of a 9-bit DAC is 10.3mv. If 000000000 represents 0v, what output is produced if the input is 101101111?

Solution: The output voltage for input 101101111 is

$$= 10.3mv\left(1\times2^8 + 0\times2^7 + 1\times2^6 + 1\times2^5 + 0\times2^4 + 1\times2^3 + 1\times2^2 + 1\times2^1 + 1\times2^0\right)$$

$$= 3.78V.$$

Problem 2: calculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10V range.

Solution: $LSB = \frac{10\,V}{2^8} = 39\,mV$

$MSB = \frac{10}{2} = 5\,V$

Full scale output = Full scale Voltage − 1 LSB

= 10 V − 39 mV = 9.961 V

Problem 3: what output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is

i) 10 (for a 2-bit DAC)

ii) 0110 (for a 4-bit DAC)

iii) 10111100 (for a 8-bit DAC)

Solution: i) $V_0 = 10\left(1 \times \frac{1}{2} + 0 \times \frac{1}{4}\right) = 5\,V$

ii) $V_0 = 10\left(0 \times \frac{1}{2} + 1 \times \frac{1}{4} + 1 \times \frac{1}{8} + 0 \times \frac{1}{16}\right) = 3.75\,V$

iii) $V_0 = 10\left(1 \times \frac{1}{2} + 0 \times \frac{1}{2^2} + 1 \times \frac{1}{2^3} + 1 \times \frac{1}{2^4} + 1 \times \frac{1}{2^5} + 1 \times \frac{1}{2^6} + 0 \times \frac{1}{2^7} + 0 \times \frac{1}{2^8}\right) = 7.34\,V$

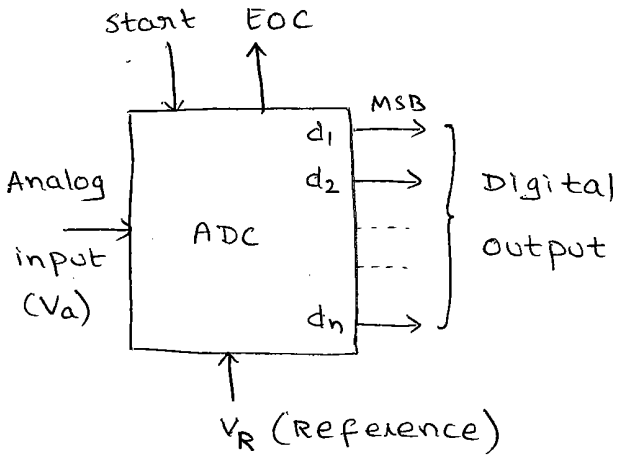
A-D Converters

The block schematic of ADC is shown in figure below It accepts an analog input voltage V_a and produces an output binary word $d_1, d_2 -- d_n$ of functional value D.

$$D = d_1 2^{-1} + d_2 2^{-2} + ---- + d_n 2^{-n}$$

where $d_1 \rightarrow$ MSB

d_A — LSB



An ADC usually has two additional control lines.

1. Start: used to tell the ADC when to start the conversion
2. End of Conversion (EOC): used to announce when the conversion is complete.

Depending upon the type of application, ADC's are designed for microprocessor interfacing or to directly drive LCD or LED displays.

ADC's are classified broadly in to two groups according to their conversion technique.

1. Direct type ADC's compare a given analog signal with the internally generated equivalent signal. This group includes
   1. Flash (comparator) type converter
   2. Counter type converter
   3. Tracking or servo converter
   4. Successive approximation type converter.
2. Integrating type ADC's perform conversion in an indirect manner by first changing the analog input signal

to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are

i) charge balancing ADC

ii) Dual slope ADC

The most commonly used ADC's are successive approximation and the integrator type. The successive approximation ADC's are used in applications such as data loggers and instrumentation where conversion speed is important. The successive approximation and comparator type are faster but generally less accurate than integrating type converters. The flash type is expensive for high degree of accuracy.

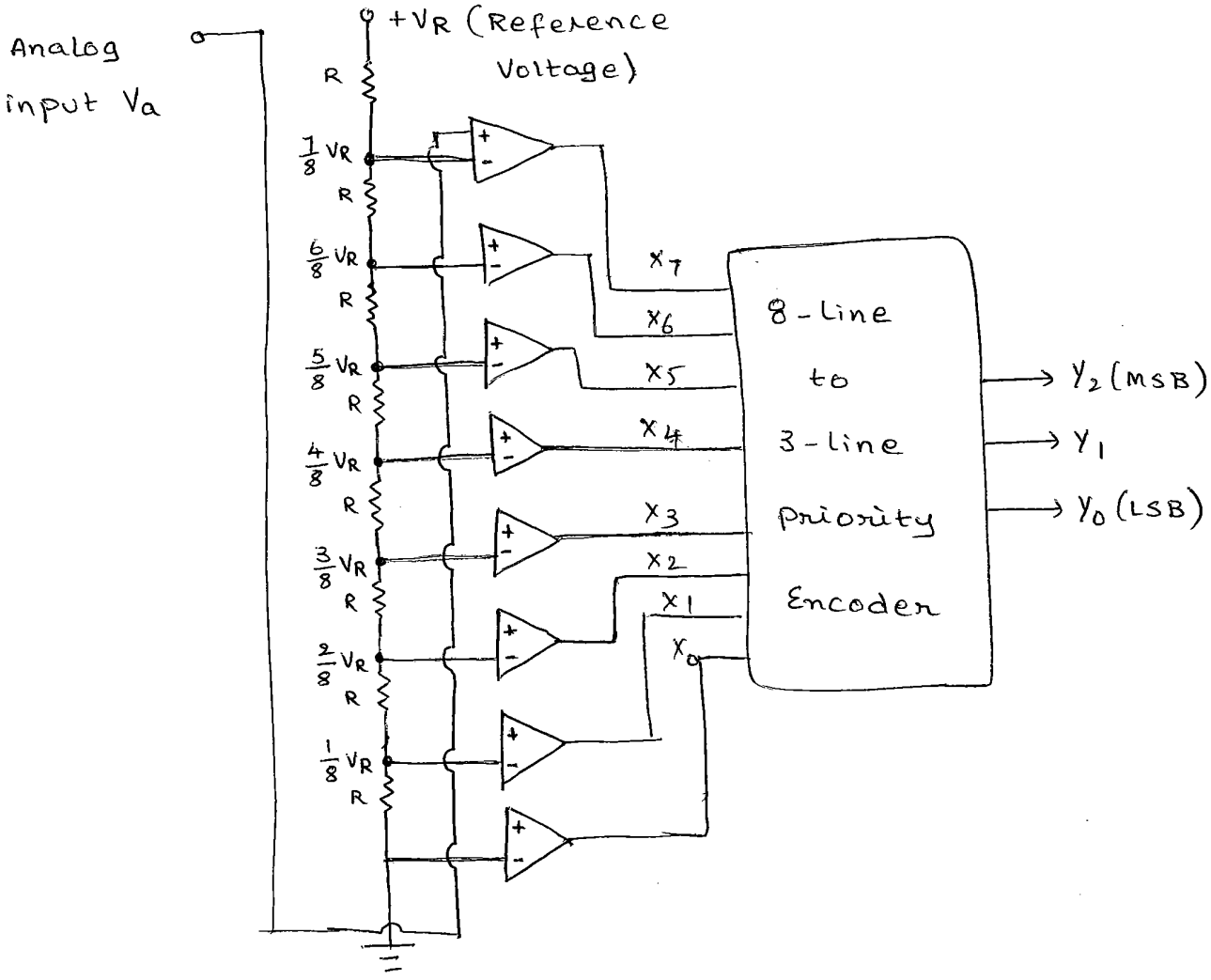
The integrating type converter is used in applications such as digital meter, panel meter and monitoring systems where the conversion accuracy is critical.

Direct type ADC's:

1) Flash (Parallel Comparator) A/D converter:

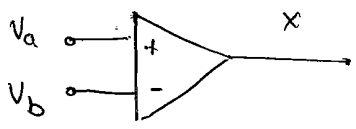
This is the simplest possible A/D Converter It is the fastest and most expensive technique. Figure below shows a 3-bit A/D Converter. The circuit consists of resistor divider network, 8 op-Amp comparators and a 8-line to 3 line Encoder. The comparator and its truth table is shown in figure below. In fig(a) At each node of the resistive divider

a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground. The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages. The truth table of the flash type A/D converter is shown below.



Fig(a): Basic circuit of a Flash type A/D Converter

Voltage input	Logic output X
$V_a > V_b$	X = 1
$V_a < V_b$	X = 0
$V_a = V_b$	previous value



Fig(b): Comparator and its truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $2V_R/8$	0	0	0	0	0	0	1	1	0	0	1
$2V_R/8$ to $3V_R/8$	0	0	0	0	0	1	1	1	0	1	0
$3V_R/8$ to $4V_R/8$	0	0	0	0	1	1	1	1	0	1	1
$4V_R/8$ to $5V_R/8$	0	0	0	1	1	1	1	1	1	0	0
$5V_R/8$ to $6V_R/8$	0	0	1	1	1	1	1	1	1	0	1
$6V_R/8$ to $7V_R/8$	0	1	1	1	1	1	1	1	1	1	0
$7V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig(c): Truth table for a Flash type A/D converter.

The circuit has the advantage of high speed as the conversion takes place simultaneously rather than sequentially. Typical conversion time 100ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder, Conversion delays of the order of 20ns can be obtained.

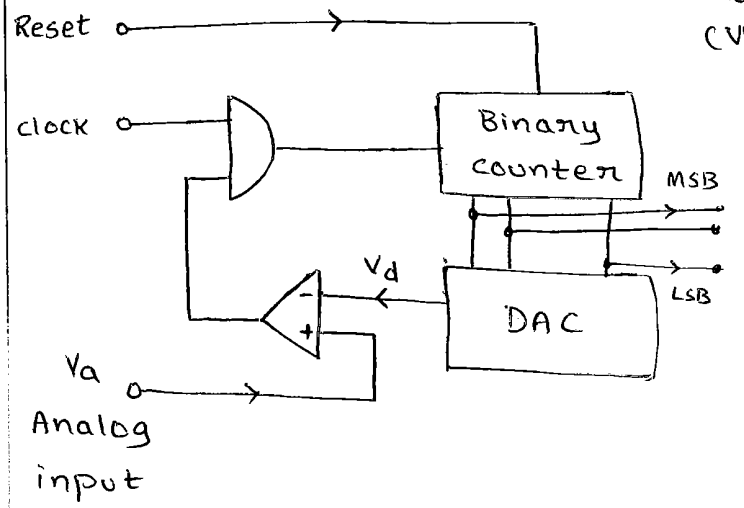
This type of ADC has the disadvantage that the number of comparators required doubles for each added bit. For Example n-bit ADC require 2^n comparators

2) Counter type A/D converter:

The D/A converter can easily be turned around to provide the inverse function A to D conversion. The principle is to adjust the DAC's input code until the DAC's output comes with in $\pm \frac{1}{2}$ LSB to the analog

input V_a which is to be converted to binary digital form.

A 3-bit counting ADC based upon the above principle is shown in figure below.



Fig(a): A Counter type A/D Converter

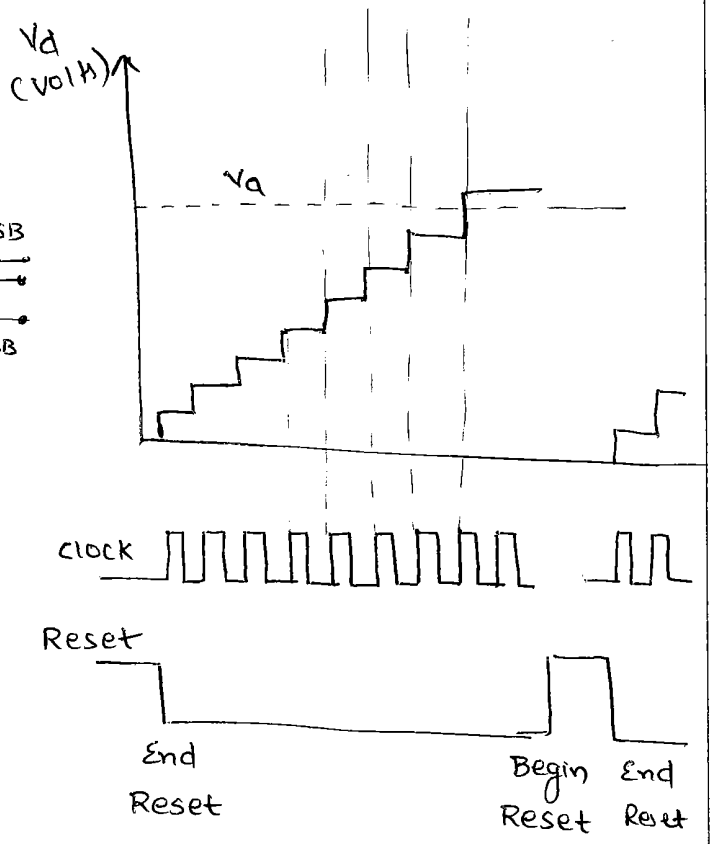


Fig (b): D/A output stair case waveform.

The counter is reset to zero count by the reset pulse. upon the release of reset, the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the binary counter. Voltage comparator high output. The number of pulses counted increase with time. The binary word representing this count is used as the input of the D/A converter whose output is the stair case shown in fig (b).

The analog output V_d of DAC is compared to the analog input V_a by the comparator. If $V_a > V_d$, the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter.

When $V_a < V_d$, the output of the Comparator becomes low and the AND gate is disabled. This stops the counting at the time $V_a \leq V_d$ and the digital output of the counter represents the analog input voltage V_a.

For a new value of analog input V_a, a second reset pulse is applied to clear the counter. upon the end of the reset, the counting begins again as shown in fig(b). The counter frequency must be low enough to give sufficient time for the DAC to settle and for the comparator to respond.

3) Successive Approximation converter:

The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods. ~~An~~

An Eight bit converter would require 8 clock pulses to obtain a digital output.

Fig (a) below shows an Eight bit Converter.

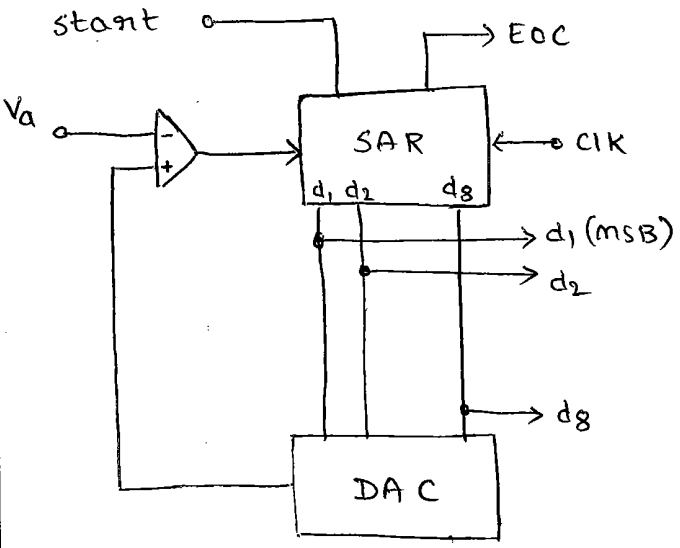


Fig: Functional diagram of the successive Approximation ADC

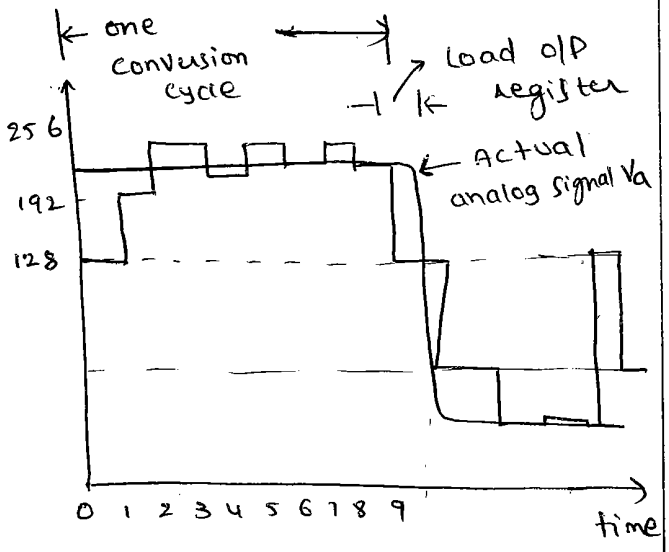


Fig: The D/A output voltage to become successively closer to the actual analog input voltage.

The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error.

The circuit operates as follows. With the arrival of the start command, the SAR sets the MSB $d_1 = 1$ with all other bits to zero so that the trial code is 10000000. The output V_d of the DAC is now Compared with analog input V_a. If V_a is greater than the DAC output V_d then 10000000 is less than the Correct digital representation.

The MSB is left at 1, and the next lower significant bit is made 1 and further tested.

correct digital representation	successive approximation register output V_d at different stages in the Conversion	comparator output
11010100	10000000	1 (Initial o/p)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig (c) : Successive approximation conversion sequence for a typical analog input.

However if V_a is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested.

Whenever DAC output crosses V_a, the comparator changes state and this can be taken as the end of conversion (EOC) command.

From fig(b) it can be seen that the D/A o/p voltage becomes successively closer to the actual analog i/p voltage. It requires 8 pulses to establish the

accurate output regardless of the value of the analog input. However, one additional clock pulse is used to load the output register and reinitialize the circuit.

Hence for an n-bit DAC, the number of clock pulses required to establish the accurate output is $(2^n + 1)$.

Integrating type ADC's :

1. Dual slope ADC :

Figure below shows the functional diagram of the dual slope or dual ramp converter. The analog part of the circuit consists of a high input impedance buffer A_1, precision integrator A_2 and a voltage comparator.

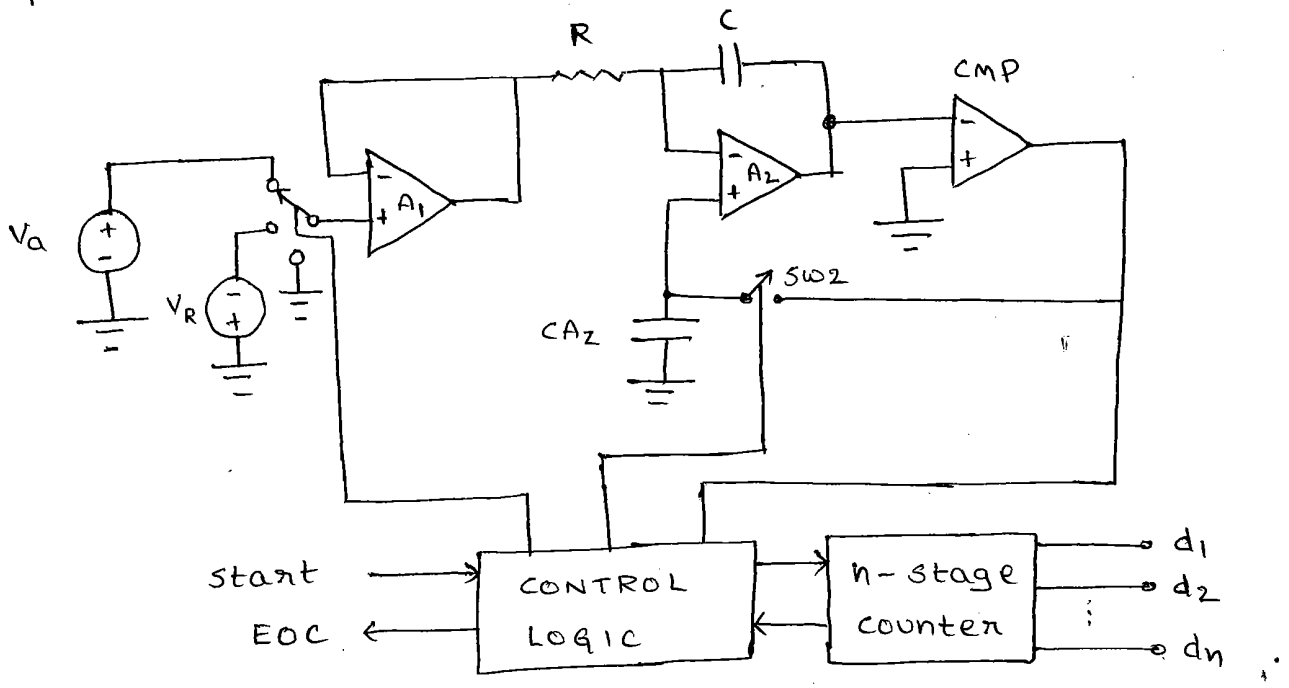
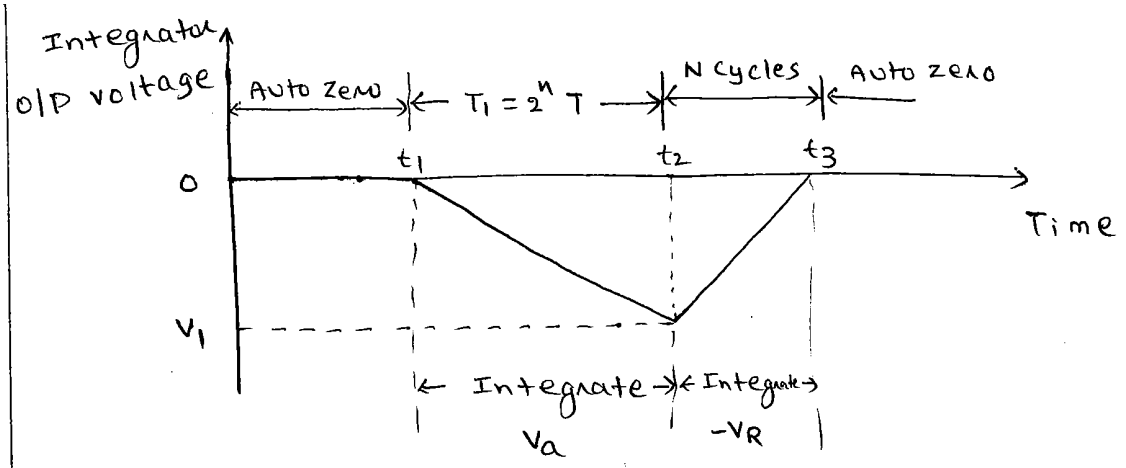


Fig (a) : Functional Diagram of the Dual slope ADC.



Fig(b): Integrated output wave form for the Dual slope ADC.

The converter first integrates the analog input signal V_a for a fixed duration of 2^n clock periods as shown in figure (b). Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero. The number N of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period. Hence N represents the desired output code.

The circuit operates as follows.

Before the start command arrives, the switch SW1 is connected to ground and SW2 is closed. Any offset voltage present in the A_1, A_2 and comparator loop after integration, appears across the capacitor C_{AZ} till the threshold of the comparator is achieved. The capacitor C_{AZ} thus provides automatic compensation

for the input offset voltages of all the three Amplifiers. Later when SW_2 opens C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled.

At the arrival of the START command at $t = t_1$, the control logic opens SW2 and connects SW1 to Va and enables the counter starting from zero. The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses.

The analog voltage Va is integrated for a fixed number 2^n counts of clock pulses after which the counter resets to zero. If the clock period is T, the integration takes place for a time $T_1 = 2^n \times T$ and the output is a ramp going downwards as shown in fig(b).

The counter resets itself at the end of the interval T_1 and the switch SW1 is connected to the reference voltage $(-V_R)$. The output voltage Vo will now have a positive slope. As long as V_o is negative, the output of the comparator is positive and the control logic allows the clock pulse to be counted.

However, when V_o becomes just zero at time $t = t_3$, the control logic issues and end of conversion (EOC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at t_3

is proportional to the analog input voltage V_a.

$$T_1 = t_2 - t_1 = 2^n T = \frac{2^n}{\text{clock rate}(f)} \longrightarrow (1)$$

and $$T_2 = t_3 - t_2 = \frac{\text{digital count}(N)}{\text{clock rate}} \longrightarrow (2)$$

For an integrator

$$\Delta V_0 = \left(\frac{-1}{RC}\right) V \Delta t$$

The voltage V_0 will be equal to V_1 at the instant t_2 and can be written as

$$V_1 = \left(\frac{-1}{RC}\right) V_a (t_2 - t_1) \longrightarrow (3)$$

The voltage V_1 is also given by

$$V_1 = \left(\frac{-1}{RC}\right)(-V_R)(t_2 - t_3) \longrightarrow (4)$$

From (3) & (4)

$$V_a (t_2 - t_1) = V_R (t_3 - t_2)$$

From (1) and (2)

$$V_a \frac{2^n}{\text{clock rate}} = V_R \frac{N}{\text{clock rate}}$$

$$\therefore V_a = V_R \left(\frac{N}{2^n}\right)$$

Here since V_R and n are constant, the analog voltage V_a is proportional to the count reading N and is indep[illegible] of R, C and T

Problem: A dual slope ADC uses a 16 bit counter and a 4MHz clock rate. The maximum input voltage is +10V, the maximum integrator output voltage should be -8V when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1 μF. Find the value of the resistor R of the integrator.

Solution:

Time period $t_2 - t_1 = \frac{2^n}{\text{clock rate}} = \frac{2^{16}}{4M} = 16.38\text{ms}$

For the integrator

$$\Delta V_0 = \left(\frac{-1}{RC}\right) V_a \ (t_2 - t_1)$$

$$\Delta V_0 = V_1 = -8; \quad V_a = 10\text{V}$$

$$RC = -\left(\frac{10}{-8\text{V}}\right) = 20.47\text{ms}$$

$$R = \frac{20.47\text{ ms}}{0.1\,\mu\text{F}} = 204.7\text{K}\Omega = 205\text{K}\Omega$$

Problem: If the analog signal V_a is 4.129V in the above example, find the equivalent digital number.

Solution: since $V_a = V_R \left(\frac{N}{2^n}\right)$

So the digital count $N = \left(\frac{V_a}{V_R}\right) 2^n$

$$N = 2^{16} \times \frac{10}{8}$$

$N = 33825$, for which the binary equivalent is **1000010000100001**

DAC | ADC Specifications:

Both DAC and ADC are available with wide range of specifications. the various important specifications of converters generally specified by the manufacturers are analysed.

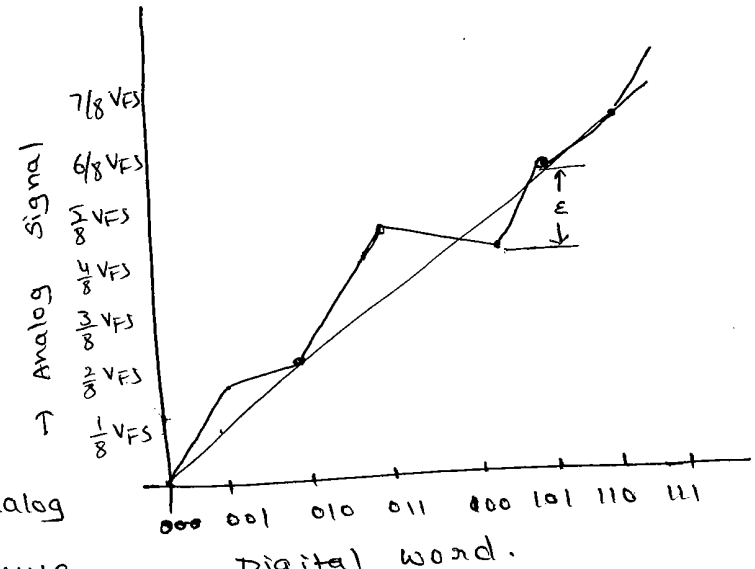
1. **Resolution:** the Resolution of a Converter is the smallest change in voltage which may be produced at the output of the converter. For ex

For example an 8-bit D/A Converter has $2^8 - 1 = 255$ intervals (equal). Hence the smallest change in output voltage is $\frac{1}{255}$ of the full scale output range. In short

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1 \text{ LSB increment.}$$

Similarly the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output.

(2) **Linearity:** the Linearity of an A/D or D/A converter is an important measure of its accuracy. and it tells us how close the converter output to its ideal transfer characteristics. In an ideal DAC, equal increment in the digital input should produce equal increment in the ~~digital~~ analog output and the transfer curve



However in the actual DAC, output voltages do not fall on a straight line because of gain and offset errors - the static performance of a DAC is determined by fitting a straight line through the measured output points. the linearity error measures the deviation of the actual output from the fitted line.

3) Accuracy : Absolute Accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed.

4) Monotonicity :

A monotonic DAC is the one whose analog output increases for an increase in digital input.

Fig shows the transfer curve for a non-monotonic DAC, since the output decreases when input code changes from 001 to 010.

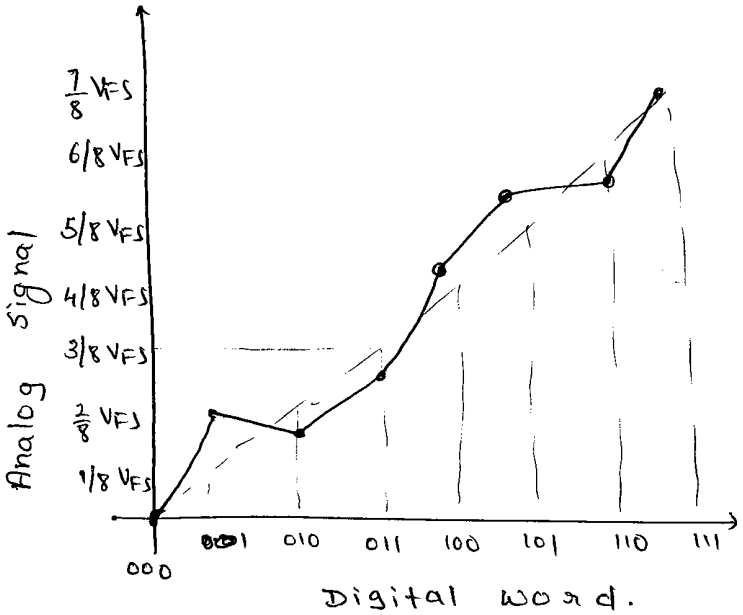


Fig: A Non monotonic 3-bit DAC

A monotonic DAC characteristic is essential in control applications, otherwise oscillations can result.

If a DAC has to be monotonic, the error should be less than $\pm \frac{1}{2}$ LSB at each output level

5) settling time: Settling time represents the time it takes for the output to settle with in a specified band $\pm \frac{1}{2}$ LSB of its final value following a code change at the input. It depends upon the switching time of the logic circuitary due to internal parasitic capacitances and inductances.

6) stability: the performance of converter changes with temperature, age and power supply variations. so all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

Problem:

1. How many levels are possible in a two-bit DAC? what is its resolution if the output range is 0 to 3 V?

Solution: Levels $= 2^2 = 4$ levels $\left[\because n = 2\right)$

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1} = \frac{3}{3} = 1\text{ V}$$