ACADEMIC REGULATIONS
COURSE STRUCTURE AND DETAILED SYLLABUS
FOR
M.TECH
VLSI SYSTEM DESIGN
FOR M.TECH.TWO YEAR POST GRADUATE COURSE
(APPLICABLE FOR THE BATCHES ADMITED FROM 2015-2016)

REGULATION:R15

INSTITUTE OF ENGINEERING & TECHNOLOGY
(UGC Autonomous)
(Accredited by NAAC, Approved by AICTE
& Permanently Affiliated to JNTUH)

J.B.INSTITUTE OF ENGINEERING & TECHNOLOGY
UGC AUTONOMOUS
(Permanently Affiliated to JNTUH,Approved By AICTE,New Delhi and Accredited By NBA,NAAC)

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J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY
UGC AUTONOMOUS

(BHASKAR NAGAR, MOINABAD MANDAL,R.R.DIST,HYDERABAD-500075,TELANGANA,INDIA)

R 15 - ACADEMICREGULATIONS (CBCS) FORM. Tech. (REGULAR) DEGREE PROGRAMMES

Applicable for the students of M. Tech. (Regular) programme from the Academic Year ***2015-16*** andonwards

The M. Tech. Degree of Jawaharlal Nehru Technological University Hyderabad shall be conferred on candidates who are admitted to the programme and who fulfill all the requirements fortheawardoftheDegree.

1.0 ELIGIBILITY FORADMISSIONS

Admission to the above programme shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.0 AWARD OFM. Tech. DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years. However, he is permitted to write the examinations for two more years after four academic years of course work, failing which he shall forfeit his seat in M. Tech. programme.

2.2 The student shall register forall88 creditsandsecureallthe88credits.

2.3 The minimum instruction days in each semester are90.

3.0 COURSESOFSTUDY

The following specializations are offered at present for the M. Tech. programme of study.

1. CAD / CAM
2. Computer Science and Engineering
3. Electrical Power Systems
4. Energy Systems
5. Software Engineering
6. Structural Engineering
7. VLSI System Design

3.1 Departments offering M. Tech. Programmes with specializations are noted below:

CIVIL ENGINEERING	STRUCTURAL ENGINEERING
COMPUTER SCIENCE & ENGINEERING	COMPUTER SCIENCE & ENGINEERING SOFTWARE ENGINEERING
ELECTRONICS & COMMUNICATION ENGINEERING	VLSI SYSTEM DESIGN
ELECTRICAL & ELECTRONICS ENGINEERING	ELECTRICAL POWER SYSTEMS ENERGY SYSTEMS
MECHANICAL ENGINEERING	CAD / CAM

4 Course Registration

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each student, who will advise him on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice/Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.

4.2 Academic Section of the College invites 'Registration Forms' from students with in 15 days from the commencement of classwork through 'ON-LINE SUBMISSIONS', ensuring 'DATE and TIME Stamping'. The ON-LINE Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply for ON-LINE Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries - during ON-LINE Registration for the Subject(s) / Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Subject/ Course in that Category will be taken into consideration.

4.5 Subject/ Course Options exercised through ON-LINE Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices will also not be considered. However, if the Subject/ Course that has already been listed for Registration (by the Head of Department) in a Semester could not be offered due to any unforeseen or unexpected reasons, then the Student shall be allowed to have alternate choice - either for a new Subject (subject to offering of such a Subject), or for another existing Subject (subject to availability of seats), which may be considered. Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

5 ATTENDANCE

The programmes are offered on a unit basis with each subject being considered a unit.

5.1 Attendance in all classes (Lectures/Laboratories etc.) is compulsory. The minimum required attendance in each theory / Laboratory etc. is 75% including the days of attendance in sports, games, NCC and NSS activities for appearing for the End Semester examination. A student shall not be permitted to appear for the Semester End Examinations (SEE) if his attendance is less than 75%.

5.2 Condonation of shortage of attendance in each subject up to 10% (65% and above and below75%) in each semester shall be granted by the College Academic Committee.

5.3 Shortage of Attendance below65% in each subject shall not be condoned.

5.4 Students whose shortage of attendance is not condoned in any subject are not eligible to write their end semester examination of that subject and their registration shall stand cancelled.

5.5 A prescribed fee shall be payable towards condonation of shortage of attendance.

5.6 A Candidate shall put in a minimum required attendance at least three (3) theory subjects in I Year I semester for promoting to I Year II Semester. In order to qualify for the award of the M.Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

5.7 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present Semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission in to the same class.

6 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

6.1 For the theory subjects 75 marks shall be awarded for the performance in the Semester End Examination and 25 marks shall be awarded for Continuous Internal Evaluation (CIE). The Continuous Internal Evaluation shall be made based on the average of the marks secured in the two Mid Term-Examinations conducted, one in the middle of the Semester and the other, immediately after the completion of Semester instructions. Each mid-term examination shall be conducted for a total duration of 120 minutes with Part A as compulsory question (10 marks) consisting of 5 sub-questions carrying 2 marks each, and Part B with 3 questions to be answered out of 5 questions, each question carrying 5 marks. The details of the Question Paper pattern for End Examination (Theory) are given below:

- The Semester End Examination will be conducted for 75 marks. It consists of two parts. i).Part-A for 25 marks, ii). Part-B for 50 marks.
- Part-A is a compulsory question consisting of 5 questions, one from each unit and carries 5 marks each.
- Part-B to be answered 5 questions carrying 10 marks each. There will be two questions from each unit and only one should be answered.

6.2 For practical subjects, 75 marks shall be awarded for performance in the Semester End Examinations and 25 marks shall be awarded for day-to-day performance as Internal Marks.

6.3 For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Principal of the College and the same to be informed to the Director of Evaluation in two weeks before for commencement of the lab end

examinations. The external examiner should be selected from outside the College concerned but within the cluster. No external examiner should be appointed from any other College in the same cluster/any other cluster which is run by the same Management.

6.4 There shall be two seminar presentations during I year I semester and II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50marks. A candidate has to secure a minimum of 50%ofmarks to be declared successful. If he fails to fulfill minimum marks, he has to reappear during the supplementary examinations.

6.5 There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce is intended to assess the students' understanding of various subjects he has studied during the M. Tech. course of study. The Head of the Department shall be associated with the conduct of the Comprehensive Viva-Voce through a Committee. The Committee consisting of Head of the Department, one senior faculty member and an external examiner. The external examiner shall be appointed by the Director of Evaluation. For this, the Principal of the College shall submit a panel of 3 examiners. There are no internal marks for the Comprehensive Viva-Voce and evaluates for maximum of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful. If he fails to fulfill minimum marks, he has to reappear during the supplementary examinations.

6.6 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the Semester End Examination and a minimum aggregate of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together.

6.7 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 6.6) he has to reappear for the Semester End Examination in that subject.

6.8 A candidate shall be given one chance to re-register for the subjects if the internal marks secured by a candidate is less than 50% and failed in that subject for maximum of two subjects and should register within four weeks of commencement of the class work. In such a case, the candidate must re-register for the subjects and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the Semester End Examination in those subjects. In the event of the student taking another chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stands cancelled.

6.9 In case the candidate secures less than the required attendance in any subject, he shall not be permitted to write the Semester End Examination in that subject. He shall re-register for the subject when next offered.

7 Examinations and Assessment - The Grading System

7.1 Marks will be awarded to indicate the performance of each student in each Theory Subject, or Lab/Practicals, or Seminar, or Project, etc., based on the % marks obtained in

CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item6above, and a corresponding Letter Grade shall be given.

7.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	*Letter Grade (UGC Guidelines)*	*Grade Points*
80% and above (□ 80% . ≤ 100%)	O (Outstanding)	10
Below 80% but not less than 70% (□ 70% . < 80%)	A^+ (Excellent)	9
Below 70% but not less than 60% (□ 60% . < 70%)	A (Very Good)	8
Below 60% but not less than 55% (□ 55% . < 60%)	B^+ (Good)	7
Below 55% but not less than 50% (□ 50% . < 55%)	B (above Average)	6
Below 50% (< 50%)	F (FAIL)	0
Absent	**Ab**	**0**

7.3 A student obtaining F Grade in any Subject shall be considered 'failed' and isbe required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered. In such cases, his Internal Marks (CIE Marks) in those Subjects will remain the same as those he obtained earlier.

7.4 A student not appeared for examination then 'Ab' Grade will be allocated in any Subject shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered.

7.5 A Letter Grade does not imply any specific Marks percentage and it will be the range of marks percentage.

7.6 In general, a student shall not be permitted to repeat any Subject/ Course (s) only for the sakeof 'Grade Improvement' or 'SGPA/ CGPA Improvement'.

7.7 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

7.8 The Student passes the Subject/ Course only when he **gets GP□ 6(B Grade or above).**

7.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit

Points (□ CP) secured **f**om ALL Subjects/ Courses registered in a Semester, by the Total is the no. of Subjects 'REGISTERED' for the Semester . SGPA is rounded off to **TWO** decimal places. SGPA is thus computed as

$$\textbf{SGPA} = \frac{\left\{\sum_{i=1}^{N} C_i G_i\right\}}{\left\{\sum_{i=1}^{N} C_i\right\}} \quad \textbf{……. For each semester.}$$

Where **'i'** is the subject indicator index (takes into account aii subjects in a semester), 'N' is the number of subjects **'registered'** for the semester (as specially required and listed under the course structure of the department). $\mathbf{G_i}$ is the number of credits allotted to the $\mathbf{i^{th}}$ subject, and $\mathbf{G_i}$ represents the grade points (GP) corresponding to the letter grade awarded for that $\mathbf{i^{th}}$subject.

7.10 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to tow decimal places. CGPA is thus computed from the I year II semester onwards at the end of each semester as per the formula.

$$\textbf{CGPA} = \frac{\left\{\sum_{j=1}^{M} C_j G_j\right\}}{\left\{\sum_{j=1}^{N} C_j\right\}} \quad \textbf{…….. For all S semester registered}$$

(i.e., up to and inclusive of S semester, S ≥ 2)

Where **'M'** is the total number of subjects (as specially required and listed under the course structure of the parent department) the student has **'registered'** i.e. from the first semester onwards upto and exclusive of the forth semester, "j" is the subject indicator index (takes in to account all subjects for one to four semester), C_j is the number of credits allotted to the j^{th} subject, G_i represents the grade points(GP) corresponding to the letter grade awarded for the j^{th} subject. After registration and completion of first year first semester, the SGPA of that semester itself may be taken as the CGPA, as there are no cumulative effects.

7.11 For Calculations listed in Item 7.6 – 7.10, performance in failed Subjects/ Courses (securing F Grade) will also be taken into account, and the Credits of such Subjects/ Courses will also be included in the multiplications and summations.

8. EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

8.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Departments offering the M. Tech. programme.

8.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

8.3 After satisfying 8.2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

8.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

8.5 A candidate shall submit his project status report in two stages at least with a gap of 3 months between them.

8.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

8.7 After approval from the PRC, the soft copy of the thesis should be submitted to the University for ANTI-PLAGIARISM for the quality check and the plagiarism report should be included in the final thesis. If the copied information is less than 24%, then only thesis will be accepted for submission.

8.8 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/School/Institute.

8.9 For Project work Review I in II Year I Sem. there is an internal marks of 50, the evaluation should be done by the PRC for 25 marks and Supervisor will evaluate for 25 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain. A candidate has to secure a minimum of 50% of marks to be declared successful for Project Work Review I. If he fails to fulfill minimum marks, he has to reappear during the supplementary examination.

8.10 For Project work Review II in II Year II Sem. there is an internal marks of 50, the evaluation should be done by the PRC for 25 marks and Supervisor will evaluate for 25 marks. The PRC will examine the overall progress of the Project Work and decide the Project is eligible for final submission or not. A candidate has to secure a minimum of 50% of marks to be declared successful for Project Work Review II. If he fails to fulfill minimum marks, he has to reappear during the supplementary examination.

8.11 For Project Evaluation (Viva Voce) in II Year II Sem. there is an external marks of 150 and the same evaluated by the External examiner appointed by the University. The candidate has to secure minimum of 50% marks in Project Evaluation (Viva-Voce) examination.

8.12 If he fails to fulfill as specified in 8.11, he will reappear for the Viva-Voce examination only after three months. In the reappeared examination also, fails to fulfill, he will not be eligible for the award of the degree.

8.13 The thesis shall be adjudicated by one examiner selected by the University. For this, the Principal of the College shall submit a panel of 3 examiners, eminent in that field, with the help of the guide concerned and Head of the Department.

8.14 If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unfavourable again, the thesis shall be summarily rejected.

8.15 If the report of the examiner is favourable, Project Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis.

8.16 The Head of the Department shall coordinate and make arrangements for the conduct of Project Viva- Voce examination.

9. AWARD OFDEGREEAND CLASS

9.1 A Student who registers for all the specified Subjects/ Courses as listed in the Course Sthe entire PG Programme (PGP), and secures the required number of **88** Credits (with CGPA 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with specialization as he admitted.

9.2 **Award of Class**

After a student has satisfied the requirements prescribed for the completion of the programme and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.75
First Class	6.75≤CGPA < 7.75
Second Class	6.00≤CGPA < 6.75

9.3 A student with final CGPA (at the end of the PGP) < 6.00 will not be eligible for the Award of Degree.

10. WITHHOLDING OFRESULTS

If the student has not paid the dues, if any, to the University or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be with held in such cases.

11. TRANSITORY REGULATIONS

11.1 If any candidate is detained due to shortage of attendance in one or more subjects, they are eligible for re-registration to maximum of two earlier or equivalent subjects at a time as and when offered.

11.2 The candidate who fails in any subject will be given two chances to pass the same subject; otherwise, he has to identify an equivalent subject as per R15 Academic Regulations.

12 GENERAL

12.1 **Credit**: A unit by which the course work is measured. It determines the number of hoursof instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

12.2 **Credit Point:** It is the product of grade point and number of credits for a course.

12.3 Wherever the words "he", "him", "his", occur in the regulations, they include "she", "her".

12.4 The academic regulation should be read as a whole for the purpose of any interpretation.

12.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

12.6 The College may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the College.

DISCIPLINARY ACTIO N FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractice/Improperconduct	**Punishment**
	If the student:	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which student is appearing but has not made use of (material shall include any marks on the body of the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other student orally or by any other body language methods or communicates through cell phones with any student or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in the subject only of all the students involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the student is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and UG major project and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The hall ticket of the student is to be cancelled and sent to the university.
3.	Impersonates any other student in connection with the examination.	The student who has impersonated shall be expelled from examination hall. The student is also debarred and forfeits the seat. The performance of the original student, who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and UG major project) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all university examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of sea. If the imposter is and outsider, he will be handed over to the police and a case is registered against him.

4.	Smuggles in the answer book or additional sheet or takes our or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in the subject and all the other subjects the student has already appeared including practical examinations and UG major project and shall not be permitted for the remaining examinations of the subjects of that semester year. The student is also debarred for two consecutive semesters from class work and all university examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the chief superintendent/assistant – superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizers a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or writer or by signs or by spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disruptthe orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the student(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The students also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the student has already appeared including practical examinations and UG major project and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all university examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat.

8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all other subjects the student has already appeared including practical examinations and UG major project and

		shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred and forfeiture of seat.
9.	If student of the college, who is not a student for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all the other subjects the student has already appeared including practical examinations and UG major project and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred and forfeiture of seat. Person(s) who do not belong to the college will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all other subjects the student has already appeared including practical examinations and UG major project and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of performance in that subject and all other subjects the student has appeared including practical examinations and UG major project of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the university for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments tothecandidates aspertheaboveguidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved inencouraging malpractices)
   - (i) Ashow causenoticeshall beissuedtothecollege.
   - (ii) Imposeasuitablefineonthecollege.
   - (iii) Shifting the examination centre from the college to another college for a specificperiodofnotlessthanoneyear.

S.No	CODE	Course Title	L	P	C
1	DM61A	VLSI Technology	4	0	4
2	DM61B	CMOS Analog Integrated Circuit Design	4	0	4
3	DM61C	CMOS Digital Integrated Circuit Design	4	0	4
	ELECTIVE-I:		4	0	4
4	DM61D	Digital System Design			
	DM61E	Hardware Software Co-Design			
	DM61F	CPLD and FPGA Architectures and Applications			
	ELECTIVE-II:		4	0	4
5	DM61G	Algorithms for VLSI Design Automation			
	DM61H	Embedded System Design			
	DM61I	Device Modeling			
	OPEN ELECTIVE-I		4	0	4
6	DM61J	Soft Computing Techniques			
	DM61K	Image and Video processing			
	DM61L	Software Defined Radio			
7	DM61M	VLSI Laboratory – I	0	4	2
8	DM61N	Seminar I	0	4	2
Total Credits			**24**	**8**	**28**

M.Tech I Year - II Semester

S.No	CODE	Course Title	L	P	C
1	DM62A	Low Power VLSI Design	4	0	4
2	DM62B	Design for Testability	4	0	4
3	DM62C	CMOS Mixed Signal Circuit Design	4	0	4
	ELECTIVE-III:		4	0	4
4	DM62D	VLSI and DSP Architectures			
	DM62E	Full custom IC Design			
	DM62F	Hardware Description Language			
	ELECTIVE-IV:				
5	DM62G	Optimization Techniques in VLSI Design	4	0	4
	DM62H	System On Chip Architecture			
	DM62I	Semiconductor Memory Design and Testing			
	OPEN ELECTIVE-II				
6	DM62J	Scripting Languages	4	0	4
	DM62K	Coding Theory and Techniques			
	DM62L	Adhoc Wireless Networks			
7	DM62M	VLSI Laboratory – II	0	4	2
8	DM62N	Seminar II	0	4	2
	Total Credits		24	8	28

S.No	CODE	Course Title	L	P	C

1	DM63A	**Comprehensive Viva-Voce**	0	0	4
2	DM63B	**Project work Review I**	0	24	12
Total Credits			0	**24**	**16**

II Year -I Semester

II Year -II Semester

S.No	**CODE**	**Course Title**	**L**	**P**	**C**
1	DM64A	**Project work Review II**	0	8	4
2	DM64B	**Project Evaluation (Viva-Voce)**	0	16	12
Total Credits			0	**24**	**16**

M.Tech – I Year – I Sem (VLSI System Design)

VLSI TECHNOLOGY

L	P	C
4	--	4

UNIT –I: Review of Microelectronics and Introduction to MOS Technologies

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II: Layout Design and Tools

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & Layouts:

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization. Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photo resists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

UNIT –IV: Doping and depositions

Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems; Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT –V: Design rules and Scaling, BICMOS ICs

Choice of transistor types, pnp transistors, Resistors, capacitors,
Packaging: Chip characteristics, package functions, package operations

TEXT BOOKS:

1.1 Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
1.2 C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000

REFERENCE BOOKS:

1. Micro Electronics circuits Analysis and Design 2nd Edition, Muhammad H Rashid, CENAGE Learning2011.
2. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999
3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000
4. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994

M. Tech – I Year – I Sem (VLSI System Design)

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

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UNIT -I: MOS Devices and Modeling

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II: Analog CMOS Sub-Circuits

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT –III: **CMOS Amplifiers**

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT –IV:CMOS Operational Amplifiers

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT –V: **Comparators**

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.

Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.

CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

M. Tech – I Year – I Sem. (VLSI System Design)

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

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UNIT –I: MOS Design

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II: Combinational MOS Logic Circuits

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III: Sequential MOS Logic Circuits

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV: Dynamic Logic Circuits

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V: Semiconductor Memories

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

M. Tech – I Year – I Sem. (VLSI System Design)
DIGITAL SYSTEM DESIGN
(Core Elective –I)

L	P	C
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UNIT -I:Minimization and Transformation of Sequential Machines

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II: Digital Design

Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III: SM Charts

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV:Fault Modeling & Test Pattern Generation

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location – Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:Fault Diagnosis in Sequential Circuits

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
1 Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
2 Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

M. Tech – I Year – I Sem. (VLSI System Design)
HARDWARE - SOFTWARE CO-DESIGN
(Core Elective –I)

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UNIT –I: Co- Design Issues
Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co- Synthesis Algorithms:
Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II: Prototyping and Emulation
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III: Compilation Techniques and Tools for Embedded Processor Architectures
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:Design Specification and Verification
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:Languages for System – Level Specification and Design-I
System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:
1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli,Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:
1. A Practical Introduction to Hardware/Software Co-design - Patrick R. Schaumont - 2010 – Springer

M. Tech – I Year – I Sem. (VLSI System Design)

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

(Core Elective –I)

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UNIT-I:Introduction to Programmable Logic Devices

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II:Field Programmable Gate Arrays

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:SRAM Programmable FPGAs

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV: Anti-Fuse Programmed FPGAs

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:Design Applications

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

M. Tech – I Year – I Sem. (VLSI System Design)
ALGORITHMS FOR VLSI DESIGN AUTOMATION
(Core Elective –II)

L	P	C
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UNIT I: PRELIMINARIES
Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II: GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION
Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III: LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING
Problems, Concepts and Algorithms. MODELLING AND SIMULATION
Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT IV: LOGIC SYNTHESIS AND VERIFICATION
Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis
HIGH-LEVEL SYNTHESIS
Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V: PHYSICAL DESIGN AUTOMATION OF FPGAs
FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs
MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin
– Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS

1. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.
2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005, Springer International Edition.

REFERENCE BOOKS

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design:Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia.

M. Tech – I Year – I Sem. (VLSI System Design)

EMBEDDED SYSTEMS DESIGN

(Core Elective –II)

L	P	C
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UNIT -I:Introduction to Embedded Systems

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II: Typical Embedded System

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III:Embedded Firmware

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV:RTOS Based Embedded System Design

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V: Task Communication

Shared Memory, Message Passing, Remote Procedure Call and Sockets,Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

M. Tech – I Year – I Sem. (VLSI System Design)
DEVICE MODELLING
(Core Elective –II)

L	P	C
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UNIT -I: Introduction to Semiconductor Physics
Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.
Integrated Passive Devices:
Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT -II: Integrated Diodes
Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models
Integrated Bipolar Transistor:
Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model-dynamic model, Parasitic effects – SPICE model –Parameter extraction

UNIT -III: Integrated MOS Transistor
NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT -IV: VLSI Fabrication Techniques
An overview of wafer fabrication, Wafer Processing–Oxidation–Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well-twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements

UNIT -V: Modeling of Hetero Junction Devices
Band gap Engineering, Band gap Offset at abrupt HeteroJunction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS:

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS:

1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

M. Tech – I Year – I Sem. (VLSI System Design)
SOFT COMPUTING TECHNIQUES
(Open Elective - I)

L	P	C
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UNIT – I: Fundamentals of Neural Networks & Feed Forward Networks

Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network :The Perceptron Model, Multilayer Feed Forward Neural Network :Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT – II: Associative Memories & ART Neural Networks

Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

UNIT – III: Fuzzy Logic & Systems

Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT – IV: Genetic Algorithms

Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Offsprings, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of Genetic Algorithm.

UNIT – V: Hybrid Systems

Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

TEXT BOOKS:

1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers
2. Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications - S.Rajasekaran, G.A. Vijayalakshmi Pai, July 2011, PHI, New Delhi.
3. Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006.
4. Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi,1994.

REFERENCE BOOKS:

1. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
2. An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998
3. Fuzzy Sets, Uncertainty and Information- Klir G.J. & Folger. T. A., PHI, Delhi, 1993.

M. Tech – I Year – I Sem. (VLSI System Design)

IMAGE AND VIDEO PROCESSING

(OPEN ELECTIVE-I)

L	P	C
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UNIT –I:Fundamentals of Image Processing and Image Transforms

Basic steps of Image ProcessingSystem Sampling and Quantization of an image, Basic relationship between pixels.

Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding,Region based segmentation.

UNIT –II:Image Enhancement

Spatial domain methods: Histogram processing, Fundamentals of Spatialfiltering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Basics of filtering in frequency domain, Image smoothing, Image sharpening, Selective filtering.

UNIT –III:Image Compression

Image compression fundamentals - Coding Redundancy, Spatial andTemporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT -IV:Basic Steps of Video Processing

Analog Video, Digital Video. Time-Varying Image Formationmodels: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT –V:2-D Motion Estimation

Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

1. Digital Image Processing – Gonzaleze and Woods, 3rd Ed., Pearson.
2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFRENCE BOOKS:

1. Digital Image Processing using MATLAB– Gonzaleze and Woods, 2nd ed., Mc Graw Hill Education, 2010
2. Image Processing Analysis , and Machine Vision- Milan Sonka, Vaclan Hlavac, 3 ed., CENGAGE, 2008
3. Digital Video Processing – A Murat Tekalp, PERSON, 2010
4. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar –TMH, 2009

M. Tech – I Year – I Sem. (VLSI System Design)
SOFTWARE DEFINED RADIO
(Open Elective-I)

L	P	C
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UNIT -I:Introduction

The Need for Software Radios, What is Software Radio, Characteristics and benefitsof software radio- Design Principles of Software Radio, RF Implementation issues- The Purpose of RF Front – End, Dynamic Range- The Principal Challenge of Receiver Design – RF Receiver Front-End Topologies- Enhanced Flexibility of the RF Chain with Software Radios- Importance of the Components to Overall Performance- Transmitter Architectures and Their Issues- Noise and Distortion in the RF Chain, ADC and DAC Distortion.

UNIT -II: Profile and Radio Resource Management

Communication Profiles- Introduction, CommunicationProfiles, Terminal Profile, Service Profile , Network Profile, User Profile, Communication Profile Architecture, Profile Data Structure, XML Structure, Distribution of Profile Data, Access to Profile Data, Management of Communication Profiles, Communication Classmarks, Dynamic Classmarks for Reconfigurable Terminals, Compression and Coding, Meta Profile Data

UNIT -III: Radio Resource Management in Heterogeneous Networks

Introduction, Definition of Radio Resource Management, Radio Resource Units over RRM Phases, RRM Challenges and Approaches, RRM Modelling and Investigation Approaches, Investigations of JRRM in Heterogeneous Networks, Measuring Gain in the Upper Bound Due to JRRM, Circuit-Switched System, Packet-Switched System, Functions and Principles of JRRM, General Architecture of JRRM, Detailed RRM Functions in Sub-Networks and Overall Systems

UNIT -IV: Reconfiguration of the Network Elements

Introduction, Reconfiguration of Base Stations andMobile Terminals, Abstract Modelling of Reconfigurable Devices, the Role of Local Intelligence in Reconfiguration, Performance Issues, Classification and Rating of Reconfigurable Hardware, Processing Elements, Connection Elements, Global Interconnect Networks, Hierarchical Interconnect Networks, Installing a New Configuration, Applying Reconfiguration Strategies, Reconfiguration Based on Comparison, Resource Recycling, Flexible Workload Management at the Physical Layer, Optimised Reconfiguration, Optimisation Parameters and Algorithms, Optimization Algorithms, Specific Reconfiguration Requirements, Reconfiguring Base Stations, Reconfiguring Mobile Terminals

UNIT -V:Object – Oriented Representation of Radios and Network Resources

Networks- Object Oriented Programming- Object Brokers- Mobile Application Environments- Joint Tactical Radio System.

Case Studies in Software Radio Design: Introduction and Historical Perspective, SPEAK easy-JTRS, Wireless Information Transfer System, SDR-3000 Digital Transceiver Subsystem, Spectrum Ware, CHARIOT.

TEXT BOOKS:

1. Software Defined Radio Architecture System and Functions- Markus Dillinger, Kambiz Madani, WILEY 2003
2. Software Defined Radio: Enabling Technologies- Walter Tuttle Bee, 2002, Wiley Publications.

REFERENCE BOOKS:

1. Software Radio: A Modern Approach to Radio Engineering - Jeffrey H. Reed, 2002,

PEA Publication.
2. Software Defined Radio for 3G - Paul Burns, 2002, Artech House.
3. Software Defined Radio: Architectures, Systems and Functions - Markus Dillinger, Kambiz Madani, Nancy Alonistioti, 2003, Wiley.
4. Software Radio Architecture: Object Oriented Approaches to wireless System Enginering – Joseph Mitola, III, 2000, John Wiley & Sons.

M. Tech – I Year – I Sem. (VLSI System Design)

VLSI LABORATORY – I

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Note:

- Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.

Design and implementation of the following CMOS digital/analog circuits using **Cadence / MentorGraphics / Synopsys / Equivalent** CAD tools. The design shall include Gate-level design,Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
11. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, Multiplication, and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits .

Part –II: VLSI Back End Design programs:

Design and implementation of the following CMOS digital/analog circuits using **Cadence / MentorGraphics / Synopsys / Equivalent** CAD tools. The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
    - Basic logic gates CMOS
    - inverter
    - CMOS NOR/ NAND gates CMOS XOR and
    - MUX gates CMOS
    - 1-bit full adder
    - Static / Dynamic logic circuit
    - (register cell) Latch
    - Pass transistor

Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths.

M. Tech – I Year – II Sem. (VLSI System Design)

LOW POWER VLSI DESIGN

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UNIT –I: Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II:

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, ArchitecturalLevel Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches:

System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.

3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

M. Tech – I Year – II Sem. (VLSI System Design)

DESIGN FOR TESTABILITY

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UNIT -I:Introduction to Testing

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II:Logic and Fault Simulation

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III:Testability Measures

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV: Built-In Self-Test

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:Boundary Scan Standard

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK:

1 Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:

2. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
3. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

M. Tech – I Year – II Sem. (VLSI System Design)

CMOS MIXED SIGNAL CIRCUIT DESIGN

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UNIT -I:Switched Capacitor Circuits
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT -II:Phased Lock Loop (PLL)
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT -III:Data Converter Fundamentals
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters-Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV:Nyquist Rate A/D Converters
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V:Oversampling Converters
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

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VLSI AND DSP ARCHITECTURES

(Core Elective –III)

L	P	C
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UNIT I

Essential feature of Instruction set architectures of CISC, RISC and DSP processors and their implications for implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor. Assessing understanding performance, Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls

UNIT II: **Data Path and Control**

Introduction, logic design conventions, building a data path, a simpleimplementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls

UNIT III: **Enhancing performance with pipeline**

An overview of pipelining, a pipe lined data path. Pipe linedcontrol, data hazards and forwarding, data hazards and stalls, branch hazards using a hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls

UNIT IV: **Computational Accuracy in DSP implementations**

Introduction, number formats for signals andcoefficients in DSP system, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors, D /A conversion errors

UNIT V: **Architectures for programmable digital signal processing devices**introduction, basicarchitectural features, DSP Computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

TEXT BOOKS:

1. Computer Organization and Design: Hard ware/ Software Interface-D.A, Patterson and J.L Hennessy, 4th ed., Elsevier, 2011
2. Structural Computer organization, A.S Tannenbaum, 4th ed., Prentice-Hall, 1999

REFERENCE BOOKS:

1. W. Wolf, Modern VLSI Design: System on Silicon, 2nd Ed., Person Education,1998
2. Keshab Parhi, VLSI Digital Signal Processing system design and implementations, Wiley 1999
3. Avatar sign, Srinivasan S, Digital Signal Processing implementations using DSP microprocessors with examples, Thomson 4th reprint, 2004.

M. Tech – I Year – II Sem. (VLSI System Design)

FULL CUSTOM DESIGN

(Core Elective –III)

L	P	C
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UNIT I: Introduction

Schematic fundamentals, Layout design, Introduction to CMOS VLSI manufacturing processes, Layers and connectivity, Process design rules Significance of full custom IC design, layout design flows.

UNIT II

Advanced techniques for specialized building blocks Standard cell libraries, Pad cells and Laser fuse cells, Advanced techniques for building blocks, Power grid Clock signals and

UNIT III

Interconnect routing. Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics.

UNIT IV

Layout considerations due to process constraints Large metal via implementations, Step coverage rules, Special design rules, Latch-up and Guard rings, Constructing the pad ring, Minimizing Stress effects.

UNIT V

Proper layout CAD tools for layout, Planning tools, Layout generation tools, Support tools.

TEXT BOOKS:

1. CMOS IC Layout Concepts Methodologies and Tools, Dan Clein, Newnes, 2000.
2.The Art of Analog Layout, 2nd Edition, Ray Alan Hastings, Prentice Hall, 2006

M. Tech – I Year – II Sem. (VLSI System Design)

HARDWARE DESCRIPTION LANGUAGE

(Core Elective –III)

L	P	C
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UNIT I: Introduction

About VHDL, Design Flows & EDA Tools, Code Structure, Data types, Operators and Attributes: Operators, Attributes, User-Defined Attributes, Operator, overloading

UNIT II: Concurrent Code

Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code: Process, Signals and Variables, IF, WAIT, CASE, Using Sequential, Code To Design Combinational Circuits

UNIT III: State Machines

Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to OneHot

UNIT IV: Introduction to Verilog-AMS

Verilog Family of Languages, Mixed Signal Simulators, Applications of Verilog-AMS, Analog Modeling.

UNIT V: Language Reference

Basics, Data Types, Signals, Expressions, Analog Behavior

TEXT BOOKS

1. Circuit Design and Simulation with VHDL, Volnei A. Pedroni, 2nd Edition, MIT Press, 2010.
2. Designers Guide to Verilog AMS, Kenneth S Kundert, Olaf Zinke, Springer, 2004

M. Tech – I Year – II Sem. (VLSI System Design)

OPTIMIZATION TECHNIQUES IN VLSI DESIGN

(Core Elective –IV)

L	P	C
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UNIT –I:Statistical Modeling

Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom" s model, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT –II:Statistical Performance, Power and Yield Analysis

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT –III:Convex Optimization

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting-Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT –IV:Genetic Algorithm

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

UNIT –V:GA Routing Procedures and Power Estimation

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

TEXT BOOKS / REFERENCE BOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.
3. Convex Optimization - Stephen Boyd, Lieven Vandenberghe, Cambridge University Press, 2004.

M. Tech – I Year – II Sem. (VLSI System Design)

SYSTEM ON CHIP ARCHITECTURE

(Core Elective –IV)

L	P	C
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UNIT –I:Introduction to the System Approach:
System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II: Processors
Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III:Memory Design for SOC
Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV:Interconnect Customization and Configuration
Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V:Application Studies / Case Studies
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

M. Tech – I Year – II Sem. (VLSI System Design)

SEMICONDUCTOR MEMORY DESIGN AND TESTING

(Core Elective –IV)

L	P	C
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UNIT -I: Random Access Memory Technologies

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT -II:Non-volatile Memories

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT -III:Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance

RAMfault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT -IV:Semiconductor Memory Reliability and Radiation Effects

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT -V:Advanced Memory Technologies and High-density Memory Packing Technologies

FerroelectricRAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

M. Tech – I Year – II Sem. (VLSI System Design)

SCRIPTING LANGUAGES

(Open Elective-II)

L	P	C
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UNIT -I: Introduction to Scripts and Scripting

Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT -II: Advanced PERL

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT -III: TCL

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT -IV: Advanced TCL

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT -V: TK and JavaScript:

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK.

JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes,Encapsulation, Data Hierarchy.

TEXT BOOKS:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

REFERENCE BOOKS:

1. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann SerieS.
2. Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindel Edition.
3. Tcl 8.5 Network Programming book- Wojciech Kocjan and Piotr Beltowski, Packt Publishing.
4. Tcl/Tk 8.5 Programming Cookbook- Bert Wheeler

M. Tech – I Year – II Sem. (VLSISystem Design)

CODING THEORY AND TECHNIQUES

(Open Elective-II)

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UNIT – I: Coding for Reliable Digital Transmission and storage

Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, MinimumDistance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - II: Cyclic Codes

Description, Generator and Parity-check Matrices, Encoding, Syndrome Computationand Error Detection, Decoding ,Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT – III:Convolutional Codes

Encoding of Convolutional Codes, Structural and Distance Properties,maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT – IV: Turbo Codes

LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolutional codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding

UNIT - V: Space-Time Codes

Introduction, Digital modulation schemes, Diversity, Orthogonal space- Time Block codes, Alamouti's schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing : General Concept, Iterative APP Preprocessing and Per-layer Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi – Layer Detection Schemes, Unified Description by Linear Dispersion Codes.

TEXT BOOKS:

1. Error Control Coding- Fundamentals and Applications –Shu Lin, Daniel J.Costello,Jr, Prentice Hall, Inc.
2. Error Correcting Coding Theory-Man Young Rhee- 1989, McGraw-Hill

REFERENCE BOOKS:

1. Error Correcting Coding Theory-Man Young Rhee-1989,McGraw – Hill Publishing,
2. Digital Communications-Fundamental and Application - Bernard Sklar, PE.
3. Digital Communications- John G. Proakis, 5th ed., 2008, TMH.
4. Introduction to Error Control Codes-Salvatore Gravano-oxford
5. Error Correction Coding – Mathematical Methods and Algorithms – Todd K.Moon, 2006, Wiley India.
6. Information Theory, Coding and Cryptography – Ranjan Bose, 2nd Edition, 2009, TMH.

M. Tech – I Year – II Sem. (VLSI System Design)

AD-HOC WIRELESS NETWORKS

(Open Elective-II)

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UNIT - I: Wireless Local Area Networks

Introduction, wireless LAN Topologies, Wireless LAN Requirements,

Physical Layer- Infrared Physical Layer, Microwave based Physical Layer Alternatives, Medium Access Control Layer- HIPERLAN 1 Sublayer, IEEE 802.11 MAC Sublayer and Latest Developments-802.11a, 802.11b, 802.11g

Personal Area Networks: Introduction to PAN technology and Applications, Bluetooth - specifications, Radio Channel, Piconets and Scatternets, Inquiry, Paging and Link Establishment, Packet Format, Link Types, Power Management, Security, Home RF - Physical and MAC Layer

UNIT - II:MAC Protocols

Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT - III: Routing Protocols

Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT – IV: Transport Layer Protocols

Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT – V: Quality of Service in Ad Hoc Wireless Networks:

Introduction, Real Time Traffic Support in Ad Hoc Wireless Networks, QoS Parameters in Ad Hoc Wireless Network, Issues and Challenges in providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions: MAC Layer Solutions, Cluster TDMA, IEEE 802.11e, DBASE, Network Layer Solutions, QoS Routing Protocols, Ticket Based QoS Routing Protocol, Predictive Location Based QoS routing protocol, Trigger Based Distributed QoS Routing Protocol, QoS enabled AODV Routing Protocol, Bandwidth QoS Routing Protocol, On Demand QoS Routing Protocol, On Demand Link-State Multipath QoS Routing Protocol, Asynchronous Slot Allocation Strategies. QoS Frameworks for Ad Hoc Wireless Networks.

TEXT BOOKS:

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Networks -P Nicopolitidis and M S Obaidat, Wiley India Edition 2003.

REFERENCE BOOKS

1. Wireless Communication Technology- Roy Blake, CENGAGE,2012
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press.

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VLSI LABORATORY - II

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Note: All the following digital/analog circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

VLSI Back End Design programs:

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
   - CMOS inverter
   - CMOS NOR/ NAND gates
   - CMOS XOR and MUX gates
   - CMOS half adder and full adder
   - Static / Dynamic logic circuits (register cell)
   - Latch
   - Pass transistor
3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
4. Introduction to SPICE simulation and coding of NMOS/CMOS circuit
5. SPICE simulation of basic analog circuits: Inverter / Differential amplifier
6. Analog Circuit simulation (AC analysis) – CS & CD amplifier
7. System level design using PLL