Department of Information Technology

Computer Organization & Digital logic Design

II B.Tech -I Sem

V. SWAPNA
Asst. Professor

J.B.Institute of Engg & Technology

Yenkapally, Moinabad(Mandal)
Himathnagar(post),Hyderabad

Results Target

Total Strength of the Class:

S. No	Class / Division	No. of Students
a.	**First Class with Distinction**	
b.	**First Class**	
c.	**Pass Class**	

Method of Evaluation

a.	**Internal Examination**	**2**
b.	**Unit Wise Assignments**	**4**
c.	**Descriptive Exam**	**2**
d	**Objective**	**2**
e.	**Final Examination**	**1**

Course Objective

. The objective of this course is to master the basic hardware and software issues of computer organization. At the end of the course, the students are expected to know the inner workings of a computer and have the ability to analyze the hardware and software issues related to computers and the interface between the two. This allows the students to work out the tradeoffs involved in designing a modern computer.

J.B.Institute of Engg & Technology

Department of Information Technology

Syllabus

Subject Name: Computer Organization & Digital logic Design **Subject Code : 53037**

Class : II B.Tech

Sl.No	Unit No:	Details of the unit
01	Unit I	Computer types
		Functional units
		Basic operational concepts
		Bus structures, software, performance
		Multiprocessors, multi computers
		Computer generations, binary numbers
		Fixed point representation, floating point representation
		Number base conversions, octal and hexadecimal numbers, complements
		Signed binary numbers, binary codes
02	Unit II	Basic logic functions, logic gates
		Universal logic gates
		Minimization of logic expressions
		Flip flops
03	Unit III	Registers
		Shift registers, binary counters
		Decoders, multiplexers
		Programmable logic devices
04	Unit IV	Algorithms for fixed point and floating point addition
		Subtraction, multiplication and division operations
		Hardware implementation of arithmetic and logic operations
		High performance arithmetic
05	Unit V	Memory locations and addresses
		Machine addresses and sequencing
		Various addressing modes
		Instruction formats, basic machine instructions
		IA-32 Pentium example

06	**Unit VI**	Introduction to CPU, register transfers
		Execution of instructions
		Multiple bus organization
		Hard wired control
		Micro programmed control
07	**Unit VII**	Concept of memory, RAM ROM memories
		Memory hierarchy, cache memories, virtual memory
		Secondary storage, memory management requirements
08	**Unit VIII**	Introduction to I/O, interrupts hardware
		Enabling and disabling interrupts
		Device control, direct memory access
		Buses, interface circuits
		Standard I/O interfaces

Guidelines to Students

Where will this subject help?

. Principles of Computer Organization answers the question "How do computers work?". It examines the underlying components and the basic organizing principles in the construction of computer systems. It includes an examination of transistors and simple logic circuits, micro-processor components, microcode, machine language, assembly language, operating systems, and a variety of machine architectures. By studying the fundamental organizing principles of computer systems, we are better able to understand, design, and implement complex systems

Books / Material

Text Books (TB)

TB1: COMPUTER ORGANIZATION-Carl Hamacher, Zvonko Vranesic, safwat zaky, 5th edition, McGraw hill.

TB2: COMPUTER ARCHITECTURE AND ORGANIZATION- an integrated approach, miles murdocca, Vincent heuring, second edition, wiley india

TB3: COMPUTER SYSTEMS ARCHITECTURE-M.Moris mano, 3rd edition pearson

Suggested / Reference Books (RB)

RB1: computer organization and architecture- william stallings 6th edition pearson

RB2:computer organization and design- david a.paterson and john l.hennessy-elsevier

RB3:fundamentals or computer organization and design- sivarama dandamudi springer int. edition

RB4: digital design – 3rd edition m.morris mano, pearson education/phi

RB5: fundamentals of logic design, roth, 5th edition thomson

J.B.Institute of Engg & Technology

Department of Information Technology

SUBJECT PLAN :

Subject Name : Computer Organization & Digital logic Design Subject Code : 53037

Class : II B.Tech Faculty Name : V.Swapna

Number of Hours / lectures available in this Semester / Year	**65**

Unit	Topic	Total No. of Hours
I	Computer types, functional units, basic operational concepts	10
	Bus structures, software, performance	
	Multiprocessors and multi computers, computer generations	
	Binary numbers, fixed point representation	
	Number base conversions	
	Complements, signed binary numbers, binary codes	
	Octal and hexadecimal numbers	
	Floating point representation	
II	Basic logic functions, logic gates	07
	Universal logic gates	
	Minimization of logic expressions	
	Flip flops	
III	Registers, shift registers	07
	Binary counters	
	Decoders	
	multiplexers	
	Programmable logic devices	
IV	Algorithms for fixed point and floating point addition	10
	Subtraction, multiplication, and division operations	
	Hardware implementation of arithmetic and logic operations	
	High performance arithmetic	

V	Memory locations and addresses	**7**
	Machine addresses and sequencing	
	Various addressing modes	
	Instruction formats	
	Basic machine instructions	
	IA-32 Pentium example	
VI	Introduction to CPU	**7**
	Register transfer	
	Execution of instructions	
	Multiple bus organization	
	Hardwired control, micro programmed control	
VII	Concept of memory	**10**
	RAM, ROM memories	
	Memory hierarchy	
	Cache memories	
	Virtual memory	
	Secondary storage	
	Memory management requirements	
VIII	Introduction to I/O	**7**
	Interrupts hardware	
	Enabling and disabling interrupts	
	Device control	
	Direct memory access, buses	
	Interface circuits, standard I/O interfaces	
	Total	**65**

J.B.Institute of Engg & Technology

Department of Information Technology

LESSON PLAN :

Subject Name : Computer Organization & Digital logic Design Subject Code : 53037

Class : II B.Tech Faculty Name : V.Swapna

Unit I : Basic structure of computers and data representation
LEARNING OBJECTIVES: Deals with basic units and internal structure of computer.

Students will be learning all the number base conversions

LECTURE PLAN:

Total no_ of classes: 10

Unit #	Topic as per JNTU syllabus	Lesson #	Suggested Books ** (Refer the list	Question Bank			Hand outs
				OQ	DQ	AQ	
Unit I	Computer types, functional units, operational concepts	01	T1				
	Bus structures, software, performance, computer generations	02	T1				
	Number base conversions, complements	03	T1				
	Signed binary numbers, binary codes	04	T1				
	Fixed pt representation, floating pt representation	05	T1				

OBJECTIVE QUESTIONS :

1. (623.77)8 =3D (?)16 **Ans:- 193.FC**

2. Convert 172 in octal to decimal **Ans:122**

3. Convert the binary number 001100111010 into octal number = **Ans:1472**

4. In the signed magnitude representation -4 is represented as **Ans:1100**

5. Find the 1's complement of the binary number 0101 = **Ans:1010**

6. Inside today's computers, data is represented **as Ans: zeros and ones**

7. Binary uses a powers of **Ans:2**

8. Group of eight bits are called **Ans: bytes**

9. The decimal equivalent of 0000000111 is **Ans:7**

10. Octal is most useful when the binary sequence is multiples of **= Ans: three**

11. Hexa decimal is most useful when the binary sequence is multiples = of **Ans: four**

DESCRIPTIVE QUESTIONS :

1. convert the following i.$(465.85)_{10}$ to binary, octal, hexadecimal ii.$(110011001111000)_2$ to octal, hexadecimal.

2. Perform subtraction operation using 10's complement i.1753-8640 ii.1200-250

ASSIGNMENT QUESTIONS:

1. convert the following i.$(465.85)_{10}$ to binary, octal, hexadecimal ii.$(110011001111000)_2$ to octal, hexadecimal.

2. Perform subtraction operation using 10's complement i.1753-8640 ii.1200-250

3. Represent the number +46.5 as a floating point binary number

4. Write details about fixed point representation with example, perform addition and subtraction.

5. Give details about performance measurement.

UNIT-II : DIGITAL LOGIC CIRCUITS-I
LEARNING OBJECTIVES:

Learn about logic gates and logic expressions

LECTURE PLAN:
Total No_ of Classes: 07

S.No	Name of the Topic	Reference book code	No. of classes required
06	Basic logic functions	T2	1
07	Logic gates	T2	1
08	Universal logic gates	T2	1
09	Minimization of logic expressions	T2	1

10	Minimization of logic expressions	T2	1
11	Flip flops	T2	1
12	Flip flops	T2	1

OBJECTIVE QUESTIONS :

1. The multiplicative identity in Boolean algebra is **Ans:1**
2. Reduce the Boolean expression A'C' + ABC + AC' to three literals **Ans: AB + C'**
3. The additive identity in Boolean algebra is **Ans:0**
4. The number of rows in the truth table of a Boolean function with n = variables is **Ans:2n**
5. Max term is the complement of its corresponding = A**ns: min term**
6. A Boolean function can be transformed from an algebraic expression = into a circuit composed of **Ans:logic gates**
7. Express the Boolean function F=3DA+B'C in a sum of min terms
Ans:- =3DA'B'C+AB'C+AB'C+ABC'+ABC
8. The number of min terms formed from n variables are **Ans:2n**
9. The Min term is obtained from **Ans:-an AND term of n variables**
10. The max term is also called **Ans:-standard sums**
11. The equivalence function is also called **Ans: XNOR**
12. A positive logic AND gate can operate as a **Ans:- negative = logic OR**
13. The number of min terms for a three variable map is **Ans:8**
14. Which of the following is used to convert the sum of products to = product of sums **Ans:- De Morgan's**
15. The logical sum of min terms associated with a Boolean function = specifies the conditions under which the function is equal **to Ans:1**

DESCRIPTIVE QUESTIONS :

1. Draw the logic diagram corresponding to following expression without simplifying them i.(A+B)(C+D)(A'+B+D) ii.(AB+A'B')(CD'+C'D)
2. Obtain the complement of the following Boolean expression i. x'yz+x'yz'+xy'z'+xy'z
ii. (x+y'+z')(x+y'+z)(x'+y+z)(x'+y+z')
3. Obtain the simplified expression of SOP form using k-map method. F(A,B,C,D,E)=∑(0,1,4,5,16,17,21,25,29)

ASSIGNMENT QUESTIONS:

1. Obtain the complement of the following Boolean expression i. x'yz+x'yz'+xy'z'+xy'z
ii. (x+y'+z')(x+y'+z)(x'+y+z)(x'+y+z') iii. x'z+x'y+xy'z+xyz iv. x'y'z+x'yz'+xy'z'+xy'z+xyz'
2. Draw the logic diagram corresponding to following expression without simplifying them i.(A+B)(C+D)(A'+B+D) ii.(AB+A'B')(CD'+C'D.
3. Express the following functions in sum of min terms and product of max terms
i. F(A,B,C,D)=B'D+A'D+BD ii.F(x,y,z)=(xy+z)(xz+y)
4.Obtain the simplified expression of SOP form using k-map method. i.F(A,B,C,D,E)=∑(0,1,4,5,16,17,21,25,29) ii. F(w,x,y,z)=∑(0,2,5,9,15)+∑d(6,7,8,10,12,13)

UNIT-III : DIGITAL LOGIC CIRCUITS-II
LEARNING OBJECTIVES:

LECTURE PLAN:
Total No_ of Classes: 07

S.No	Name of the Topic	Text/Reference book code	No. of classes required
13	Registers	T2	1
14	Shift registers	T2	1
15	Binary counters	T2	1
16	Decoders, multiplexers	T2	1
17	Programmable logic devices	T2	1

OBJECTIVE QUESTIONS :

1. The AND-NOR circuit can be equal to the following circuit **Ans: NAND-AND**
2. An AND-OR implementation requires an expression in the form of **Ans:-Sum of products**
3. An OR-AND-INVERT implementation requires an expression in the form of **Ans:- Product of sums**
4. The multiple variable exclusive -OR operation is defined as **Ans:-an odd function**
5. Which of the following gate can perform the Boolean function xy'+x'y **Ans:-XOR**
6. The complement of exclusive-OR gate is **Ans:-exclusive-NOR**
7. The NAND gate is also called as a **Ans:- AND-Invert**
8. The NOR gate is also called as a **Ans:-OR Invert**
9. The following is the adjacent cell for the cell 15 in five variable K -map **Ans:-31**
10. The sum of two min terms in adjacent squares of three variable map can be simplified to a **Ans: Single AND gate**
11. A combinational circuit has a logic gates with **Ans:-no feed back paths**
12. Every combinational circuit corresponds a Boolean function which describes the circuit **Ans:- logical behavior**
13. The over flow occurs when the addition is perform , this problem = in digital computers takes care by using a **Ans:-flip-flop**

DESCRIPTIVE QUESTIONS :

1. Design 3to8 line decoder mention its truth table
2. Implement the following using PLA & PAL
$F_1(A,B,C,D)=\sum m(0,1,2,3,6,9,11)$ $F_2(A,B,C,D)=\sum m(0,1,6,8,9)$

ASSIGNMENT QUESTIONS:

1. Give the circuit diagram for 4-bit register with parallel load
2. Design 3to8 line decoder mention its truth table
3. Implement the following using PLA & PAL
$F_1(A,B,C,D)=\sum m(0,1,2,3,6,9,11)$ $F_2(A,B,C,D)=\sum m(0,1,6,8,9)$
4. Design PLA architecture for 4inputs and 5 outputs.
5. Implement the following using PAL
$w(a,b,c,d)=\sum m(0,2,6,7,8,9,12,13)$
$x(a,b,c,d)=\sum m(0,2,6,7,8,9,12,13,14)$
$y(a,b,c,d)=\sum m(2,3,8,9,10,12,13)$ $z(a,b,c,d)=\sum m(1,3,4,9,12,14)$

UNIT-IV : COMPUTER ARITHMETIC

- **LEARNING OBJECTIVES:**

LECTURE PLAN:
Total No_ of Classes: 10

S.No	Name of the Topic	Text/Reference book code	No. of classes required
18	Algorithms for fixed pt and floating pt. addition	T2	2
19	Subtraction, multiplication, division operations	T2	1
20	Hardware implementation of arithmetic and logic operations	T2	1
21	High performance	T2	1

OBJECTIVE QUESTIONS :

1. The basic arithmetic operation in digital computers is = Ans:-addition
2. In the binary multiplier the successive partial products are Ans:-shifted one position to the left
3. BCD adder consists of **Ans:-two binary adders and logic circuit = with AND and OR gates**
4. In the Binary Multiplier the final product is obtained from the **Ans:-sum of the partial products**
5. To construct a Binary Multiplier with J multiplier bits and K multiplicand bits the following are required **Ans:-(J x K) AND gates and (J-1) K- bit adders**
6. The full adder can be implemented using **Ans:-two half adders**
7. A combinational circuit that performs the addition of three bits = is called a **Ans:-full adder**
8. A digital computer with more than one processor is called as **Ans**: **Multiprocessor System**
9. In a computer system control information is transferred in **Ans : control bus only**
10. The part of the hardware of computer that is used to manipulate data is **Ans: CPU**
11. Signed 1's complement representation of -14 with eight bits is **Ans**:**1110001**
12. The 1' s complement of decimal number 21 in binary is **Ans: 01010**
13. The two parts in floating-point representation are **Ans**: **mantissa , exponent**
14. A normalized floating-point binary number is **Ans: 1.010**
15. In floating point representation, the fixed point mantissa **Ans: may be fraction or integer**

DESCRIPTIVE QUESTIONS :

1. Explain booth's algorithm Algorithm with an example multiplicand 10111, multiplier 10011
2. High- performance multiplication.
3. Hard ware implementation of addition and subtraction

ASSIGNMENT QUESTIONS:

1. Explain booth's algorithm Algorithm with an example multiplicand 10111, multiplier 10011
2. High- performance multiplication, division, addition and subtraction
3. Hard ware implementation of addition and subtraction, division and multiplication

4. Give flow chart of arithmetic operations for floating point numbers

UNIT-V: INSTRUCTION SET AND ADDRESSING

- **LEARNING OBJECTIVES:**

LECTURE PLAN:
Total No_ of Classes: 7

S.No	Name of the Topic	Text/Reference book code	No. of classes required
22	Memory locations and addresses machine addresses and sequencing	T2	1
23	Various addressing modes	T2	1
24	Instruction formats	T2	2
25	Basic machine instructions	T2	2
26	IA-32 Pentium example	T2	2
27	addresses	T2	2

OBJECTIVE QUESTIONS :

1. Register transfer denoting memory write operation is **M {[AR]}←DR**
2. The operation executed on data stored in registers is called **micro operation**
3. The symbolic notation used to describe the micro operation transfers among registers is called **Register Transfer language**
4. The arithmetic micro operation R3←R1+ +1 denotes **Subtraction of R2 from R1**
5. The arithmetic micro operation R2← +1 denotes **2's complement of R2**
6. The arithmetic micro operation denotes **The sum of R1 and R2 is transferred to R3**
7. The arithmetic micro operation denoting decrementing the content of R1 by one is **R1←R1-1**
8. The category of micro operation used for serial transfer of data is **Shift micro operation**

DESCRIPTIVE QUESTIONS :

1. Explain various addressing modes of computer with example
2. Explain about shift operation and rotate operation

ASSIGNMENT QUESTIONS:

1. Explain various addressing modes of computer with example
2. Explain about shift operation and rotate operation
3. What are IA-32 processors? Give the register structure of IA-32 Pentium processor

UNIT-VI: PROCESSOR ORGANIZATION

- **LEARNING OBJECTIVES:**

LECTURE PLAN:
Total No_ of Classes: 07

S.No	Name of the Topic	Text/Reference book code	No. of Lecture classes required
28	Introduction to CPU, register transfers	R3	1
29	Execution of instructions	R3	1
30	Multiple bus organization	R3	1
31	Hardwired control	R3	1
32	Micro programmed control	R3	1

OBJECTIVE QUESTIONS :

1. In IAS computer address part specifies **Address of operand in memory**

2. The part of instruction code that specifies operation to be performed is **op code**

3. The computer register used to hold instruction code is **Instruction register**

4. computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. Draw the instruction word format and indicate the number of bits in each. **indirect 1bit, Op code 5bits, Register 8bits, Address 18 bits**

5. The instruction that clears start stop flip flop and stops sequence counter from counting is **HLT**

6. In the instruction cycle the phase that reads instruction into instruction register from memory is **Fetch**

7. The instruction that increments accumulator is **INC**

DESCRIPTIVE QUESTIONS :

1. Explain the process of fetching a word from memory along with its timing diagram. Also discuss about writing a word to memory.

2. Distinguish between micro programmed control and hard wired control.

ASSIGNMENT QUESTIONS:

1. Explain the process of fetching a word from memory along with its timing diagram. Also discuss about writing a word to memory.

2. Distinguish between micro programmed control and hard wired control.

3. Explain with an example the steps required for executing an instruction

4. Explain micro instruction sequencing with next-address field

UNIT-VII: MEMORY ORGANIZATION

- **LEARNING OBJECTIVES**

LECTURE PLAN: Basic Design Using a RTOS:

Total No_ of Classes: 10

S.No	Name of the Topic	Text/Reference book code	No. of classes required
37	Concepts of memories RAM, ROM memories	R3	1
38	Memory hierarchy	R3	1

39	Cache memories	R3	1
40	Virtual memory	R3	1
41	Secondary storage	R3	1
42	Memory management requirements	R3	1
43	Memory hierarchy	R3	1
44	Virtual memory	R3	1
45	Memory management	R3	1

OBJECTIVE QUESTIONS :

1. The memory reference instruction that denotes operation PC ←AR is **BUN**
2. ROM stands for **Read Only Memory**
3. PROM stands for **programmable read only memory**
4. RAM is volatile
5. ROM is non volatile and is permanent storage
6. DMA stands for **Direct Memory Access**
7. Data stored in cache memory in the form of blocks which are addressable known as **cache line**
8. Direct mapping process is **fast**

DESCRIPTIVE QUESTIONS :

1. Compare and contrast asynchronous DRAM and synchronous DRAM
2. Explain the organization of a 1k×1 memory with a neat sketch
3. Explain the applications of ROM, PROM, EPROM, EEPROM

ASSIGNMENT QUESTIONS:

1. Compare and contrast asynchronous DRAM and synchronous DRAM
2. Explain the organization of a 1k×1 memory with a neat sketch
3. Explain the applications of ROM, PROM, EPROM, EEPROM
4. What are the different types of mapping techniques used in the usage of cache memory. explain

UNITVIII: I/O ORGANIZATION

- **LEARNING OBJECTIVES:**

LECTURE PLAN:
Total No_ of Classes: 7

S.No	Name of the Topic	Text/Reference book code	No. of classes required
50	INTRODUCTION TO I/O	T1	1
51	Interrupts hardware	T1	2
52	Enabling and disabling interrupts	T1	1

53	Device control	T1	1
54	Direct memory access	T1	1
55	Interface circuits	T1	1
56	Standard I/O interfaces	T1	1

OBJECTIVE QUESTIONS :

1. Most computers based on RISC architecture **use hardwired control unit**

2. The program that translates symbolic micro program into its binary equivalent is **Assembler**

3. Arrange the following with the increasing speed of execution **Vertical microinstruction, horizontal microinstruction, hardwired implementation**

4. Arrange the following with the increasing logic of circuitry **Horizontal microinstruction, vertical microinstruction, hardwired implementation**

5. USB stands for **universal serial bus**

6. The process of selecting the next device that can become the bus master i.e., it can have the control of the bus is called **bus arbitration**

7. programmed I/O and Interrupt driven I/O are **types of communication techniques**

DESCRIPTIVE QUESTIONS :

1. Write short notes on DMA controller

2. Explain different types of I/O commands

ASSIGNMENT QUESTIONS:

1. Write short notes on DMA controller

2. Explain different types of I/O commands

3. What are the different kinds of DMA transfers and mention its advantages

DEPARTMENT OF INFORMATION TECHNOLOGY

INDIVIDUAL TIME TABLE

NAME OF THE FACULTY*:* V.SWAPNA

Period	1	2	3	4		5	6	7
Day/Time	9.00-9.50	9.50-10.40	10.40-11.30	11.30-12.20	L U N C H	12.50-1.40	1.40-2.30	2.30-3.20
Mon								
Tue								
Wed								
Thu								
Fri								
Sat								

COMPUTER ORG. & DLD

Total no of theory classes :

Total no of practical classes :

Total no of classes :

J. B.Institue of Engineering & Techology
II B.Tech -2009-Batch/I SEM (I-MID DESCRIPTIVE)
BRANCH: INFORMATION TECHNOLOGY
SUB: CO AND DLD

TIME: 60 MINUTES **Marks: 10**

SECTION-A & B

Answer any TWO of the following: **(2x5=10M)**

1. xxxxxxxxxxxxxxx
a) xxxxxxxxxxxx
b) xxxxxxxxxxx
c) xxxxxxxxxxxxxxxxxx

2. xxxxxxxxxxxxxxxxxx
   a) xxxxxxxxxxxxxxxx
   b) xxxxxxxxxxxxxxx
   c) xxxxxxxxxxxxxx

3. xxxxxxxxxxxxxxxxxxx?

4. xxxxxxxxxxxxxxxs? xxxxx?

Marks for Internal Theory Examination

ROLL.NO	NAME OF THE STUDENT	I MID (Des+Obj+Assign))	II MID Des+Obj+Assign))