J.B. INSTITUTE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)

ACADEMIC YEAR **2013-14**

http://www.jbiet.edu.in

	COURSE PLAN	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE

COURSE DETAILS

Name Of The Programme::	B.Tech	Batch::	2012-16
Designation::			
Year II		Semester II	
Department::	CSE		
Title of The Subject	Computer Organization	Subject Code	6754012
No of Students	113		

	COURSE PLAN	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE

1. TARGET

a) Percentage Pass 100%

b) Percentage I class 95%

2. COURSE PLAN

(Please write how you intend to cover the contents: i.e., coverage of Units by lectures, guest lectures, design exercises, solving numerical problems, demonstration of models, model preparation, or by assignments, etc.)

3. METHOD OF EVALUATION

3.1. ☐ Continuous Assessment Examinations (CAE 1, CAE 2)

3.2. ☐ Assignments / Seminars

3.3. ☐ Mini Projects

3.4. ☐ Quiz

3.5. ☐ Term End Examination

3.6. ☐ Others

4. List out any new topic(s) or any innovation you would like to introduce in teaching the subject in this Semester.
In this semester I would like to introduce advanced topic to motivate students in designing machine instruction:
(i) Instruction-Level Parallelism
(ii) Thread-Level Parallelism used in multiprocessors.

Signature of HOD
Date:

Signature of Faculty
Date:

	GUIDELINES TO STUDY THE SUBJECT	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty::	Abhay Kumar
Designation:	Associate Professpr
Department::	CSE
Guidelines for Preparing the Course:	

Course Description:
Basic understanding of computer organization: roles of processors, main memory, and input/output devices. Understanding the concept of programs as sequences of machine instructions. Understanding arithmetic and logical operations with integer operands. Understanding floating-point number systems and operations. Understanding simple data path and control designs for processors. Understanding memory organization, including cache structures and virtual memory schemes. Course include ALU, control and memory design and organization, pipelining and vector processing, computer arithmetic, I/O organization.

Course Objectives: (CO)
1. To have a thorough understanding of the basic structure and operation of a digital computer. 2. Perform the basic operations with signed and unsigned integers in decimal and binary number systems. 3. Explain the regular operation of a computer in terms of the fetch-decode-execute-write cycle and the interaction between the instruction set architecture and the computer organization. 4. To have knowledge about different addressing modes. 5. To have understanding of the design of control unit using either hardwired control method or micro programmed control method. 6. To discuss in detail the operation of the arithmetic unit including the algorithms & implementation of fixed-point and floating-point addition, subtraction, multiplication & division. 7. To study the hierarchical memory system including cache memories and virtual memory. 8. To study the different ways of communicating with I/O devices and standard I/O interfaces. 9. To study the design of pipeline and vector processing system. 10. To understand the design of multiprocessor system.

Learning Outcomes: (LO)
1. Learn the basic structure of a digital computer. 2. Understand the arithmetic and logical operations of binary number system. 3. Understand the design of the Control unit. 4. Have knowledge about the organization of Arithmetic and Logical unit and I/O unit. 5. Understand the design of Memory unit.

	COURSE OBJECTIVES	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE

On completion of this Subject / Course the student shall be able to:

S.No.	Objectives (CO)	Outcomes (LO)
1.	To have a thorough understanding of the basic structure and operation of a digital computer.	1
2.	Perform basic operations with signed and unsigned integers in decimal and binary number systems.	1,2
3.	Explain the regular operation of a computer in terms of the fetch-decode-execute-write cycle and the interaction between the instruction set architecture and the computer organization.	1,4
4.	To have knowledge about different addressing modes.	1,5
5.	To have understanding of the design of control unit using either hardwired control method or micro programmed control method.	3
6.	To discuss in detail the operation of the arithmetic unit including the algorithms & implementation of fixed-point and floating-point addition, subtraction, multiplication & division.	2,4
7.	To study the hierarchical memory system including cache memories and virtual memory.	5
8.	To study the different ways of communicating with I/O devices and standard I/O interfaces.	4
9.	To study the design of pipeline and vector processing system.	4
10.	To understand the design of multiprocessor system.	4,5

Signature of Faculty
Date:

Note: For each of the OBJECTIVE indicate the appropriate OUTCOMES to be achieved.
Kindly refer Page 16, to know the illustrative verbs that can be used to state the objectives.

	COURSE OUTCOMES	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE

The expected outcomes of the Course / Subject are:

S.No.	General Categories of Outcomes	Specific Outcomes of the Course
A.	An ability to apply knowledge of mathematics, science, and engineering	Students were able to design mathematical model of binary adder and subtraction circuit independently
B.	An ability to design and conduct experiments, as well as to analyze and interpret data	
C.	An ability to design a system, component, or process to meet desired needs within realistic Constraints such as economic, environmental, social, political, ethical, health and safety, Manufacturability and sustainability	Students were able to analyze and interpret date, design flowchart of 4-bit binary adder circuit
D.	An ability to function on multi-disciplinary teams	
E.	An ability to identify, formulate, and solve engineering problems	
F.	An understanding of professional and ethical responsibility	
G.	An ability to communicate effectively	
H.	The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context	
I.	A recognition of the need for, and an ability to engage in life-long learning	
J.	A knowledge of contemporary issues	
K.	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.	

Objectives – Outcome Relationship Matrix (Indicate the relationships by ☒ mark).

Objectives \ Outcomes	A	B	C	D	E	F	G	H	I	J	K
1.	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
2.	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
3.	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
4.	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
5.	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
6.	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
7.	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
8.	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
9.	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
10.	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐

	COURSE SCHEDULE	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE
The Schedule for the whole Course / Subject is:: Computer Organization

S. No.	Description	Duration (Date)		Total No. of Periods
		From	To	
1.	BASIC STRUCTURE OF COMPUTERS	09-12-2013	21-12-2013	10
2.	REGISTER TRANSFER LANGUAGE AND MICROOPERATIONS AND MEMORY	23-12-2013	11-01-2014	15
3.	MICRO PROGRAMMED CONTROL	13-01-2014	25-01-2014	10
4.	COMPUTER ARITHMETIC	27-01-2014	08-02-2014	10
5.	THE MEMORY SYSTEM	10-02-2014	22-02-2014	10
6.	INPUT-OUTPUT ORGANIZATION	24-02-2014	08-03-2014	10
7	PIPELINE AND VECTOR PROCESSING	10-03-2014	22-03-2014	10
8	MULTI PROCESSORS	24-03-2014	05-04-2014	10

Total No. of Instructional periods available for the course: 85 Periods (50 minutes per period)

Text Books:

TB1- Computer Systems Architecture, M.Moris Mano, IIIrd Edition, Pearson/PHI

TB2- Computer Organization,Carl Hamacher, Zvonks Vranesic, SafeaZaky, Vth Edition, McGraw Hill.

TB3- Computer Organization and Architecture, William Stallings Sixth Edition, Pearson/PHI

TB4- Structured Computer Organization, Andrew S. Tanenbaum, 4th Edition PHI/Pearson

	SCHEDULE OF INSTRUCTIONS UNIT - I	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE
The Schedule for the whole Course / Subject is:: Computer Organization

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives(CO) & Outcome(LO) Nos.	References (Text Book, Journal…) Page No___ to ___
1	09-12-2013	1	Computer Types	CO1, LO1	TB2 Page No 2 to 3
2	10-12-2013	2	Functional unit	CO1, LO1	TB2 Page No 3 to 7
3	11-12-2013	3	Basic OPERATIONAL concepts	CO1, LO1	TB1 Page No 7 to 9
4	12-12-2013	4	Bus structures	CO1, LO1	TB2 Page No 9 to 10
5	14-12-2013	5	Software, Performance	CO1, LO1	TB2 Page No 13 to 18
6	16-12-2013	6	Multiprocessors and multi computers	CO10, LO3	TB2 Page No 18 to 19
7	17-12-2013	7	Data Representation	CO2, LO2	TB1 Page No 67 to 77
8	18-12-2013	8	Fixed Point Representation	CO2, LO2	TB1 Page No 77 to 82
9	19-12-2013	9	Floating – Point Representation	CO2, LO2	TB1 Page No 83 to 84
10	21-12-2013	10	Error Detection codes	CO2, LO2	TB1 Page No 87 to 89

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

	SCHEDULE OF INSTRUCTIONS UNIT - II	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE
The Schedule for the whole Course / Subject is:: Computer Organization

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives(CO) & Outcome(LO) Nos.	References (Text Book, Journal…) Page No___ to ___
1	23-12-2013	1	Register Transfer language	CO1 CO3 LO1 LO2	TB1 Page No 93 to 94
2	24-12-2013	2	Register Transfer, Bus and memory transfers	CO1 CO3 LO1 LO2	TB1 Page No 95 to 102
3	25-12-2013	3	Arithmetic Mircrooperatiaons, logic micro operations	CO1 CO3 LO1 LO2	TB1 Page No 102 to 113
4	26-12-2013	4	Shift micro operations, Arithmetic logic shift unit	CO1 CO3 LO1 LO2	TB1 Page No 114 to 118
5	28-12-2013	5	Instruction codes, Computer Registers	CO1 CO3 LO1 LO2	TB1 Page No 125 to 134
6	30-12-2013	6	Computer instructions	CO1 CO3 LO1 LO2	TB1 Page No 134to 137
7	31-12-2013	7	Instruction cycle	CO1 CO3 LO1 LO2	TB1 Page No 93 to 94
8	01-01-2014	8	Memory reference Instructions	CO1 CO3 LO1 LO2	TB1 Page No 141 to 146
9	02-01-2014	9	Input – Output Interrupt	CO1 CO8 LO1 LO2	TB1 Page No 152 to 158
10	04-01-2014	10	STACK organization	CO1 CO3 LO1 LO2	TB1 Page No 249 to 257
11	06-01-2014	11	Instruction formats	CO1 CO3 LO1 LO2	TB1 Page No 257 to 262
12	07-01-2014	12	Addressing modes	CO1 CO4 LO1 LO2	TB1 Page No 262 to 268
13	08-01-2014	13	DATA Transfer and manipulation	CO1 CO3 LO1 LO2	TB1 Page No 268 to 274

14	09-01-2014	14	Program control	CO1 CO3 LO1 LO2	TB1 Page No 275 to 284
15	11-01-2014	15	Reduced Instruction set computer	CO1 CO3 LO1 LO2	TB1 Page No 284 to 293

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

	SCHEDULE OF INSTRUCTIONS UNIT - III	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE
The Schedule for the whole Course / Subject is:: Computer Organization

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives(CO) & Outcome(LO) Nos.	References (Text Book, Journal…) Page No___ to ___
1	13-01-2014	1	Control memory	CO5 LO3	TB1 Page No 215 to 217
2	14-01-2014	2	Control memory	CO5 LO3	TB1 Page No 217 to 218
3	15-01-2014	3	Address sequencing	CO5 LO3	TB1 Page No 218 to 220
4	16-01-2014	4	Address sequencing	CO5 LO3	TB1 Page No 220 to 222
5	18-01-2014	5	Microprogram example	CO5 LO3	TB1 Page No 222 to 228
6	20-01-2014	6	Microprogram example	CO5 LO3	TB1 Page No 228 to 233
7	21-01-2014	7	Design of control unit	CO5 LO3	TB1 Page No 233 to 237
8	22-01-2014	8	Hard wired control	CO5 LO3	TB2 Page No 425 to 429
9	23-01-2014	9	Microprogrammed control	CO5 LO3	TB2 Page No 429 to 440
10	25-01-2014	10	Microprogrammed control with example	CO5 LO3	TB2 Page No 440 to 445

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC

	SCHEDULE OF INSTRUCTIONS UNIT - IV	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE
The Schedule for the whole Course / Subject is:: Computer Organization

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos.	References (Text Book, Journal…) Page No___ to ___
1	27-01-2014	1	Addition and subtraction	CO6 LO4	TB1 Page No 336 to 340
2	28-01-2014	2	Addition and subtraction	CO6 LO4	TB1 Page No 340 to 342
3	29-01-2014	3	Multiplication Algorithms	CO6 LO4	TB1 Page No 342 to 350
4	30-01-2014	4	Division Algorithms	CO6 LO4	TB1 Page No 350 to 356
5	01-02-2014	5	Floating – point Arithmetic operations	CO6 LO4	TB1 Page No 356 to 360
6	03-02-2014	6	Floating – point Arithmetic operations	CO6 LO4	TB1 Page No 360 to 365
7	04-02-2014	7	Decimal Arithmetic unit	CO6 LO4	TB1 Page No 365 to 368
8	05-02-2014	8	Decimal Arithmetic unit	CO6 LO4	TB1 Page No 369 to 371
9	06-02-2014	9	Decimal Arithmetic operations	CO6 LO4	TB1 Page No 371 to 374
10	08-02-2014	10	Decimal Arithmetic operations	CO6 LO4	TB1 Page No 375 to 378

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC

	SCHEDULE OF INSTRUCTIONS UNIT - V	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE
The Schedule for the whole Course / Subject is:: Computer Organization

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos.	References (Text Book, Journal…) Page No___ to ___
1	10-02-2014	1	Memory systems - Basic concepts	CO7 LO5	TB2 Page No 292 to 295
2	11-02-2014	2	Semiconductor RAM memories	CO7 LO5	TB2 Page No 295 to 300
3	12-02-2014	3	Semiconductor RAM memories	CO7 LO5	TB2 Page No 301 to 309
4	13-02-2014	4	Read-only memories	CO7 LO5	TB2 Page No 309 to 313
5	15-02-2014	5	Cache memories	CO7 LO5	TB2 Page No 314 to 320
6	17-02-2014	6	Cache memories	CO7 LO5	TB2 Page No 321 to 329
7	18-02-2014	7	Performance considerations	CO7 LO5	TB2 Page No 329 to 337
8	19-02-2014	8	Virtual memories	CO7 LO5	TB2 Page No 337 to 343
9	20-02-2014	9	Secondary storage	CO7 LO5	TB2 Page No 344 to 359
10	22-02-2014	10	Introduction to RAID	CO7 LO5	TB2 Page No 351 to 352

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC

	SCHEDULE OF INSTRUCTIONS UNIT - VI	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE
The Schedule for the whole Course / Subject is:: Computer Organization

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos.	References (Text Book, Journal…) Page No___ to ___
1	24-02-2014	1	Peripheral Devices	CO8 LO4	TB1 Page No 383 to 387
2	25-02-2014	2	Input-Output Interface	CO8 LO4	TB1 Page No 387 to 393
3	26-02-2014	3	Asynchronous data transfer	CO8 LO4	TB1 Page No 393 to 404
4	27-02-2014	4	Modes of Transfer	CO8 LO4	TB1 Page No 404 to 409
5	01-03-2014	5	Priority Interrupt	CO8 LO4	TB1 Page No 409 to 417
6	03-03-2014	6	Direct memory Access,	CO8 LO4	TB1 Page No 417 to 422
7	04-03-2014	7	Input –Output Processor (IOP)	CO8 LO4	TB1 Page No 422 to 431
8	05-03-2014	8	Serial communication, Introduction to peripheral component interconnect (PCI) bus	CO8 LO4	TB2 Page No 261 to 272
9	06-03-2014	9	Introduction to standard serial communication protocols like RS232	CO8 LO4	TB2 Page No 571 to 571
10	08-03-2014	10	Introduction to standard serial communication protocols like USB, IEEE1394	CO8 LO4	TB2 Page No 272 to 282

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC

	SCHEDULE OF INSTRUCTIONS UNIT - VII	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE
The Schedule for the whole Course / Subject is:: Computer Organization

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos.	References (Text Book, Journal…) Page No___ to ___
1	10-03-2014	1	Parallel Processing	CO9 LO4	TB1 Page No 301 to 304
2	11-03-2014	2	Pipelining	CO9 LO4	TB1 Page No 304 to 306
3	12-03-2014	3	Pipelining	CO9 LO4	TB1 Page No 307 to 309
4	13-03-2014	4	Arithmetic Pipeline	CO9 LO4	TB1 Page No 309 to 311
5	15-03-2014	5	Arithmetic Pipeline	CO9 LO4	TB1 Page No 311 to 312
6	17-03-2014	6	Instruction Pipeline	CO9 LO4	TB1 Page No 312 to 315
7	18-03-2014	7	Instruction Pipeline	CO9 LO4	TB1 Page No 315 to 317
8	19-03-2014	8	RISC Pipeline	CO9 LO4	TB1 Page No 317 to 321
9	20-03-2014	9	Vector Processing	CO9 LO4	TB1 Page No 312 to 329
10	22-03-2014	10	Array Processors	CO9 LO4	TB1 Page No 329 to 331

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC

	SCHEDULE OF INSTRUCTIONS UNIT - VIII	2013-14 Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE
The Schedule for the whole Course / Subject is:: Computer Organization

Sl. No.	Date	No. of Periods	Topics / Sub - Topics	Objectives & Outcome Nos.	References (Text Book, Journal…) Page No___ to ___
1	24-03-2014	1	Characteristics of Multiprocessors	CO10 LO5	TB1 Page No 491 to 492
2	25-03-2014	2	Difference between multiprocessors and multicomputer	CO10 LO5	TB1 Page No 492 to 493
3	26-03-2014	3	Interconnection Structures	CO10 LO5	TB1 Page No 493 to 497
4	27-03-2014	4	Interconnection Structures	CO10 LO5	TB1 Page No 498 to 502
5	29-03-2014	5	Interprocessor Arbitration	CO10 LO5	TB1 Page No 502 to 505
6	31-03-2014	6	Interprocessor Arbitration	CO10 LO5	TB1 Page No 505 to 507
7	01-04-2014	7	InterProcessor Communication and Synchronization	CO10 LO5	TB1 Page No 507 to 509
8	02-04-2014	8	InterProcessor Communication and Synchronization	CO10 LO5	TB1 Page No 509 to 511
9	03-04-2014	9	Cache Coherance	CO10 LO5	TB2 Page No 641 to 645
10	05-04-2014	10	Shared Memory Multiprocessors	CO10 LO5	TB2 Page No 637 to 638

Signature of Faculty
Date

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED **BOLDLY**.
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC

	COURSE COMPLETION STATUS	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar

Subject:: Computer Organization Subject Code 6754012

Department:: CSE

Actual Date of Completion & Remarks, if any

Units	Remarks	Nos. of Objectives Achieved
Unit 1	21-12-2013	2
Unit 2	11-01-2014	3
Unit 3	25-01-2014	1
Unit 4	08-02-2014	1
Unit 5	22-02-2014	1
Unit 6	08-03-2014	1
Unit 7	22-03-2014	1
Unit 8	05-04-2014	1

Signature of Dean of School
Date:

Signature of Faculty
Date:

NOTE: AFTER THE COMPLETION OF EACH UNIT MENTION THE NUMBER OF OBJECTIVES ACHIEVED.

	TUTORIAL SHEETS - I	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE
The Schedule for the whole Course / Subject is:: Computer Organization

Date: 21-12-2013

This Tutorial corresponds to Unit Nos. I, II, III and IV

Time:1pm

Q1. Explain in detail the basic functional units of a computer [1].

Q2. Draw a block diagram of a 4-bit arithmetic circuit and briefly explain it [6].

Q3. Using a simple example draw the block diagram for the design of control unit [5].

Q4. Explain addition and subtraction with signed-magnitude data [2].

Q5. Explain Instruction cycle and draw the flowchart for instruction cycle using an example [3].

Q6. Briefly explain all the addressing modes using examples [4].

Q7. Briefly explain stack organization with an example [4].

Q8. Explain hardware implementation for multiplication algorithm [6].

Q9. Explain how to generate control signals using hardwired control method [5].

Q10. Explain three methods of representing signed numbers using examples [2].

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the objectives to which these questions / Problems are related.

Signature of Dean of School
Date:

Signature of Faculty
Date:

	TUTORIAL SHEETS - II	2013-14
		Regulation: R11

FACULTY DETAILS:

Name of the Faculty:: Abhay Kumar
Designation: Associate Professor
Department:: CSE
The Schedule for the whole Course / Subject is:: Computer Organization

Date: 08-02-2014

This Tutorial corresponds to Unit Nos. V, VI, VII and VIII

Time:1pm

Q1. Briefly explain different types of semiconductor RAM memories [7].

Q2. Explain DMA in detail using block diagram [8].

Q3. Explain instruction pipeline using four-segment example [9].

Q4. Briefly explain any three schemes of interconnection structures of a multiprocessor system [10].

Q5. Explain cache memory. Briefly explain different type of mapping functions associated with cache memory [7].

Q6. Explain three different ways of modes of transfer [8].

Q7. Explain RISC pipeline using three-segment example [9].

Q8. Briefly explain inter-processor arbitration [10].

Q9. Explain virtual memory and address translation method [7].

Q10. Briefly explain inter-processor communication and synchronization [10].

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the objectives to which these questions / Problems are related.

Signature of Dean of School
Date:

Signature of Faculty
Date:

	ILLUSTRATIVE VERBS FOR STATING INSTRUCTIONAL OBJECTIVES	2013-14
		Regulation: R11

These verbs can also be used while framing questions for Continuous Assessment Examinations as well as for End – Semester (final) Examinations.

ILLUSTRATIVE VERBS FOR STATING **GENERAL OBJECTIVES**

Know Comprehend	Understand Apply	Analyze Design	Generate Evaluate

ILLUSTRATIVE VERBS FOR STATING **SPECIFIC OBJECTIVES:**

A. Cognitive Domain

1	2	3	4	5	6
Knowledge	**Comprehension Understanding**	**Application** of knowledge & comprehension	**Analysis** of whole w.r.t. its constituents	**Synthesis** combination of ideas/constituents	**Evaluation** judgement
Define	Convert	Change	Breakdown	Categorize	Appraise
Identify	Defend	Compute	Differentiate	Combine	Compare
Label	Describe (a	Demonstrate	Discriminate	Compile	Conclude
List	procedure)	Deduce	Distinguish	Compose	Contrast
Match	Distinguish	Manipulate	Separate	Create	Criticize
Reproduce	Estimate	Modify	Subdivide	Devise	Justify
Select	Explain why/how	Predict		Design	Interpret
State	Extend	Prepare		Generate	Support
	Generalize	Relate		Organize	
	Give examples	Show		Plan	
	Illustrate	Solve		Rearrange	
	Infer			Reconstruct	
	Summarize			Reorganize	
				Revise	

B. Affective Domain		**C. Psychomotor Domain (skill development)**				
Adhere	Resolve	Bend	Dissect	Insert	Perform	Straighten
Assist	Select	Calibrate	Draw	Keep	Prepare	Strengthen
Attend	Serve	Compress	Extend	Elongate	Remove	Time
Change	Share	Conduct	Feed	Limit	Replace	Transfer
Develop		Connect	File	Manipulate	Report	Type
Help		Convert	Grow	Move preciselyReset		Weigh
Influence		Decrease	Handle	Operate	Run	
Initiate		Demonstrate	Increase	Paint	Set	

	LESSON PLAN Unit-1	2013-14
		Regulation: R11

Name of the Faculty: Abhay Kumar

Subject Computer Organization Subject Code 6754012

Unit I

INSTRUCTIONAL OBJECTIVES:

1. To have a thorough understanding of the basic structure and operation of a digital computer.
2. Perform basic operations with signed and unsigned integers in decimal and binary number systems.

Session No	Topics to be covered	Time (Min)	Ref	Teaching Method
1	Computer Types	50	TB2	Chalkboard
2	Functional unit	50	TB2	Chalkboard
3	Basic OPERATIONAL concepts	50	TB1	Chalkboard
4	Bus structures	50	TB2	Chalkboard
5	Software, Performance	50	TB2	Chalkboard
6	Multiprocessors and multi computers	50	TB2	PPT
7	Data Representation	50	TB1	Chalkboard
8	Fixed Point Representation	50	TB1	Chalkboard
9	Floating – Point Representation	50	TB1	Chalkboard
10	Error Detection codes	50	TB1	PPT

On completion of this lesson the student shall be able to (Outcomes)

1. Learn the basic structure of a digital computer.

	ASSIGNMENT **Unit-I**	2013-14
		Regulation: R11

Assignment / Questions

Analyze the functional units of a digital computer system.

Course Objectives: To have a thorough understanding of the basic structure and operation of a digital computer.

Learning Outcomes: Learn the basic structure of a digital computer

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

	LESSON PLAN Unit-II	2013-14
		Regulation: R11

Name of the Faculty: Abhay Kumar

Subject Computer Organization Subject Code 6754012

Unit II

INSTRUCTIONAL OBJECTIVES:

1. Explain the regular operation of a computer in terms of the fetch-decode-execute-write cycle and the interaction between the instruction set architecture and the computer organization.
2. To have knowledge about different addressing modes.

Session No	Topics to be covered	Time (Min)	Ref	Teaching Method
1	Register Transfer language	50	TB1	Chalkboard
2	Register Transfer Bus and memory transfers	50	TB1	Chalkboard
3	Arithmetic Mircrooperatiaons, logic micro operations	50	TB1	Chalkboard
4	Shift micro operations, Arithmetic logic shift unit	50	TB1	Chalkboard
5	Instruction codes, Computer Registers	50	TB1	Chalkboard
6	Computer instructions	50	TB1	Chalkboard
7	Instruction cycle	50	TB1	Chalkboard
8	Memory reference Instructions	50	TB1	Demonstration
9	Input – Output Interrupt	50	TB1	Chalkboard
10	STACK organization	50	TB1, TB3	PPT
11	Instruction formats	50	TB1	Chalkboard
12	Addressing modes	50	TB1	PPT
13	DATA Transfer and manipulation	50	TB1	Chalkboard
14	Program control	50	TB1	Chalkboard
15	Reduced Instruction set computer	50	TB1, TB4	Chalkboard

On completion of this lesson the student shall be able to (Outcome)

1. Understand the arithmetic and logical operations of binary number system.

	ASSIGNMENT **Unit-II**	2013-14
		Regulation: R11

Assignment / Questions

Why stack organization is used in the processors?
What do you understand by register stack and memory stack.

Course Objectives: Explain the regular operation of a computer in terms of the fetch-decode-execute-write cycle and the interaction between the instruction set architecture and the computer organization.

Learning Outcomes: Understand the arithmetic and logical operations of binary number system.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

	LESSON PLAN Unit-III	2013-14
		Regulation: R11

Name of the Faculty: Abhay Kumar

Subject Computer Organization Subject Code 6754012

Unit III

INSTRUCTIONAL OBJECTIVES: To have understanding of the design of control unit using either hardwired control method or micro programmed control method.

Session No	Topics to be covered	Time	Ref	Teaching Method
1	Control memory	50	TB1	Chalkboard
2	Control memory	50	TB1, TB3	Chalkboard
3	Address sequencing	50	TB1	Chalkboard
4	Address sequencing	50	TB1, TB4	Chalkboard
5	Microprogram example	50	TB1	PPT
6	Microprogram example	50	TB1	PPT
7	Design of control unit	50	TB1	Chalkboard
8	Hard wired control	50	TB2	Chalkboard
9	Microprogrammed control	50	TB2	PPT
10	Microprogrammed control with example	50	TB2	PPT

On completion of this lesson the student shall be able to (Outcomes)

2. Understand the design of the Control unit.

	ASSIGNMENT **Unit-III**	2013-14 Regulation: R11

Assignment / Questions

Hardwired control unit is faster than micro programmed control unit. Justify this statement?

Course Objectives: To have understanding of the design of control unit using either hardwired control method or micro programmed control method.

Learning Outcomes: Understand the design of the Control unit.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

	LESSON PLAN Unit-IV	2013-14
		Regulation: R11

Name of the Faculty: Abhay Kumar

Subject Computer Organization Subject Code 6754012

Unit IV

INSTRUCTIONAL OBJECTIVES: To discuss in detail the operation of the arithmetic unit including the algorithms & implementation of fixed-point and floating-point addition, subtraction, multiplication & division

Session No	Topics to be covered	Time	Ref	Teaching Method
1	Addition and subtraction	50	TB1	Chalkboard
2	Addition and subtraction	50	TB1	Chalkboard
3	Multiplication Algorithms	50	TB1	Chalkboard
4	Division Algorithms	50	TB1	Chalkboard
5	Floating – point Arithmetic operations	50	TB1	PPT
6	Floating – point Arithmetic operations	50	TB1	Chalkboard
7	Decimal Arithmetic unit	50	TB1	Chalkboard
8	Decimal Arithmetic unit	50	TB1	PPT
9	Decimal Arithmetic operations	50	TB1	Chalkboard
10	Decimal Arithmetic operations	50	TB1	PPT

On completion of this lesson the student shall be able to (Outcomes)

1. Have knowledge about the organization of Arithmetic and Logical unit

	ASSIGNMENT **Unit-IV**	2013-14
		Regulation: R11

Assignment / Questions

Using diagram explain hardware implementation for division algorithm.

Course Objectives: To discuss in detail the operation of the arithmetic unit including the algorithms & implementation of fixed-point and floating-point addition, subtraction, multiplication & division

Learning Outcomes: Have knowledge about the organization of Arithmetic and Logical unit.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

	LESSON PLAN Unit-V	2013-14
		Regulation: R11

Name of the Faculty: Abhay Kumar

Subject Computer Organization Subject Code 6754012

Unit V

INSTRUCTIONAL OBJECTIVES: To study the hierarchical memory system including cache memories and virtual memory.

Session No	Topics to be covered	Time	Ref	Teaching Method
1	Memory systems - Basic concepts	50	TB2	Chalkboard
2	Semiconductor RAM memories	50	TB2	PPT
3	Semiconductor RAM memories	50	TB2	Demonstration
4	Read-only memories	50	TB2	Chalkboard
5	Cache memories	50	TB2	PPT
6	Cache memories	50	TB2	PPT
7	Performance considerations	50	TB2	Chalkboard
8	Virtual memories	50	TB2	Chalkboard
9	Secondary storage	50	TB2	Demonstration
10	Introduction to RAID	50	TB2, TB3, TB4	Chalkboard

On completion of this lesson the student shall be able to (Outcomes)

1. Understand the design of Memory unit.

	ASSIGNMENT **Unit-V**	2013-14 Regulation: R11

Assignment / Questions

Analyze the performance improvement of using cache memory.

Course Objectives: To study the hierarchical memory system including cache memories and virtual memory.

Learning Outcomes: Understand the design of Memory unit.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

	LESSON PLAN Unit-VI	2013-14
		Regulation: R11

Name of the Faculty: Abhay Kumar

Subject Computer Organization Subject Code 6754012

Unit VI

INSTRUCTIONAL OBJECTIVES: To study the different ways of communicating with I/O devices and standard I/O interfaces.

Session No	Topics to be covered	Time	Ref	Teaching Method
1	Peripheral Devices	50	TB1	Demonstration
2	Input-Output Interface	50	TB1	Chalkboard
3	Asynchronous data transfer	50	TB1	Chalkboard
4	Modes of Transfer	50	TB1	Demonstration
5	Priority Interrupt	50	TB1	Chalkboard
6	Direct memory Access	50	TB1	Chalkboard
7	Input –Output Processor (IOP)	50	TB1, TB3	Chalkboard
8	Serial communication, Introduction to peripheral component interconnect (PCI) bus	50	TB2	PPT
9	Introduction to standard serial communication protocols like RS232	50	TB2	PPT
10	Introduction to standard serial communication protocols like USB, IEEE1394	50	TB2, TB4	PPT

On completion of this lesson the student shall be able to (Outcomes)

1. Have knowledge about the organization of Input/output unit

	ASSIGNMENT **Unit-VI**	2013-14
		Regulation: R11

Assignment / Questions

Justify the advantages of having DMA.

Course Objectives: To study the different ways of communicating with I/O devices and standard I/O interfaces.

Learning Outcomes: Have knowledge about the organization of Input/output unit.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

	LESSON PLAN Unit-VII	2013-14
		Regulation: R11

Name of the Faculty: Abhay Kumar

Subject Computer Organization Subject Code 6754012

Unit VII

INSTRUCTIONAL OBJECTIVES: To study the design of pipeline and vector processing system.

Session No	Topics to be covered	Time	Ref	Teaching Method
1	Parallel Processing	50	TB1	PPT
2	Pipelining	50	TB1	PPT
3	Pipelining	50	TB1, TB3	PPT
4	Arithmetic Pipeline	50	TB1	Chalkboard
5	Arithmetic Pipeline	50	TB1	Chalkboard
6	Instruction Pipeline	50	TB1	Chalkboard
7	Instruction Pipeline	50	TB1, TB4	Chalkboard
8	RISC Pipeline	50	TB1	Chalkboard
9	Vector Processing	50	TB1	PPT
10	Array Processors	50	TB1	PPT

On completion of this lesson the student shall be able to (Outcomes)

1. Have knowledge about the organization of Arithmetic and Logical unit.
2. Understand the design of the Control unit.

	ASSIGNMENT **Unit-VII**	2013-14
		Regulation: R11

Assignment / Questions

Using diagram design a RISC pipeline.

Course Objectives: To study the design of pipeline and vector processing system.

Learning Outcomes: Have knowledge about the organization of Arithmetic and Logical unit.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.

	LESSON PLAN **Unit-VIII**	2013-14 Regulation: R11

Name of the Faculty: Abhay Kumar

Subject Computer Organization Subject Code 6754012

Unit VIII

INSTRUCTIONAL OBJECTIVES: To understand the design of multiprocessor system.

Session No	Topics to be covered	Time	Ref	Teaching Method
1	Characteristics of Multiprocessors	50	TB1, TB3	Demonstration
2	Difference between multiprocessors and multicomputer	50	TB1	Demonstration
3	Interconnection Structures	50	TB1	PPT
4	Interconnection Structures	50	TB1	PPT
5	Interprocessor Arbitration	50	TB1	Chalkboard
6	Interprocessor Arbitration	50	TB1	Chalkboard
7	InterProcessor Communication and Synchronization	50	TB1	PPT
8	InterProcessor Communication and Synchronization	50	TB1	PPT
9	Cache Coherance	50	TB2, TB4	Chalkboard
10	Shared Memory Multiprocessors	50	TB2	Chalkboard

On completion of this lesson the student shall be able to (Outcomes)

1. Understand the design of Memory unit.

	ASSIGNMENT **Unit-VIII**	2013-14
		Regulation: R11

Assignment / Questions

Specify the difference between multiprocessor computer system and multicomputer based system.

Course Objectives: To understand the design of multiprocessor system.

Learning Outcomes: Understand the design of Memory unit.

Signature of Faculty

Note: Mention for each question the relevant objectives and outcomes.