J.B.INSTITUTE OF ENGINEERING & TECHNOLOGY
UGC AUTONOMOUS

M.Tech. (VLSI SYSTEM DESIGN)
COURSE STRUCTURE AND SYLLABUS-R18

I Year – I Semester

S.No	Course Code	Course Title	L	P	C
1	GM61A	Digital System Design using HDL	3	-	3
2	GM61B	Digital CMOS Integrated Circuit Design	3	-	3
3	GM61C GM61D GM61E	Device Modeling Digital System Design Scripting Languages for VLSI	3	-	3
4	GM61F GM61G GM61H	Micro Controllers for Embedded Systems CPLD and FPGA Architectures and Applications VLSI Technology and Design	3	-	3
5	GM61I	HDL simulation Lab	-	4	2
6	GM61J	Digital CMOS VLSI Design Lab	-	4	2
7	GM11K	Research Methodology and IPR	2	-	2
8		Audit course 1	2	-	-
		Total Credits	**16**	**8**	**18**

S.No	Course Code	Course Title	L	P	C
1	GM62A	Analog CMOS Design	3	-	3
2	GM62B	ASIC Design	3	-	3
3	GM62C GM62D GM62E	Low Power VLSI Design Design for Testability System On Chip Architecture	3	-	3
4	GM62F GM62G GM62H	Hardware Software Co-Design Optimization Techniques in VLSI Design Image and Video Processing	3	-	3
5	GM62I	Analog CMOS Design Lab	-	4	2
6	GM62J	ASIC Design Lab	-	4	2
7	GM62K	Mini Project	2	-	2
8		Audit course 2	2	-	-
	Total Credits		**16**	**8**	**18**

II Year – I Semester

S.No	Course Code	Course Title	L	P	C
1	GM63A GM63B GM63C	Advanced Computer Architecture CAD for VLSI CMOS Mixed Signal Circuit Design	3	-	3
2	GM6OA GM6OB	Digital Signal Processors and Architectures AD-HOC Wireless Networks	3	-	3
3	GM63D	Dissertation Phase – I	-	20	10
		Total Credits	**6**	**20**	**16**

II Year – II Semester

S.No	Course Code	Course Title	L	P	C
1	GM64A	Dissertation Phase – II	-	32	16
		Total Credits	**-**	**32**	**16**

Audit course 1 & 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills

JB INSTITUTE OF ENGINEERING & TECHNOLOGY (UGC Autonomous)
(Accredited by NAAC, Approved by AICTE & Permanently Affiliated to JNTUH)

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL SYSTEM DESIGN USING HDL

(Core I)

M.Tech (VLSISD) **I Year-I Semester**

Course Code: GM61A **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- Learn digital design of Sequential Machines.
- Learn drawing state graphs.
- Learn realization and implementation of SM Charts.
- Learn Fault modeling and test pattern generation of Combinational circuits.
- Learn fault diagnosis in sequential circuits and understand machine design, identification of fault detection experiment.

COURSE OUTCOMES: After going through the course students will be able to

- Create understanding of the design techniques of sequential Machines.
- Create understanding of the fundamental concepts of PLD's, design of FPGA's.
- Learn implementation of SM charts in combinational and sequential circuits.
- Develop skills in modeling fault free combinational circuits.
- Develop skills in modeling Sequential circuits in terms of reliability, availability and safety.

UNIT I

Digital System Design Automation and RTL Design with Verilog Degital Design Flow-design entry, Test bench in Verilog, Design validation

Compilation and synthesis, Post synthesis simulation, Timing analysis, Hardware generation in Verilog, Test Benches.

UNIT II

Verilog Language Concepts Characterizing Hardware Languages, Module Basics, Verilog Simulation Model,
Compiler Directives, System Tasks and Functions

UNIT III

Combinational Circuit Description Module Wires, Gate Level Logic, Hierarchical Structures, Describing Expressions with Assign statements, Behavioral Combinational Descriptions, Combinational Synthesis

UNIT IV

Sequential Circuit Description Sequential models, Basic Memory Components, Functional Registers, State Machine Coding, Sequential Synthesis. **Component Test, Verification and Detailed Modeling**
Test Bench, Test Bench Techniques, design Verification, Assertion Verification, Text Based Test Benches, Detailed Modeling- Switch Level Modeling, Strength Modeling

UNIT V

RTL Design and Test Sequential Multiplier- Shift-and- Add Multiplication process, sequential multiplier design, Multiplier testing, Von Neumann Computer Model- Processor and memory model, processor model specification,
designing the adding CPU, Design of datapath, Control part design, Adding CPU verilog description, tesing adding CPU

Text Books:

1. Zainalabdien Navabi, Verlog Digital System Design, TMH, 2nd edition.

Reference Books:

1. Fundamentals of Digital Logic with Verilog design by Stephen. Brown and Zvonko Vranesis, TMH, 2nd edition 2010.
2. Digital Logic Design using Verilog, State machine & synthesis for FPGA, Sunggulee, Cengage Learning, 2009
3. Verilog HDL- SamirPalnitkar, 2nd edition.
4. Advanced Digital Design with Verilog HDL- Michael D. Ciletti, PHI, 2005.

5. Digital Systems Design using VHDL- Charles H Roth, Jr. Thomson Publications, 2004

DIGITAL CMOS INTEGRATED CIRCUIT DESIGN
(Core II)

M.Tech (VLSISD) **I Year-I Semester**

Course Code: GM61B **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about Combinational, Sequential MOS logic circuits
- To introduce and familiarize with the various logic circuits.
- To prepare them to face the challenges in dynamic logic circuits.
- To create interest in the integrated circuit design and prepare them to face .the challenges in VLSI technology.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to know about the various Combinational and Sequential MOS logic circuits.
- An in-depth knowledge of applying the concepts on real time applications
- An ability to know the design of dynamic MOS logic circuits.
- Able to know the design of semiconductor memories.
- An ability to understand the basic concepts of Boolean expressions.

.

UNIT I

MOS Design: Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response,
Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates ,
AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT III

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits,
CMOS D latch and edge triggered flipflop.

UNIT IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits,
Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT V

Semiconductor Memories Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation,
SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

TEXT BOOKS

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

INSTITUTE OF ENGINEERING & TECHNOLOGY
(UGC Autonomous)
(Accredited by NAAC, Approved by AICTE & Permanently Affiliated to JNTUH)

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

DEVICE MODELLING
(Program Elective -I)

M.Tech (VLSISD) **I Year-I Semester**

Course Code: GM61C **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To impart to students knowledge of semi conductor physics and integrated passive devices.
- To enable students to analyze the behavior of monolithic diodes with the help of models of integrated diodes.
- To enable students to analyze the behavior of integrated NMOS and PMOS transistors with the help of SPICE models.
- To enable students visualize different VLSI fabrication techniques of different processes.
- To enable students to model hetero junction devices.

COURSE OUTCOMES

- The graduate student will be equipped with knowledge of semiconductor physics.
- The graduate student will be able relate model parameters to structures of integrated passive devices.
- The graduate will be able to analyze static and dynamic behavior of diodes.
- The graduate student will be able to model electrically NMOS and PMOS transistors.
- The graduate student will be able to use SPICE model level 1, 2,3and 4 and hence will be able to analyze various integrated circuits.
- The graduate student will have sound knowledge of VLSI fabrication technique details of different processes.
- The graduate student will be able to model electrically hetero junction devices.

UNIT I

Introduction to Semiconductor Physics:

Review of Quantum Mechanics, Boltzmann transport equation, Continuity equation, Poisson equation.

Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT -II

Integrated Diodes: Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models

Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model dynamic model, Parasitic effects – SPICE model –Parameter extraction

UNIT III

Integrated MOS Transistor:

NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects –

MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT IV

VLSI Fabrication Techniques: An overview of wafer fabrication, Wafer Processing – Oxidation –Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process –

CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements –Interconnects circuit elements

UNIT V

Modeling of Hetero Junction Devices: Band gap Engineering, Band gap Offset at abrupt Hetero Junction,

Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS

1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

DIGITAL SYSTEM DESIGN
(Program Elective -I)

M.Tech (VLSISD) **I Year-I Semester**

Course Code: GM61D **L/T/P/C: 3/0/0/3**

UNIT I

Minimization and Transformation of Sequential Machines: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT II

Digital Design: Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller

A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT III

SM Charts: State machine charts, Derivation of SM Charts, Realization of SM Chart,

Implementation of Binary Multiplier, dice game controller.

UNIT IV

Fault Modeling & Test Pattern Generation: Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT V

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment,

Machine identification, Design of fault detection experiment

TEXT BOOKS

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.

2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A.

Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH

2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.

3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

INSTITUTE OF ENGINEERING & TECHNOLOGY (UGC Autonomous)
(Accredited by NAAC, Approved by AICTE & Permanently Affiliated to JNTUH)

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

SCRIPTING LANGUAGES FOR VLSI
(Program Elective -I)

M.Tech (VLSISD) **I Year-I Semester**

Course Code: GM61E **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To describe the need of using scripting language programs.
- To use PERL scripting language at the instances required.
- To apply advanced level PERL for software automation.
- To employ the PERL scripting language for file system navigation.
- To illustrate software automation using TCL

COURSE OUTCOMES After going through this course the student will be able to

- The students will be in a position to judge whether scripting language program is needed for a particular code.
- Students will be acquainted with the basic level scripting language programming in PERL.
- Students will be skillful to code in PERL for advanced level software automation.

- Students will have the programming skills to automate the software for event-driven programs too.
- Students will be in a position to demonstrate software automation using Java Script, PERL-TK, and in basic level using python scripting language.

UNIT I

Introduction to Scripts and Scripting: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data,

Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT II Advanced PERL Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References,
Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT III

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output,
Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT IV

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware'
'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT V

TK and JavaScript: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes,
Encapsulation, Data Hierarchy.

TEXT BOOKS

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

REFERENCE BOOKS

1. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann SerieS.
2. Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindel Edition.

INSTITUTE OF ENGINEERING & TECHNOLOGY
(UGC Autonomous)
(Accredited by NAAC, Approved by AICTE & Permanently Affiliated to JNTUH)

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN
(Program Elective -II)

M.Tech (VLSISD) **I Year-I Semester**

Course Code: GM61F **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To introduce the outline architecture of ARM7 microcontroller including basics of pipelines, registers, exception modes.
- To set up and customize a microcontroller development environment.
- To give an overview of system peripherals which cover bus structure, memory map, register programming and much more.
- To write programs that interacts with other devices.
- To learn the Memory Management of RISC Microcontrollers.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to understand the hardware implementation of the ARM7microcontrollers.
- An ability to Integrate peripherals based on I/O functions.
- An ability to learn the concept of pipelines, registers and exception modes
- An ability to program in ARM and THUMB modes.
- An ability to interpret the functions of Memory Management Unit (MMU).
- An ability to compare the performance of various ARM families of Microcontrollers.
- An ability to know the software development flow and working with projects.

UNIT I

ARM Architecture: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline
Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT II

ARM Programming Model – I: Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load
Store Instructions, PSR Instructions, Conditional Instructions.

UNIT III

ARM Programming Model – II:
Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions Stack, Software Interrupt Instructions

UNIT IV

ARM Programming: Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic
Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT V

Memory Management: Cache Architecture, Polices, Flushing and Caches
MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

INSTITUTE OF ENGINEERING & TECHNOLOGY
(UGC Autonomous)
(Accredited by NAAC, Approved by AICTE & Permanently Affiliated to JNTUH)

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

(Program Elective -II)

M.Tech (VLSISD) **I Year-I Semester**

Course Code: GM61G **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To understand the concept of Programmable Logic Device architectures and technologies.
- Underlying FPGA architectures and technologies in detail.
- To understand the difference between CPLDs and FPGAs
- To provide knowledge about SRAM Programmable FPGA Device architecture.
- To comprehend knowledge about Anti-Fuse Programmable FPGA Device architecture.

COURSE OUTCOMES: After going through this course the student will be able to

- To know the concept of programmable architectures.
- Perceiving CPLD and FPGA technologies
- Study and compare the different architectures of CPLDs and FPGAs
- An ability to know the SRAM Technology based FPGAs
- An ability to know the Anti-Fuse Technology based FPGAs

UNIT I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic;

Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture
The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture,
The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator
A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

INSTITUTE OF ENGINEERING & TECHNOLOGY
(UGC Autonomous)
(Accredited by NAAC, Approved by AICTE & Permanently Affiliated to JNTUH)

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

VLSI TECHNOLOGY AND DESIGN
(Program Elective -II)

M.Tech (VLSISD) **I Year-I Semester**
Course Code: GM61H **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To enable the student to visualize MOS fabrication technologies and to understand electrical properties of MOS, CMOS and Bi CMOS circuits.
- To train the student to draw integrated circuit layouts following design rules.
- To enable the student design combinational circuit, do verification, power optimization and network testing.
- To enable the student to use power optimization techniques, design validation procedures and testing of sequential circuits.
- To train the student to use different floor planning methods and different low power architectures.

COURSE OUTCOMES: Graduate student will be able to

- Visualize the steps taken for MOS fabrication technologies.
- Analyze electrical behavior of MOS, CMOS and Bi-CMOS circuits.
- Draw the layout of integrated circuits following design rules.
- Design combinational circuit.
- Design sequential circuits using different clocking disciplines.
- Carry out power optimization techniques, design validation procedure and testing of circuits.
- Carry out floor planning for different low power architectures.

UNIT I

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo.

Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT II

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT III

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect design

Power optimization, Switch logic networks, Gate and Network testing.

UNIT IV

Sequential Systems: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT V

Floor Planning: Floor planning methods, Global Interconnect,
Floor Plan Design, Off-chip connections.

TEXT BOOKS

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

INSTITUTE OF ENGINEERING & TECHNOLOGY (UGC Autonomous)
(Accredited by NAAC, Approved by AICTE & Permanently Affiliated to JNTUH)

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

HDL SIMULATION LAB

M.Tech (VLSISD) **I Year-I Semester**
Course Code: GM61I **L/T/P/C: 0/0/4/2**

Objectives:

This lab deals with programming using Verilog for advanced digital design techniques. It offers board coverage of HDL from a practical design perspective. Introduces students to gate, dataflow(RTL) and behavioral modeling.

Note: All the following digital circuits are to be designed and implemented on FPGA using XILINX's/ Altera's/ Equivalent CAD tools.

Programming can be done using any HDL compiler, Verification of the Functionality of the module using functional Simulator, Timing Simulator for Critical Path tine Calculation, Synthesis of module, Place & Route and implementation of design using FPGA.

1. Digital Circuits Description using Verilog/ VHDL
2. Verification of the Functionality of designed Circuits using function Simulator.
3. Timing Simulation for critical path time calculation.
4. Synthesis of Digital Circuits.
5. Place and Route techniques for major FPGA vendors such as Xilinx/ Altera/ Actel etc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

DIGITAL CMOS IC DESIGN LABORATORY

M.Tech (VLSISD) **I Year-I Semester**
Course Code: GM61CJ **L/T/P/C: 0/0/4/2**

COURSE OBJECTIVES

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about Combinational, Sequential MOS logic circuits
- To introduce and familiarize with the various logic circuits.
- To prepare them to face the challenges in dynamic logic circuits.
- To prepare them to design various building blocks in combinational and sequential circuits.

COURSE OUTCOMES: After going through this course the student will be able to

- An ability to know about the various Combinational and Sequential MOS logic circuits.
- An in-depth knowledge of applying the concepts on real time applications
- An ability to understand the basic concepts of Boolean expressions.
- Able to design different Combinational logic blocks.
- Able to analyze and implement various memory elements.

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.

1. Design and Draw layout for CMOS Inverter gate and perform DRC, LVS, RC Extraction.
2. Design and Draw layout for CMOS NOR/ NAND gate and perform DRC, LVS, RC Extraction.

3. Design and Draw layout for CMOS XOR gate using Transmission Gates and perform DRC, LVS, RC Extraction.
4. Design and Draw layout for Full Adder using CMOS logic and perform DRC, LVS, RC Extraction.
5. Design and Draw layout for Latch using CMOS logic and perform DRC, LVS, RC Extraction.
6. Design and Draw layout for SRAM Design using CMOS logic and perform DRC, LVS, RC Extraction.

ANALOG CMOS INTEGRATED CIRCUIT DESIGN

Core-III

M.Tech (VLSISD) **I Year-II Semester**
Course Code: GM62A **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about fabrication process and technology
- To introduce and familiarize with the various Amplifiers &OP-amps
- To prepare them to face the challenges in CMOS technology

COURSE OUTCOMES:

After going through this course the student will be able to

- Able to develop an in-depth understanding of the design principles and applications of CMOS analog IC design
- An ability to know the fabrication steps involved in CMOS technology.
- Familiar with the small signal and large signal models of CMOS transistors
- An in-depth knowledge of applying the concepts on real time applications
- Analyze and design of CMOS op Amps and compensation techniques

UNIT I

MOS Devices and Modeling : The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model,

Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT II

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper,

Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT III

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers,

Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT IV

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps

Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT V

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop

Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

APPLICATION SPECIFIC INTEGRATED CIRCUITS

Core -IV

M.Tech (VLSISD) **I Year-II Semester**
Course Code: GM62B **L/T/P/C: 3/0/0/3**

UNIT I

Introduction to ASIC's and CMOS Logic Types of ASICs - Design flow - CMOS transistors - CMOS Design rules - Combinational Logic Cell –Sequential logic cell
Data path logic cell-Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

ASIC Library Design and Programmable Technologies
Library cell design - Schematic view of Library architecture - Anti fuse - Static RAM
EPROM and EEPROM technology - PREP benchmarks

UNIT II

ASIC Verification The Verification Process, The Verification Methodology Manual, Basic Test bench Functionality, Methodology Basics, Constrained-Random Stimulus, Functional Coverage
Test bench Components, Building a Layered Test bench, Simulation Environment Phases, Maximum Code Reuse, Test bench Performance

UNIT III

Synthesis and Static Timing Analysis: Logic Simulation – Types of Simulation – Synthesis: RTL and Technology Schematics- Schematic entry Needs for testing – Types of testing - Boundary scan test - Fault simulation - Automatic test pattern generation. Logic Synthesis and Optimization. Design levels.
Main concepts. Basic steps of synthesis. Logic synthesis. Specification. Design description. Design constraints. Logic circuit. Logic synthesis steps. Parameter trade-off. Cell logic model. Characterization,Timing and Area Constraints. Static Timing Analysis(STA)-Need of STA at Different Design Phases and Limitations.

UNIT IV

Design for Testability Challenges of DFT. Quality achievement problems. Systematic defects. Stuck-at fault model. Undetectable faults. Test coverage and fault coverage. Testing sequential designs. Scannable equivalent flip-flop. Scan testing protocol: example. Overlap of test patterns.

Scannable equivalent flip-flop. Ripple-counter violation. Ripple-counter RTL DFT solution. Physical-aware DFT flow. SCANDEF file. Re-partitioning with SCANDEF. Alpha-numeric ordering. Reordering within scan chain. Reordering across scan-chains. Clock tree based reordering. Placement-based scan chain routing. Increase of power consumption by scan testings.

UNIT V

Physical Design Physical design flow, System partition -Partitioning methods

Floor planning - Placement -– Global routing - Detailed routing - Circuit extraction – DRC.

Text Books

1. M.J.S .Smith, "Application Specific Integrated Circuits", Pearson Education, 2010.
2. Farzad Nekoogar and FaranakNekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.
3. D. Papa, I. Markov. "Multi-Objective Optimization in Physical Synthesis of Integrated Circuits" Springer; 2012.
4. V.Taraate, "Digital Logic Design Using Verilog: Coding and RTL Synthesis", Springer; 2016.

Reference Books

1. G.Hachtel, F. Somenzi. Logic Synthesis and Verification Algorithms. Springer; 2013
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.

LOW POWER VLSI DESIGN
(Program Elective -III)

M.Tech (VLSISD) **I Year-II Semester**

Course Code:GM62C **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To know about the need for low power circuit design.
- To provide strong foundation of fundamentals of low power circuit design.
- To furnish knowledge of various low power design approaches for VLSI System design.
- To analyze different low power design techniques.
- To develop different low voltage low power logic styles using low power techniques.

COURSE OUTCOMES

After going through this course the student will be able to

- Student develops strong knowledge of fundamentals of low power VLSI circuit design.
- Student will be aware of various low power VLSI design approaches.
- Student will be aware of various low power logic styles.
- Student will be able to analyze all the low power design techniques.
- Student will develop the capability of designing low power data path subsystems such as adders and multipliers.
- Student will be equipped with technical knowledge to design low power memories for a VLSI system.

Student will be able to design all low power circuit designs

UNIT I

Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation

Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT II

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches:

System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT III

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders Carry Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT IV

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier
Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT V

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit
Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

DESIGN FOR TESTABILITY
(Program Elective -III)

M.Tech (VLSISD) **I Year-II Semester**
Course Code:GM62D **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To provide knowledge about VLSI Testing.
- To understand VLSI Technology Trends affecting Testing
- To get knowledge on Design verification and Test Evaluation
- To understand the concept of BIST architecture.
- To provide knowledge about Boundary Scan Test.

COURSE OUTCOMES

- Create understanding of the fundamental concepts of Testing in VLSI design.
- Perceiving Trends affecting Testing
- An ability to know the high level testability measures and scan methods.
- An ability to know the BIST architecture: Test pattern generation, Circuit under test and Output response analyzer.
- Develop skills in modeling and evaluating Boundary Scan Standards.

UNIT I

Introduction to Testing Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT II

Logic and Fault Simulation:

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation

Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods

Scan Design, Partial-Scan Design, Variations of Scan.

UNIT IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction

Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions

Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

SYSTEM ON CHIP ARCHITECTURE
(Program Elective -III)

M.Tech (VLSISD) **I Year-II Semester**

Course Code:GM62E **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To describe the system design approach with respect to the hardware and software
- To apply the techniques for reducing the delays in program execution
- To categorize and compare different processor types for their selection into a System on Chip.
- To compare different memory designs and their purposes
- To interpret the architectures and applications of various buses.

COURSE OUTCOMES

After going through this course the student will be able to

- Students will be able to summarize all the components required for system design.
- Students will be acquired the techniques to minimize the delays for better performance of a system on chip.
- Students will be able to analyze different types of buses for respective applications.
- Students will be skilful to judge a configurable device based on the application requirement for a system on chip
- Students will have the technique to implement AES algorithm if required.

UNIT I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures

Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling.

Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time

Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V

Application Studies / Case Studies: SOC Design approach, AES algorithms,

Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India
Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley
Professional

REFERENCE BOOKS

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004,
Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded
Technology) – Jason Andrews – Newnes, BK and CDROM.

HARDWARE - SOFTWARE CO-DESIGN

(Program Elective -IV)

M.Tech (VLSISD) **I Year-II Semester**

Course Code:GM62F **L/T/P/C: 3/0/0/3**

Course Objectives

- Describeanembeddedsystemdesignflowfromspecificationtophysicalrealization
- Describe structural behavior of systems.
- Master complex systems.
- Devise new theories, techniques, and tools in design, implementation and testing.
- Master contemporary development techniques.

Course Outcomes

After going through this course the student will be able to

- Gain knowledge of contemporary issues and algorithms used.
- Know the interfacing components, different verification techniques and tools.
- Demonstrate practical skills in the construction of prototypes.
- Understand the use of modern hardware and software tools for building prototypes of embedded systems.
- Apply embedded software techniques to satisfy functional and response time requirements.

UNIT I

Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT II

Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT III

Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT IV

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent

Computations, interfacing components

design verification, implementation verification, verification tools, interface verification

UNIT V

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level

Specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos

System.

TEXT BOOKS

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - springer

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

OPTIMIZATION TECHNIQUES IN VLSI DESIGN
(Program Elective -IV)

M.Tech (VLSISD) **I Year-II Semester**

Course Code:GM62G **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To understand the trade offs among various design styles given a set of design constraints in physical design automation and to understand performance/area trade offs in a chip design process.
- To learn the various statistic modeling methods like Monte Carlo techniques and Pelgroms model etc.,
- To learn the implementation issues for digital design automation including optimization techniques.
- To understand concept of design optimization algorithms and their application to physical design automation.
- To understand the latest design techniques as practiced in the Industry for design layout optimization.

COURSE OUTCOMES

After going through this course the student will be able to

- Apply the appropriate design practices, emerging technologies, state-of-the-art design techniques, software tools, and research methods for IC design.
- Design the systems by using concepts of High level statistical, Gate level statistical analysis methods.
- Design the low power digital systems by applying appropriate partitioning and Floor planning algorithms.
- Design the real time applications using optimization techniques like Genetic Algorithms.
- Understand the concepts of geometric programming and convex functions.

UNIT –I

Statistical Modeling:

Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom‟s model, Principle component based modeling

Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT –II

Statistical Performance, Power and Yield Analysis:

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis

dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT –III

Convex Optimization:

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT –IV

Genetic Algorithm:

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation-partitioning-automatic placement, routing technology, Mapping for FPGA

Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

UNIT –V

GA Routing Procedures and Power Estimation:

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures

Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

TEXT BOOKS / REFERENCE BOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.
3. Convex Optimization - Stephen Boyd, Lieven Vandenberghe, Cambridge University Press, 2004.

INSTITUTE OF ENGINEERING & TECHNOLOGY
(UGC Autonomous)
(Accredited by NAAC, Approved by AICTE & Permanently Affiliated to JNTUH)

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

IMAGE AND VIDEO PROCESSING
(Program Elective -IV)

M.Tech (VLSISD) **I Year-II Semester**

Course Code:GM62H **L/T/P/C: 3/0/0/3**

Course Objectives

- To understand representation of digital images and video in the spatial (pixel) and frequency domains, and learn common digital video formats.
- To understand spatial and temporal resolution and aliasing; understand basic image and video filtering operations.
- To understand principles and methods of motion/optical flow estimation; understand fundamentals of image compression.
- To understand fundamentals of video compression; learn recent image and video compression standards.

Course outcomes

- To implement image and video processing algorithms using MATLAB or another programming language.
- Able to analyze and interpret the results of image processing methods and algorithms.
- Get broad exposure to and understanding of various applications of image processing in industry, medicine, and defense.
- Learn the signal processing algorithms and techniques in image enhancement and image restoration.

UNIT –I

Fundamentals of Image Processing and Image Transforms:

Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.

Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT –II

Image Enhancement:

Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Basics of filtering in frequency domain, Image smoothing, Image sharpening, Selective filtering.

UNIT –III

Image Compression:

Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless Huffman coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT –IV

Basic Steps of Video Processing:

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT –V

2-D Motion Estimation:

Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation

Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

1. Digital Image Processing – Gonzaleze and Woods, 3rd Ed., Pearson.
2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFRENCE BOOKS:

1. Digital Image Processing using MATLAB– Gonzaleze and Woods, 2nd ed., Mc Graw Hill Education, 2010
2. Image Processing Analysis , and Machine Vision- Milan Sonka, Vaclan Hlavac, 3 ed., CENGAGE, 2008
3. Digital Video Processing – A Murat Tekalp, PERSON, 2010
4. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar –TMH, 2009

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

ANALOG CMOS IC DESIGN LAB

M.Tech (VLSISD) **I Year-II Semester**

Course Code:GM62I **L/T/P/C: 0/0/4/2**

COURSE OBJECTIVES

- To describe over view about evolution of CMOS integrated circuits.
- To provide knowledge about fabrication process and technology
- To introduce and familiarize with the various Amplifiers &OP-amps
- To prepare them to face the challenges in CMOS technology

COURSE OUTCOMES

After going through this course the student will be able to

- Able to develop an in-depth understanding of the design principles and applications of CMOS analog IC design
- An ability to know the fabrication steps involved in CMOS technology.
- Familiar with the small signal and large signal models of CMOS transistors
- An in-depth knowledge of applying the concepts on real time applications
- Analyze and design of CMOS op Amps and compensation techniques

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.

1. Analyze the NMOS and PMOS Operating point Characteristics.

2. Design a CMOS Current Mirror and find out the AC, DC, OP analysis.
3. Design a NMOS Differential Amplifier and find out the AC, DC, OP analysis.
4. Design a PMOS Differential Amplifier and find out the AC, DC, OP analysis.
5. Design a CMOS Operational Amplifier and find out the AC analysis and noise margin analysis.
6. Design a comparator using Operational Amplifier and find out the AC analysis.
7. Draw the Analog Layout for CMOS current Mirror and perform DRC, LVS, RC Extraction.

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY
ASIC DESIGN LAB

M.Tech (VLSISD) **I Year-II Semester**

Course Code:GM62J **L/T/P/C: 0/0/4/2**

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.

1. Develop Verification environment using system Verilog for any one digital system.
2. Design and analyze the performance with respect to area, power and speed for different Adders using ASIC Logic Design Tools.
3. Design and analyze the performance with respect to area, power and speed for different Multipliers using ASIC Logic Design Tools.
4. Perform Synthesis for any digital system to meet the given specifications.
5. Perform Static Timing Analysis for any digital system to meet the given specifications.
6. Perform Floor planning, , clock tree synthesis, Placement and Routing, RC extraction for given netlist to meet the specifications.

ADVANCED COMPUTER ARCHITECTURE
(Program Elective -V)

M.Tech (VLSISD) **II Year-I Semester**

Course Code: GM63A **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To learn how to build the best processor/computing system understanding the underlying trade offs and ramifications.
- To identify and analyze the attributes of computer architecture design with recent trend technology.
- To identify the techniques to improve the speed and performance of computers – Parallelism in Instruction level – Hardware approaches - pipelining, dynamic scheduling, superscalar processors, and multiple issue of instructions.
- To implement the design aspects and categorize various issues , causes and hazards due to parallelisms.
- To examine and compare the performance with benchmark standards.

COURSEOUTCOMES

After going through this course the student will be able to

- An ability to discuss the organisation of computer-based systems and how a range of design choices are influenced by applications.
- An ability to understand the components and operation of a memory hierarchy and the range of performance issues influencing its design.
- An ability to interpret the organisation and operation of current generation parallel computer systems, including

multiprocessor and multi core systems.

- An ability to understand the various techniques to enhance a processors ability to exploit instruction-level parallelism (ILP), and its challenges.
- An ability to undertake performance comparisions of modern and high performance computers.

UNIT I

Fundamentals of Computer Design:

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design

Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

UNIT II

Pipelines:

Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design:

Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT III

Instruction Level Parallelism (ILP) - The Hardware Approach:

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach:

Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT IV

Multi Processors and Thread Level Parallelism:

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture

Distributed shared – Memory architecture, Synchronization.

UNIT V

Inter Connection and Networks:

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super
Scalar Processors

2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

CAD FOR VLSI CIRCUITS

(Program Elective -V)

M.Tech (VLSISD) **I Year-II Semester**

Course Code:GM63B **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVE

- To provide an introduction to the fundamentals of Computer-Aided Design tools for the modelling, design, analysis, test, and verification of digital Very Large Scale Integration (VLSI)systems.
- To study various physical design methods inVLSI
- To understand the concepts behind the VLSI design rules and routingtechniques.
- To use the simulation techniques at various levels in VLSI designflow
- To understand the concepts of various algorithms used for floor planning and routing techniques.

COURSE OUTCOME

After going through the course students will be able to

- Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development andenhancement.
- TopracticetheapplicationoffundamentalsofVLSItechnologies
- Optimize the implemented design for area, timing and power by applying suitable constraints.
- To gain knowledge on the methodologies involved in

design, verification and implementation of digital designs on reconfigurable hardware platform(FPGA)

UNIT I

VLSI Physical Design Automation:

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle

New Trends in Physical Design Cycle, Design Styles, System Packaging Styles;

UNIT II

Partitioning, Floor Planning, Pin Assignment and Placement:

Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization

Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments, Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms;

UNIT III

Global Routing and Detailed Routing:

Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms

Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms;

UNIT IV

Physical Design Automation of FPGAs:

FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model;

Physical Design Automation of MCMs:

Introduction to MCM Technologies, MCM Physical Design Cycle.

UNIT V

Chip Input and Output Circuits:
ESD Protection, Input Circuits, Output Circuits and noise
On-chip clock Generation and Distribution, Latch-up and its prevention.

TEXT BOOKS

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

CMOS MIXED SIGNAL CIRCUIT DESIGN
(Program Elective -V)

M.Tech (VLSISD) **IIYear-II Semester**

Course Code:GM63C **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- This course provides the concepts of switched capacitor circuits used in mixed signal circuit design.
- To know mixed signal circuits like DAC, ADC, PLLetc.,
- To acquire knowledge on design different architectures in mixed signal mode.
- To gain knowledge on noise shaping modulators and higher order modulators.
- It deals with the design and analysis of Biquad Filters.

COURSE OUTCOMES

After going through this course the student will be able to

- Analyze and design of switched capacitor circuits used in mixed signal circuit design
- Design noise shaping converters given a set of requirements such as bandwidth, clock speed and signal-to-noise ratio
- Design an integrated mixed signal circuit in CMOS using modern design tools
- Demonstrate in-depth knowledge in PLL and Data Converters (DAC andADC)
- Analyze complex engineering problems critically for conducting research in data converters

UNIT I

Switched Capacitor Circuits:

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits

Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNITII

Phased Lock Loop (PLL):

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump

Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT III

Data Converter Fundamentals:

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters

Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT IV

Nyquist Rate A/D Converters:

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters

Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT V

Oversampling Converters:

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators

Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inderscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Inderscience, 2009.

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES (OPEN ELECTIVE)

M.Tech (VLSISD) **I Year-II Semester**

Course Code:GM6OA **L/T/P/C: 3/0/0/3**

COURSE OBJECTIVES

- To provide sound foundation of digital signal processing (DSP) architectures for designing efficient VLSI architectures for DSP systems.
- To analyze general purpose digital signal processors.
- To understand pipelining, parallel processing and retiming.
- To illustrate the features of on-chip peripheral devices and its interfacing along with its programming details.
- To analyze DSP architectures.

COURSE OUTCOMES

After going through this course the student will be able to An ability to design analog and digital filters for signal-processing applications.

- An ability to recognize the fundamentals of fixed and floating point architectures of various DSPs.
- An ability to learn the architecture details and instruction sets of fixed and floating point DSPs.
- An ability to Infer about the control instructions, interrupts, and pipeline operations.
- Anabilitytoanalyzeandlearntoimplementthesignalprocessingal gorithmsinDSPs.
- An ability to learn the DSP programming tools and use them for applications.

UNIT I

Introduction to Digital Signal Processing: Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT)

Linear time-invariant systems, Digital filters, Decimation and interpolation.

UNIT II

Computational Accuracy in DSP Implementations:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors

DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory

Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT IV

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors

Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT V

Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.

Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware

Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.

AD-HOC WIRELESS NETWORKS

(OPEN ELECTIVE)

Course Code:GM6OB
L/T/P/C: 3/0/0/3

Course Objectives:

- To understand aspects of ad hoc networks from design through performance issues to application requirements.
- To understand characteristics features applications of ad hoc networks, Modulation techniques and voice coding.
- To Understand IEEE 802.11 Wireless LAN and Bluetooth standards.

Course Outcomes:

- Able to gain an understanding of the current topics in MANETs and WSNs, both from an industry and research point of views. ·
- Able to understanding of the principles of mobile ad hoc networks (MANETs) and what distinguishes them from infrastructure-based networks. ·
- Will be able to analyze proactive routing protocols function and their implications on data transmission delay and bandwidth consumption.

UNIT – I

Wireless Local Area Networks:

Introduction, wireless LAN Topologies, Wireless LAN Requirements, Physical Layer- Infrared Physical Layer, Microwave based Physical Layer Alternatives, Medium Access Control Layer- HIPERLAN 1 Sublayer, IEEE 802.11 MAC Sublayer and Latest Developments- 802.11a, 802.11b, 802.11g

Personal Area Networks: Introduction to PAN technology and Applications, Bluetooth -specifications, Radio Channel, Piconets and Scatternets, Inquiry, Paging and Link Establishment, Packet Format, Link Types, Power Management, Security, Home RF -Physical and MAC Layer

UNIT – II

MAC Protocols:

Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols

Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT – III

Routing Protocols:

Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols

Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT – IV

Transport Layer Protocols:

Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks

Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT – V

Quality of Service in Ad Hoc Wireless Networks:

Introduction, Real Time Traffic Support in Ad Hoc Wireless Networks, QoS Parameters in Ad Hoc Wireless Network, Issues and Challenges in providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions: MAC Layer Solutions, Cluster TDMA, IEEE 802.11e, DBASE, Network Layer Solutions

QoS Routing Protocols, Ticket Based QoS Routing Protocol, Predictive

Location Based QoS routing protocol, Trigger Based Distributed QoS Routing Protocol, QoS enabled AODV Routing Protocol, Bandwidth QoS Routing Protocol, On Demand QoS Routing Protocol, On Demand Link-State Multipath QoS Routing Protocol, Asynchronous Slot Allocation Strategies. QoS Frameworks for Ad Hoc Wireless Networks.

TEXT BOOKS:

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Networks -P Nicopolitidis and M S Obaidat, Wiley India Edition 2003.

REFERENCE BOOKS

1. Wireless Communication Technology- Roy Blake, CENGAGE,2012

Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press.

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

AUDIT COURSES

ENGLISH FOR RESEARCH PAPER WRITING

Course Code: **L/T/P/C: 2/0/0/2**

Course objectives:

- To state how to put research on paper
- To demonstrate how to write an abstract
- To apply the process of research
- To appraise the key skills involved in writing the title, abstract, introduction and review of literature
- To compose a paper which is good and has the qualities of acceptance and publication

Course Outcomes:

- Will be able to understand how to write a research paper
- Will outline the drafting of an abstract
- Will acquire the skills of various elements of research
- Will be in a position to write a good paper
- Will result in increasing the chance of publication

Unit1: Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

Unit 2: Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction.

Unit 3: Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

Unit 4: Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an

Introduction, skills needed when writing a Review of the Literature.

Unit 5: Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusion.

Unit 6: Useful phrases, how to ensure paper is as good as it could possibly be the first- timesubmission.

Reference Books:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on GoogleBooks)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge UniversityPress
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook.
4. Ian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

DISASTER MANAGEMENT

Course Code: L/T/P/C: 2/0/0/2

Course Objectives:

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Critically understand the strengths and weaknesses of disaster management approaches,
- Planning and programming in different countries, particularly their home country or the countries they work in.

Course Outcomes:

- Capacity to integrate knowledge and to analyze, evaluate and manage the different public health aspects of disaster events at a local and global levels, even when limited information is available.
- Capacity to describe, analyze and evaluate the environmental, social, cultural, economic, legal and organizational aspects influencing vulnerabilities and capacities to face disasters.
- Capacity to work theoretically and practically in the processes of disaster management (disaster risk reduction, response, and recovery) and relate their interconnections, particularly in the field of the Public Health aspects of the disasters.
- Capacity to manage the Public Health aspects of the disasters.
- Capacity to obtain, analyze, and communicate information on risks, relief needs and lessons learned from earlier disasters in order to formulate strategies for mitigation in future scenarios with the ability to clearly present and discuss their conclusions and the knowledge and arguments behind them.

Unit I

Introduction: Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Unit II

Repercussions of Disasters and Hazards: **Economic Damage**, Loss of Human and Animal Life, Destruction of Ecosystem. **Natural Disasters**: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

Unit III

Disaster Prone Areas in India: Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides and Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

Unit IV

Disaster Preparedness and Management: Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

Unit V

Risk Assessment: Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co- Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

Unit VI

Disaster Mitigation: Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Reference Books:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal bookCompany
2. Sahni, PardeepEt.Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall Of India, NewDelhi.
3. Goel S. L., Disaster Administration And Management Text And Case Studies" ,Deep &Deep Publication Pvt. Ltd., NewDelhi.

SANSKRIT FOR TECHNICAL KNOWLEDGE

Course Code:
L/T/P/C: 2/0/0/2

Course objectives:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects
- Enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Course Outcomes*:*

- Understanding basic Sanskrit alphabets and Understand tenses in Sanskrit Language.
- Enable students to understand roots of Sanskrit language.
- Students learn engineering fundamentals in Sanskrit.
- Students can attempt writing sentences in Sanskrit.
- Ancient Sanskrit literature about science & technology can be understood

Unit 1: Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences

Unit 2: Order, Introduction of roots, Technical information about Sanskrit Literature

Unit 3: Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

Reference Books:

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, NewDelhi
2. "Teach Yourself Sanskrit" PrathamaDeeksha-VempatiKutumbshastri, RashtriyaSanskrit Sansthanam, New DelhiPublication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., NewDelhi.

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

VALUE EDUCATION

Course Code:
L/T/P/C: 2/0/0/2

Course Objectives:

- Understand value of education and self-development
- Imbibe good values in students
- Let the should know about the importance of character
- To understand the significance of human conduct and self-development
- To enable students to imbibe and internalize the value and Ethical behaviour in personal and professional lives.

Course outcomes: Students will be able to

- Knowledge of self-development
- Learn the importance of Human values
- Developing the overall personality
- Student will be able to realize the significance of ethical human conduct and self-development
- Students will be able to inculcate positive thinking, dignity of labor and religious tolerance.

Unit 1: Values and self-development –Social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non- moral valuation, Standards and principles, Value judgment.

Unit 2: Importance of cultivation of values, Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

Unit 3: Personality and Behavior Development - Soul and Scientific attitude, Positive Thinking, Integrity and discipline, Punctuality, Love and Kindness, Avoid fault Thinking, Free from anger, Dignity of labour, Universal brotherhood and religious tolerance, True friendship, Happiness vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, Doing best for saving nature.

Unit 4: Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

Reference Books:

1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi.

INSTITUTE OF ENGINEERING & TECHNOLOGY (UGC Autonomous)
(Accredited by NAAC, Approved by AICTE & Permanently Affiliated to JNTUH)

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

INDIAN CONSTITUTION

Course Code:
L/T/P/C: 2/0/0/2

Course Objectives:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
- Role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.
- To understand the role and functioning of Election Commission of India.

Course Outcomes: Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of1956.
- Discuss the significance of Election Commission of India.

Unit 1: History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working).

Unit 2: Philosophy of the Indian Constitution: Preamble Salient Features.

Unit 3: Contours of Constitutional Rights &Duties: Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

Unit 4: Organs of Governance: Parliament-Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

Unit 5: Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

Unit 6: Election Commission: Election Commission: Role and Functioning, Chief Election Commissioner and Election Commissioners, State Election Commission: Role and Functioning, Institute and Bodies for the welfare of SC/ST/OBC and women.

Reference Books:

1. The Constitution of India, 1950 (Bare Act), GovernmentPublication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition,2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis,2015.

PEDAGOGY STUDIES

Course Code:
L/T/P/C: 2/0/0/2

Course Objectives:

- Review existing evidence on the review topic to inform Programme design and policy making
- Undertaken by the DFID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.
- Establishing coordination among people in order to execute pedagogy methods.
- To study pedagogy as a separate discipline.

Course Outcomes: Students will be able to understand

- What pedagogical practices are being used by teachers in formal classrooms in developing countries?
- What pedagogical practices are being used by teachers in informal classrooms in developing countries?
- Synergy from the work force.
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

Unit 1: Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

Unit 2: Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

Unit 3: Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

Unit 4: Professional development: alignment with classroom practices and follow- up support, Peer support, Support from the head teacher and the community, Curriculum and assessment, Barriers to learning: limited resources and large class sizes

Unit 5: Research gaps and future directions: Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

Reference Books:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3):361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London:DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3):272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston :Blackwell.

6. Chavan M (2003) Read India: A mass scale, rapid, ‘learning to read’campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

J.B.INSTITUTE OF ENGINEERING AND TECHNOLOGY

STRESS MANAGEMENT BY YOGA

Course Code:
L/T/P/C: 2/0/0/2

Course Objectives:

- To achieve overall Good Health of Body and Mind.
- To lower blood pressure and improve heart health.
- To become non-violent and truthfulness.
- To increase the levels of happiness.
- To eliminate all types of body pains.

Course Outcomes: Students will be able to

- Develop healthy mind in a healthy body thus improving social health also improve efficiently.
- Develop body awareness. Learn how to use their bodies in a healthy way. Perform well in sports and academics.
- *Will balance*, *flexibility*, and stamina, strengthen *muscles* and connective tissues enabling good *posture*.
- Manage stress through breathing, awareness, meditation and healthy movement.
- Build concentration, confidence and positive self-image.

Unit 1: Definitions of Eight parts of yog. (Ashtanga)

Unit 2: Yam and Niyam. Do`s and Don't's inlife. Ahinsa, satya, astheya, bramhacharya and aparigraha Shaucha, santosh, tapa, swadhyay,ishwarpranidhan

Unit 3: Asan andPranayam, Various yog poses and their benefits for mind & body. Regulaization of breathing techniques and its effects-Types of pranayam

Reference Books:

1. 'Yogic Asanas for Group Tarining-Part-I" : Janardan Swami YogabhyasiMandal,Nagpur
2. "Rajayoga or conquering the Internal Nature" by SwamiVivekananda, AdvaitaAshrama(Publication Department),Kolkata

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

Course Code:
L/T/P/C: 2/0/0/2

Course Objectives:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students
- To differentiate three types of happiness (Sukham)
- To describe the character traits of a spiritual devotee

Course Outcomes:

- Study of Shrimad- Bhagwad-Gita wiil help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- To develop self-developing attitude towards work without self-aggrandizement
- To develop tranquil attitude in all favorable and unfavorable situations
- To develop high spiritual intelligence

Unit 1: Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride &heroism)
- Verses- 26,28,63,65 (virtue)
- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

Unit 2: Approach to day to day work and duties.

- Shrimad Bhagwad Geeta : Chapter 2-Verses 41,47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23,35,
- Chapter 18-Verses 45, 46,48.

Unit 3: Statements of basic knowledge.

- Shrimad BhagwadGeeta: Chapter2-Verses 56, 62,68
- Chapter 12 -Verses 13, 14, 15, 16,17,18
- Personality of Role model. Shrimad Bhagwad Geeta: Chapter2-Verses 17, Chapter 3-Verses36,37,42,
- Chapter 4-Verses 18,38,39
- Chapter18 – Verses37,38,63

Reference Books:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department),Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, NewDelhi.